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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Cycle** | **reset** | **pc** | **instr** | **branch** | **srca** | **srcb** | **aluout** | **zero** | **pcsrc** | **writedata** | **memwrite** | **read data** |
| 1 | 1 | 00 | addi $2,$0,5  20020005 | 0 | 0 | 5 | 5 | 0 | 0 | 0 | 0 | x |
| 2 | 0 | 04 | addi $3,$0,12  2003000c | 0 | 0 | c | c | 0 | 0 | 0 | 0 | x |
| 3 | 0 | 08 | addi $7,$3,-9  20067fff7 | 0 | c | -9 | 3 | 0 | 0 | 0 | 0 | x |
| 4 | 0 | 0C |  |  |  |  |  |  |  |  |  |  |
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**Table 1. First sixteen cycles of executing mipstest.asm**



**Single-cycle MIPS processor**

# Extended functionality. Main Decoder:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **Op5:0** | **RegWrite** | **RegDst** | **AluSrc1:0** | **Branch** | **MemWrite** | **MemtoReg** | **ALUOp1:0** | **Jump** |  |  |  |
| R-type | 000000 | 1 | 1 | 00 | 0 | 0 | 0 | 10 | 0 |  |  |  |
| lw | 100011 | 1 | 0 | 01 | 0 | 0 | 1 | 00 | 0 |  |  |  |
| sw | 101011 | 0 | X | 01 | 0 | 1 | X | 00 | 0 |  |  |  |
| beq | 000100 | 0 | X | 00 | 1 | 0 | X | 01 | 0 |  |  |  |
| addi | 001000 | 1 | 0 | 01 | 0 | 0 | 0 | 00 | 0 |  |  |  |
| j | 000010 | 0 | X | XX | X | 0 | X | XX | 1 |  |  |  |
| ori | 001101 |  |  |  |  |  |  |  |  |  |  |  |
| bne | 000101 |  |  |  |  |  |  |  |  |  |  |  |

**Extended functionality. ALU Decoder:**

|  |  |
| --- | --- |
| **ALUOp1:0** | **Meaning** |
| 00 | Add |
| 01 | Subtract |
| 10 | Look at funct field |
| 11 |  |