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Assignment 0

CPE 301 – 1001

0. PART 0

The assignment took me an overall 30 minutes to complete. I got a little bit carried away going through some features Atmel studio offered.

1. PART A

My design consists of three distinct integers greater than 30 but less than 60 being added up to produce a sum and determine if at any given time there was an overflow. I consider the integer values to be signed, therefore the sum must be between $-2^7 \dots (2^7 - 1)$ otherwise an overflow would occur because our MSB would be one (0b1xxx_xxxx), hence it's a negative in 2s compliment. Once an overflow is detected it goes to a label Overflow, configures PortB bit positon 4 to be an output while the rest to be inputs and after PortB bit position 4 will be assigned a high to output. The code then continues; however, this time I intentionally let add integers that sum produce a value less than 127. Thus when I sum up the signed integer values the overflow flag should never be set and should branch to the noOverflw label. Once at the noOverflw label it configure PortB bit position 2 to be an output and output a low.
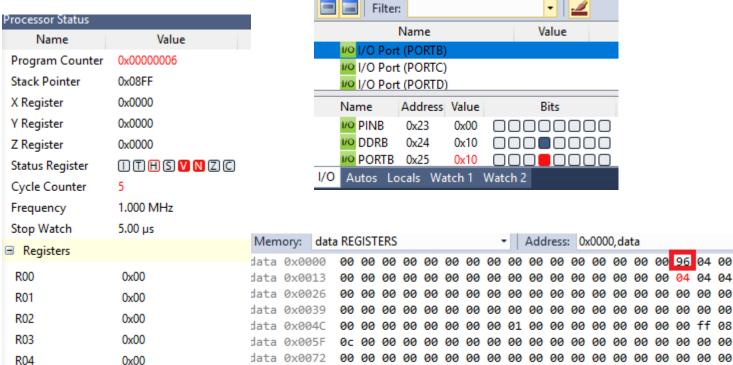
PART B

```
;
; DA0_1.asm
;
; Created: 1/24/2017 3:22:31 PM
; Author : Luis
;

; Replace with your application code
main:

    LDI r16,55            ;r16 = 55
       LDI r17,45         ;r17 = 45
       ADD r16,r17        ;r16 += r17 (r16 = 45 + 55)
       brvs Overflw       ;if Overflow flag is set goto Overflw
```

```asm
        LDI r17, 50           ;r17 = 50
        ADD r16,r17           ;r16 += r17 (r16 = 100 + 50)

        ;flag should set here and goto Overflw
        brvs Overflw  ;if Overflow flag is set goto Overflw

    ;I intentionally add numbers that add
    ; and create a sum less than 127
    back:

        LDI r16,31            ;r16 = 31
        LDI r17,32            ;r17 = 32
        ADD r16,r17           ;r16 += r17 (r16 = 31 + 32)
        LDI r17, 33           ;r17 = 33
        ADD r16,r17           ;r16 += r17 (r16 = 63 + 33)

        ;the overlow flag shoul be zero and go to noOverflw
        brvc noOverflw        ;if Overflow flag is not set goto NoOverflw
        rjmp end

    Overflw:
        LDI r17, 0x10         ;r16 = 0b0000_0100
        OUT DDRB, r17         ;configure Port B bits input: 7:3 & 1:0, output: 2
        OUT PORTB, r17        ;turn PortB on
        rjmp back

    noOverflw:
        LDI r16, 0x10         ;r16 = 0b0000_0100
        OUT DDRB, r16         ;configure Port B bits input: 7:3 & 1:0, output: 2
        LDI r16, 0x00         ;r16 = 0b0000_0000
        OUT PORTB, r16

    end:nop
```
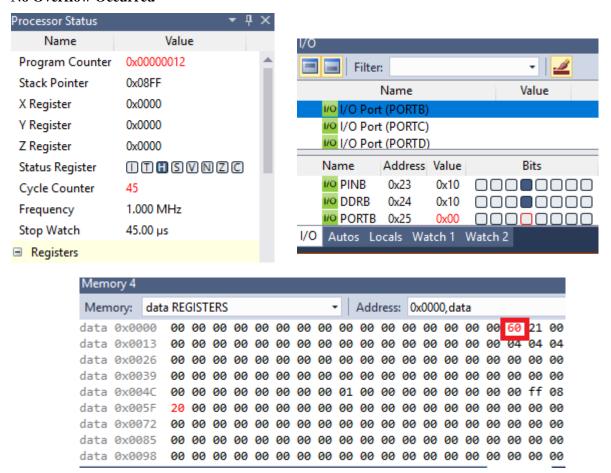
PART C

Overflow Occurred

The running sum was being held by reg16 (0x10) which indicates a value of 150, it is pass the signed

value of 127 thus an overflow

No Overflow Occurred

The overflow flag doesn't get set since r16 value is 112 and is less than 127 therefore PORTB bit position

3 outputs a low

PART D

URL Video of Design Assignment 0: https://youtu.be/yx41uX9qbLM

PART E

Status Register   □□**H**□□□

Cycle Counter   23

Frequency   8.000 MHz

Stop Watch   2.88 µs

$$Execution\ Time = \frac{Cycle\ Counter}{Frequency} = \frac{23}{8.00 MHz} \approx 2.88\ µs$$