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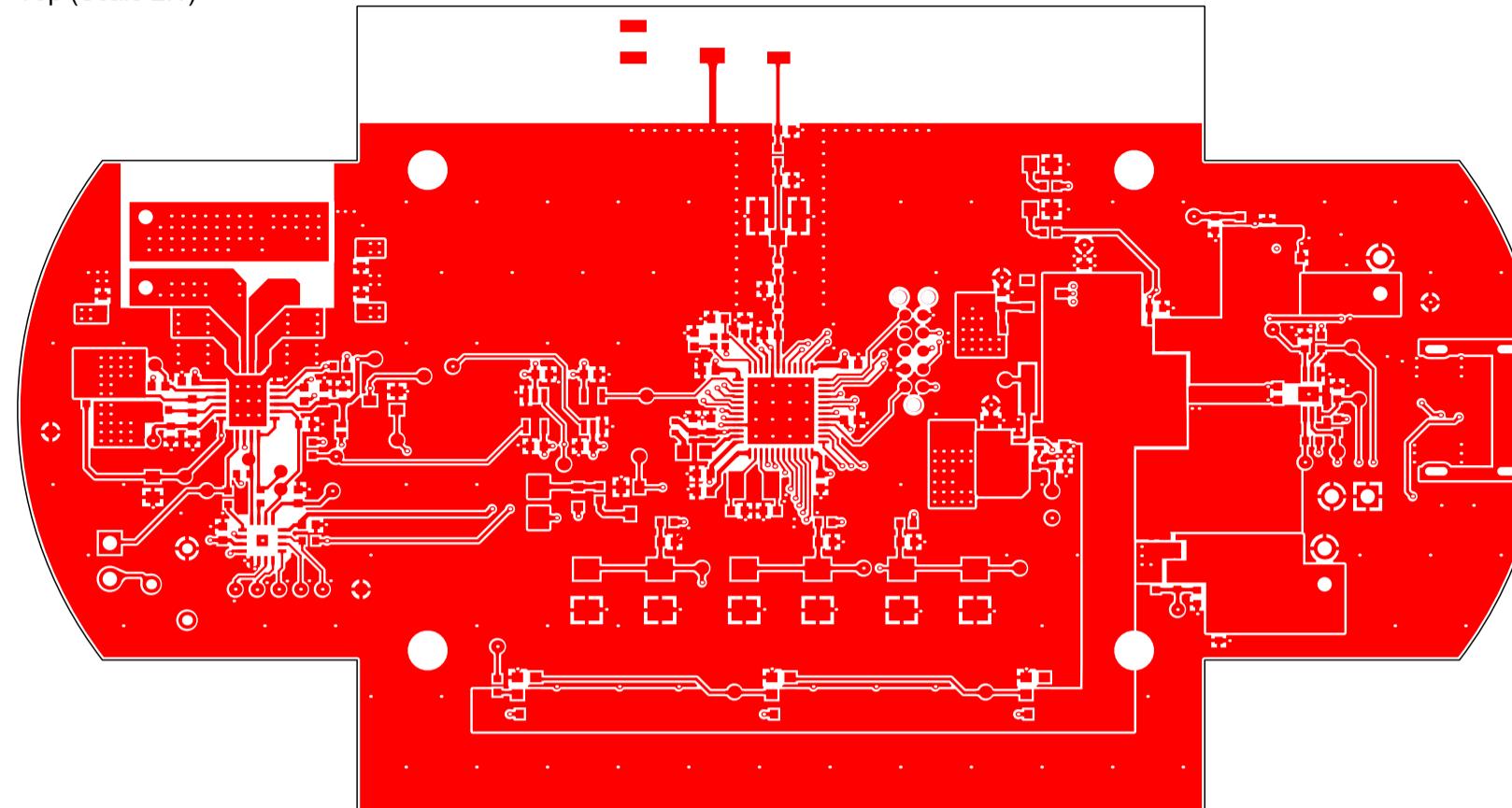
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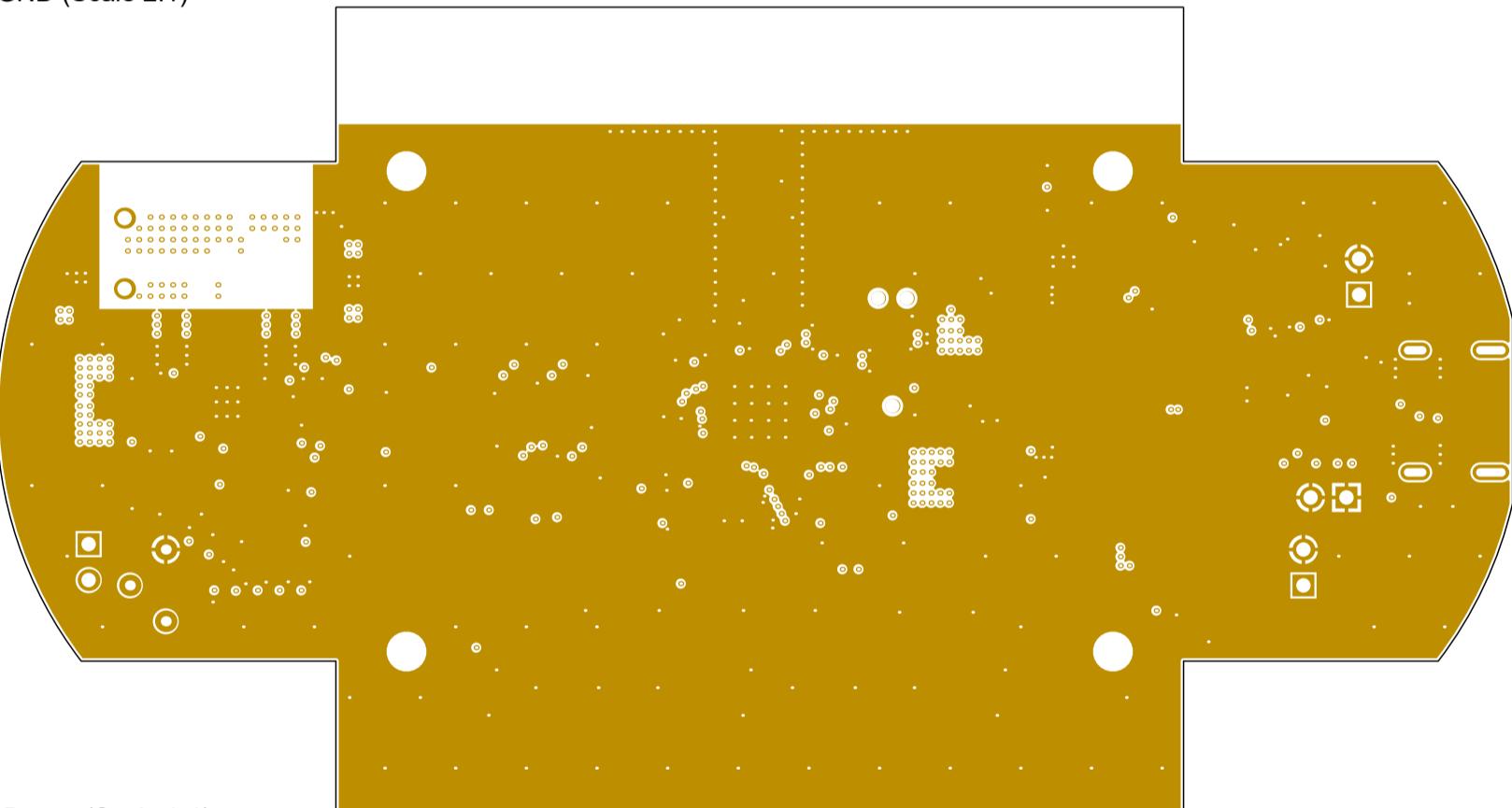
H

## Fabrication View / Notes

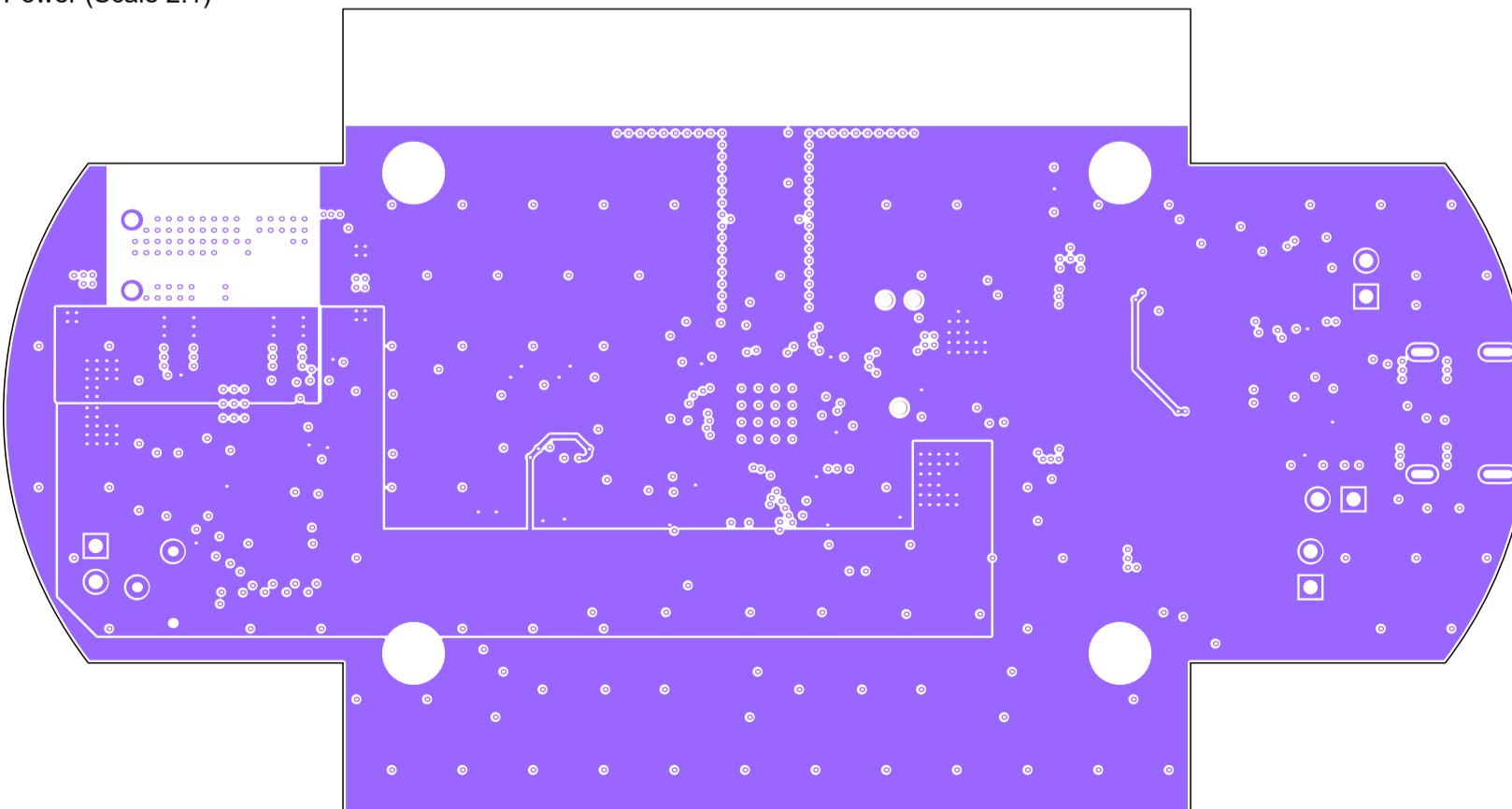
Top (Scale 2:1)



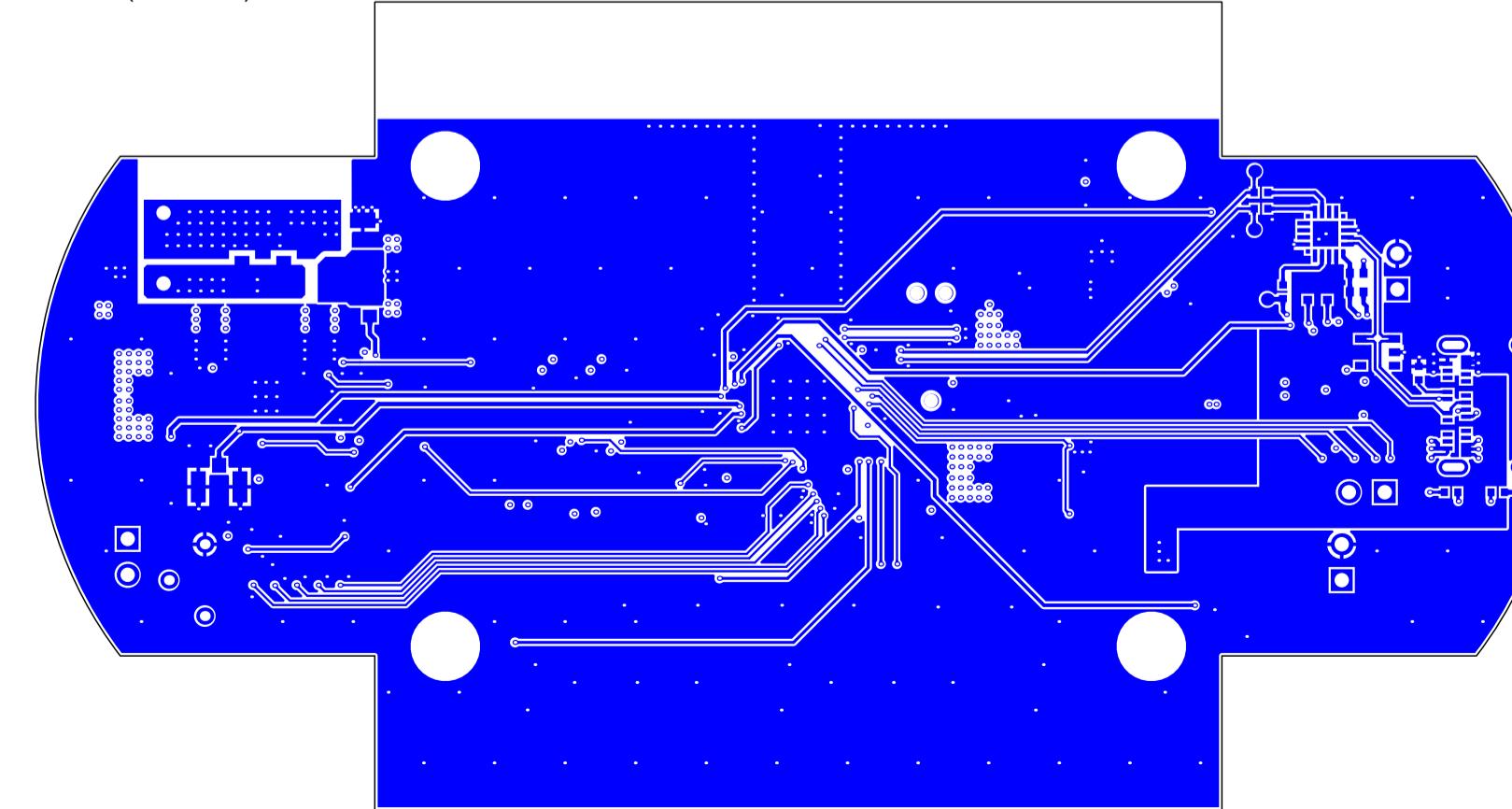
GND (Scale 2:1)



Power (Scale 2:1)



Bottom (Scale 2:1)



Notes: Unless otherwise specified, all dimensions are in mm.

1. Board material is FR4 RoHS 140°C Tg or higher.
2. RoHS compliant materials to be used for lead-free assembly process. Finished boards shall be free of oils, lubricants or other contaminants.
3. Minimum trace width/spacing is 0.152 mm / 0.152 mm.
4. Surface finish must be ENIG (Electroless Nickel Immersion Gold).
  - Electroless nickel thickness: 3 - 6um (refer to IPC-4552).
  - Immersion gold thickness: 0.05um minimum.
5. Layer stack can be modified. Final stackup to be approved by Focus.
6. All boards to pass 100% continuity test for opens and shorts.
7. Impedance control and verification is only required if an impedance table is provided. Refer to the table for the final characteristic impedance of different traces. Fabricator may modify designed trace width.
8. The serial number format to be placed in silkscreen in the space marked by SN. The serial number format is as follows: VerMay.VerMin.Rev-XXXX. VerMay is the major version which is 1, VerMin is the minor version which is 2 and XXXX is the number assigned to the board for its identification, starting in 0001.
9. Silkscreen (overlay) is white.
10. Soldermask colour is black.
11. Manufacturer must provide final gerber files before starting production.

	FOCUS	Project: WPTChargerMain.PrjPcb
Title:	Draftman	Ver: 1.2
Design by:	Mathias Ferreira	Date: 28/08/2024
Reviewed by:	Julian Evia	Date: 28/08/2024
Comments:		

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# Drill drawings

Drill Drawing View (Scale 4:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
x	577	0.20mm	Plated	
□	3	0.71mm	Plated	
◊	3	0.99mm	Non-Plated	
▽	10	1.02mm	Plated	
✳	2	1.60mm	Plated	
✳	2	2.10mm	Plated	
○	4	2.30mm	Non-Plated	
601 Total				

	FOCUS	Project: WPTChargerMain.PjrPcb
Title:	Draftman	Ver: 1.2
Design by:	Mathias Ferreira	Date: 28/08/2024
Reviewed by:	Julian Evia	Date: 28/08/2024
Comments:		

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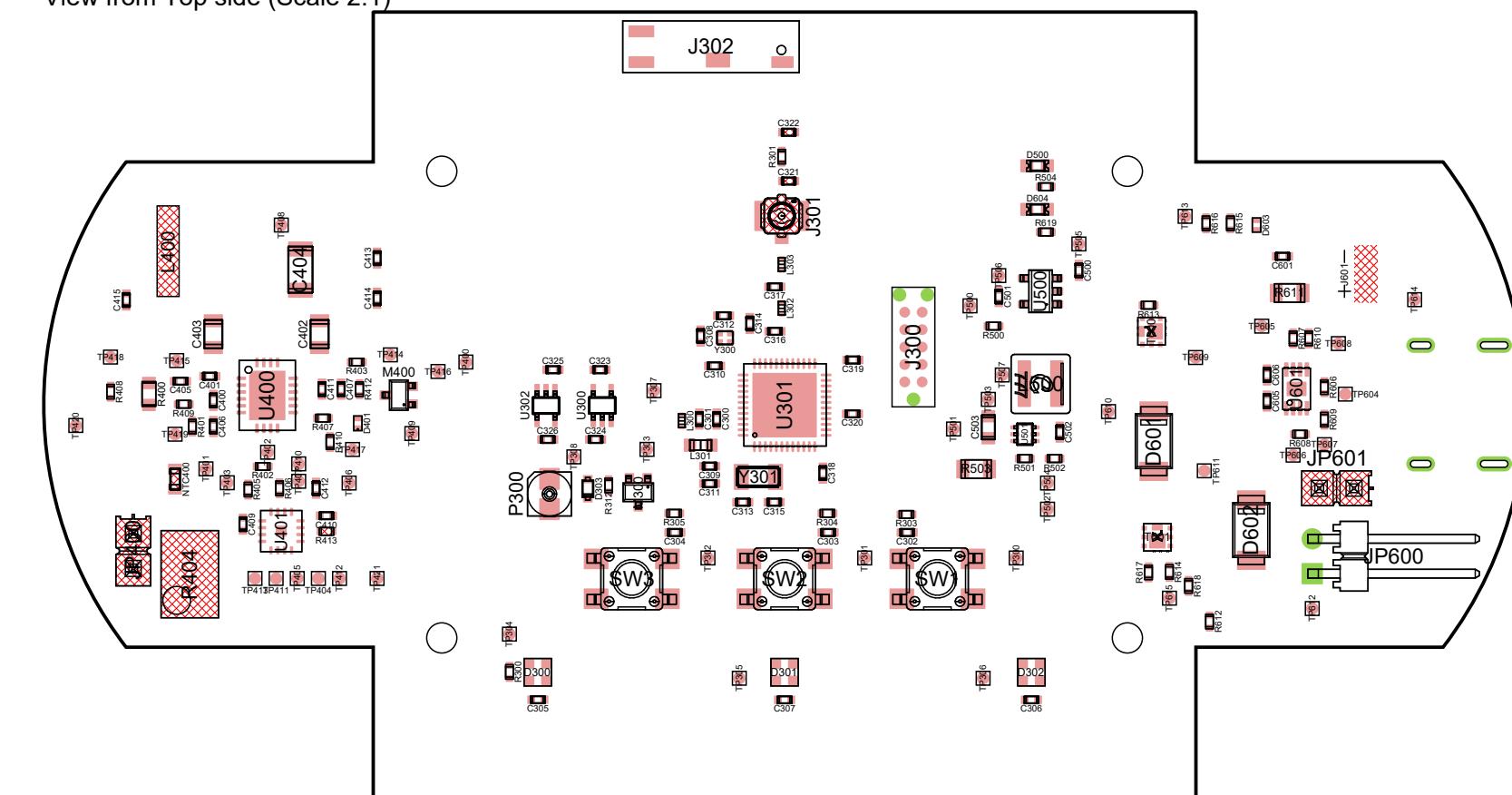
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# Assembly View:

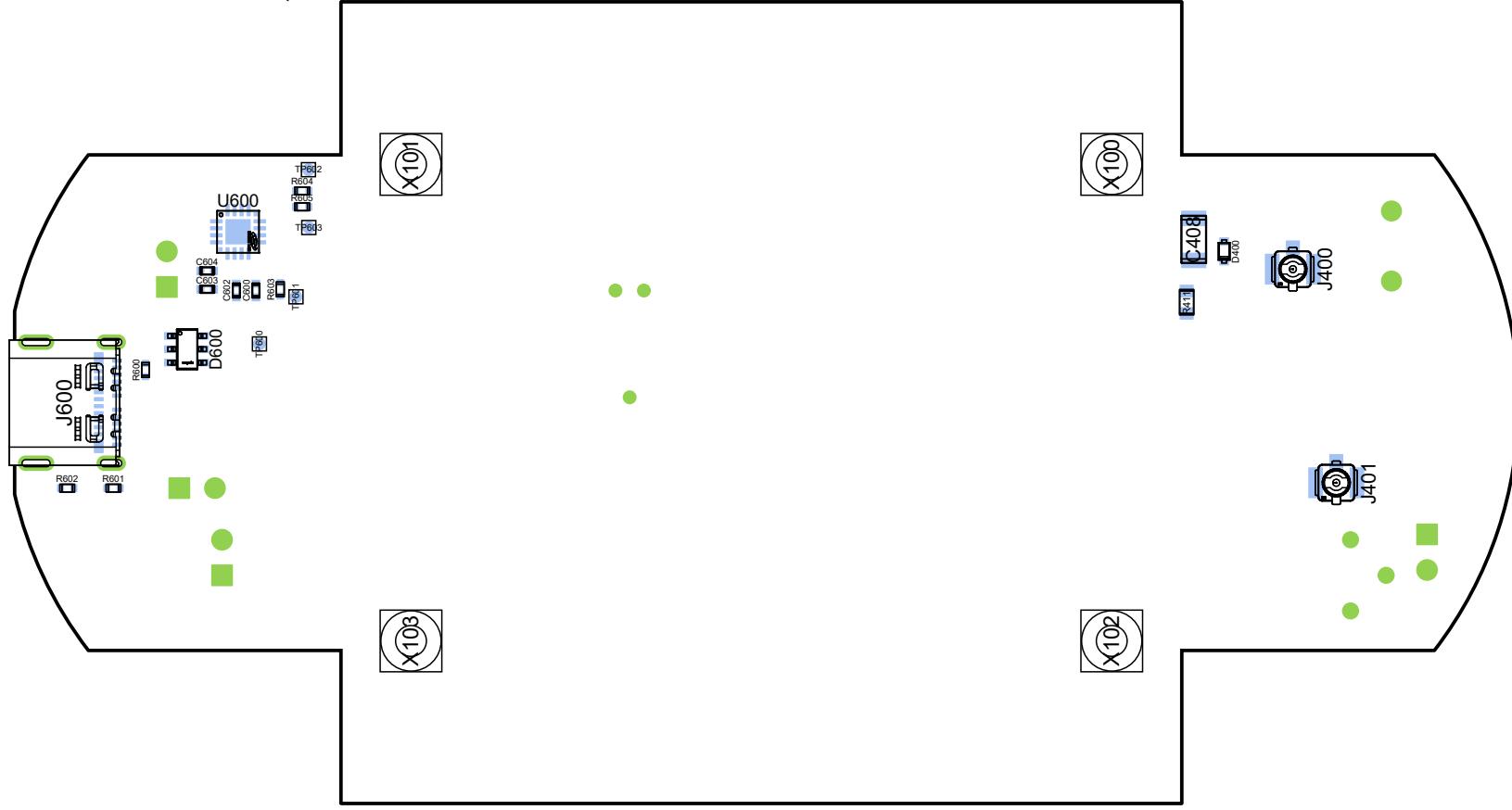
Notes:

12. DNP components are hatched over in the Assembly Views.

View from Top side (Scale 2:1)



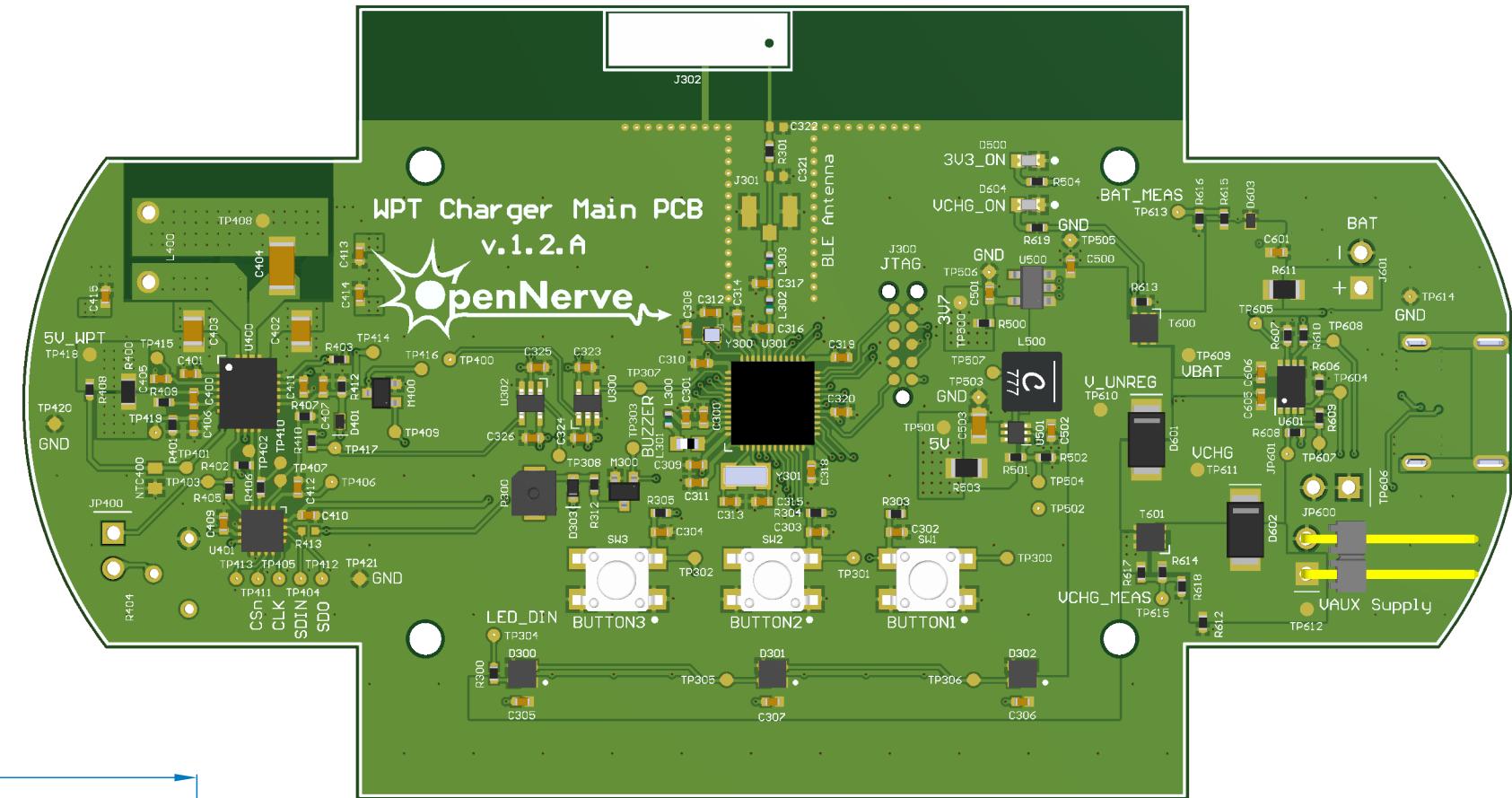
View from Bottom side (Scale 2:1)



	<b>FOCUS</b>	Project: WPTChargerMain.PrcPcb
Title:	Draftman	Ver: 1.2
Design by:	Mathias Ferreira	Date: 28/08/2024
Reviewed by:	Julian Evia	Date: 28/08/2024
Comments:		

# Dimensions

Realistic View



## Region View (Scale 2:1)

A technical drawing showing a rectangular base plate. The width of the plate is indicated by a blue arrow at the top right, labeled "59.99m". The height of the plate is indicated by a blue arrow on the left side, labeled "scale 2:1" above and "110.92mm" below. The entire plate is filled with a pattern of diagonal hatching.

A technical drawing showing a central rectangular panel with two semi-circular end caps. The central panel has a height of 35.36mm and a width of 100.00mm. Each end cap has a height of 46.27mm and a radius of 25.26mm. The entire assembly is 100.00mm wide.

 <b>FOCUS</b>	<b>Project:</b> WPTChargerMain.PrjPcb
<b>Title:</b> <b>Draftman</b>	<b>Ver:</b> 1.2
<b>Design by:</b> <b>Mathias Ferreira</b>	<b>Date:</b> <b>28/08/2024</b>
<b>Reviewed by:</b> <b>Julian Evia</b>	<b>Date:</b> <b>28/08/2024</b>
<b>Comments:</b>	

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# Stackup

## Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
1	Surface Material	Top Overlay	0.02mm	Solder Resist	Legend	GTO
	Copper	Top Solder	0.05mm		Solder Mask	GTS
		Top			Signal	GTL
	Prepreg		0.20mm	FR-4		Dielectric
2	Copper	GND	0.03mm		Signal	G1
	Core		0.97mm	FR-4		Dielectric
	Copper	Power	0.03mm		Signal	G2
	Prepreg		0.20mm	FR-4		Dielectric
3	Copper	Bottom	0.05mm		Signal	GBL
	Surface Material	Bottom Solder	0.02mm	Solder Resist	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

Total thickness: 1.57mm

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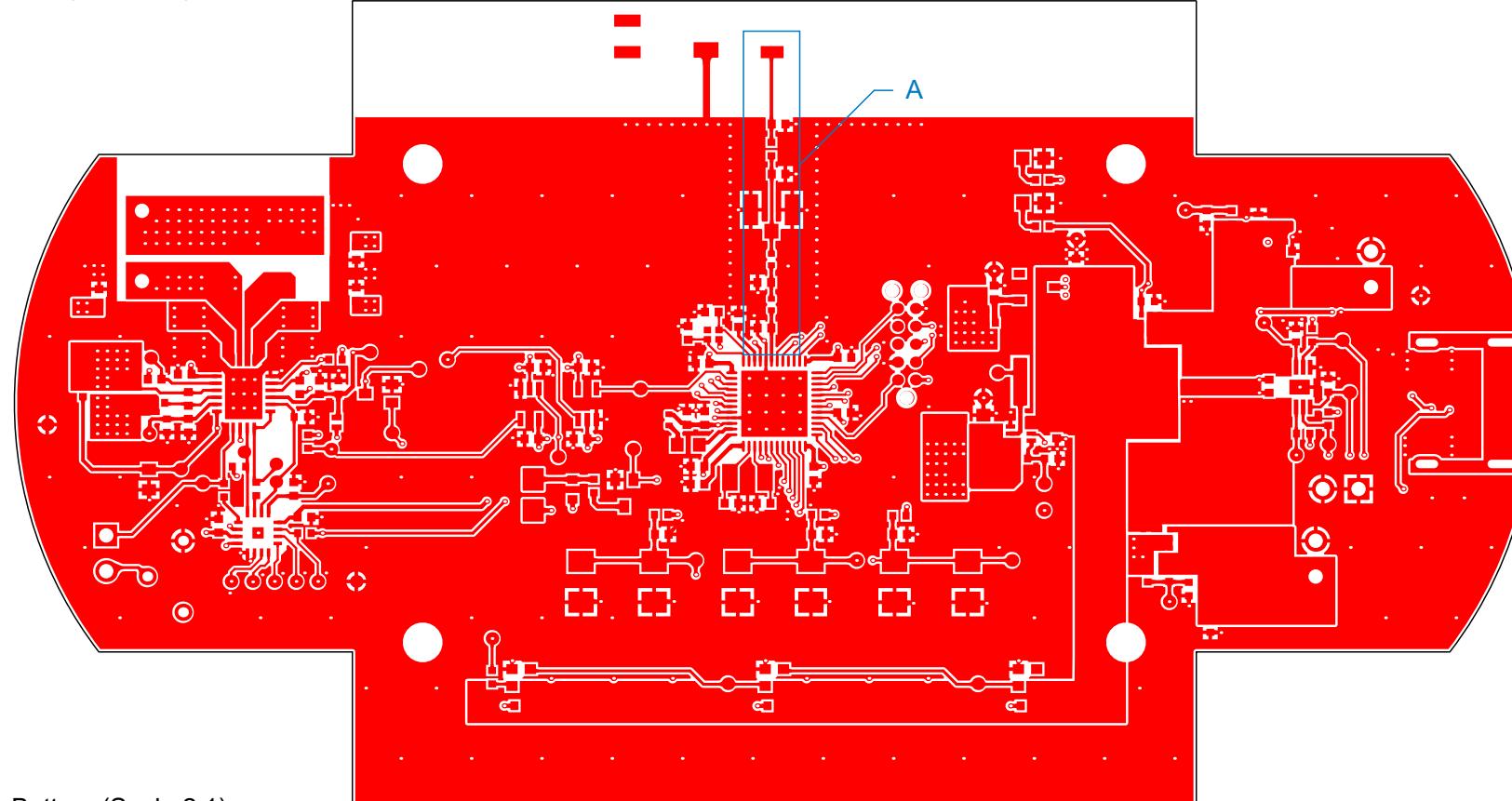
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# Impedance Control

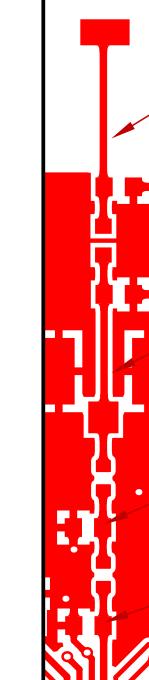
Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Gap	Reference layers	Substack	Clearance	Target Tolerance
2	Coated Coplanar Waveguide With Ground	50	50.00	Top	0.25mm	0.25mm		GND	Board Layer Stack	0.15mm	10%
3	Diff Coated Coplanar Waveguide With Ground	90	90.01	Bottom	0.20mm	0.20mm	0.15mm	Power	Board Layer Stack	0.15mm	10%

Top (Scale 2:1)



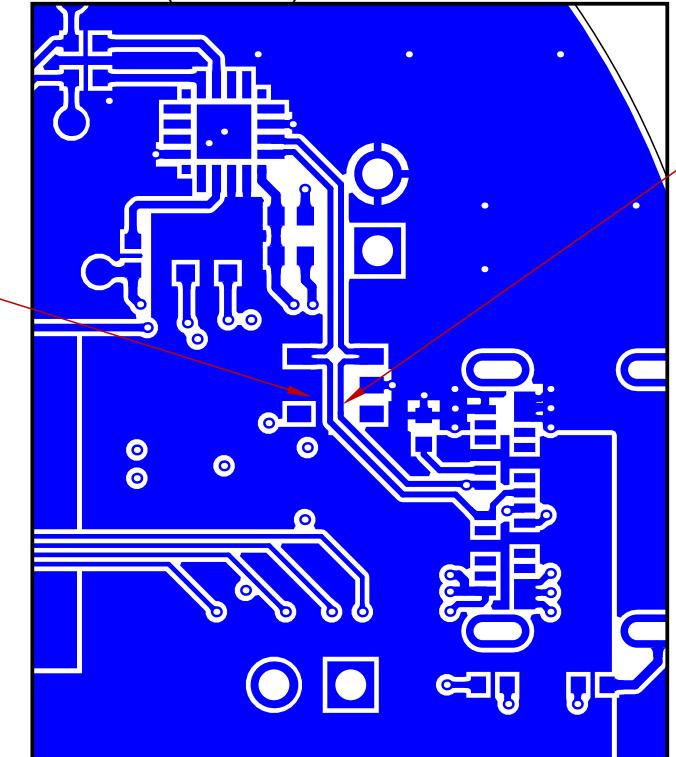
DETAIL A (Scale 4:1)



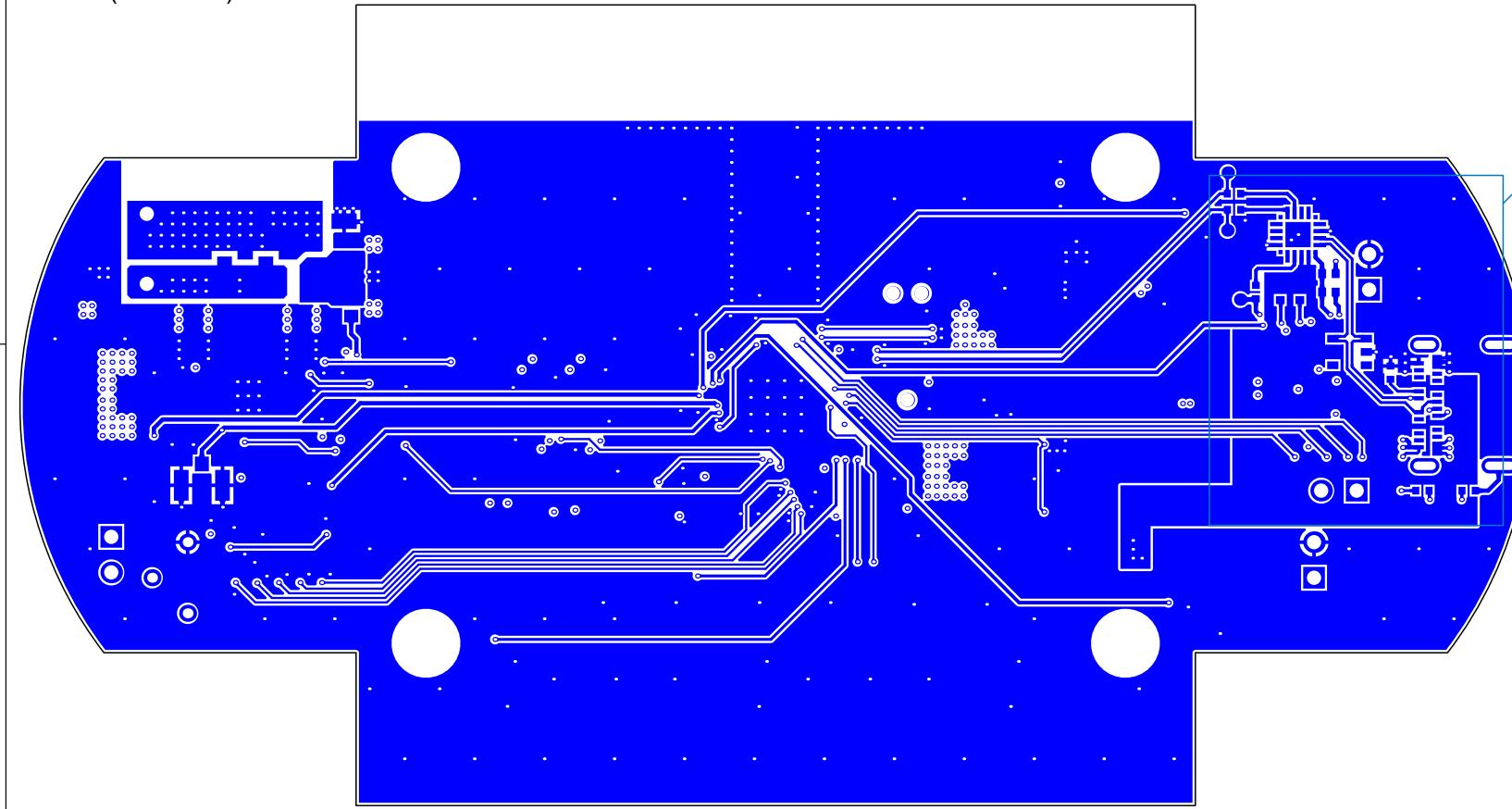
Controlled impedance nets for the Break Away

Net name	Impedance Id	Detail Reference	Note number
USB_P	3	B	6
USB_N	3	B	5
ANT MCU	2	A	1
NetC317_2	2	A	2
ANT+	2	A	3
ANT_PCB+	2	A	4

DETAIL B (Scale 4:1)



Bottom (Scale 2:1)



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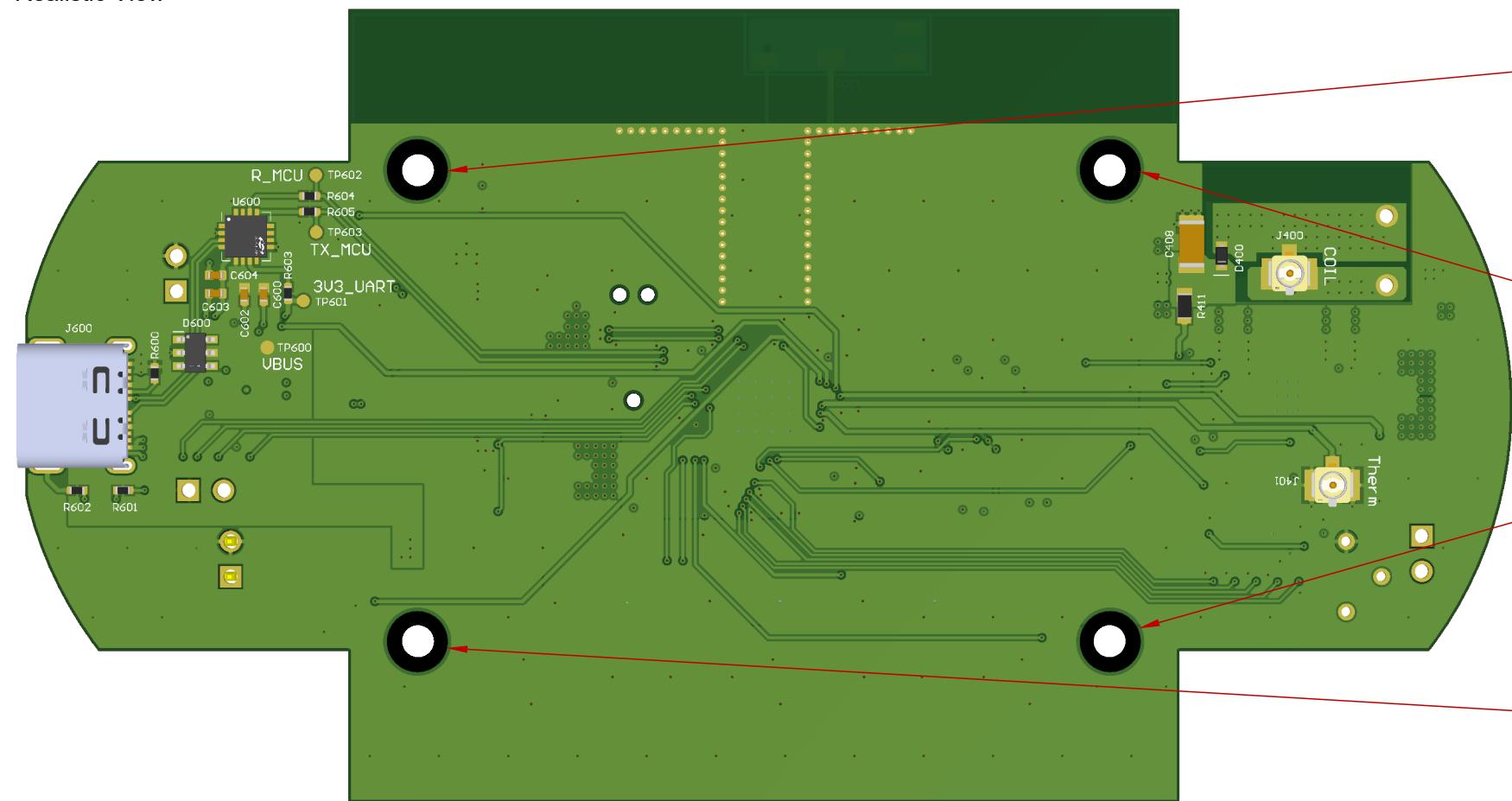
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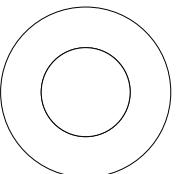
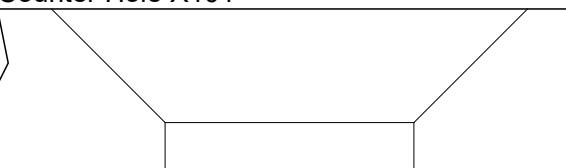
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# Chamfered holes

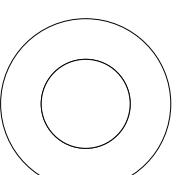
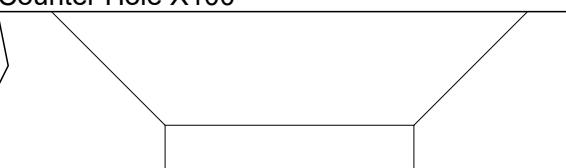
Realistic View



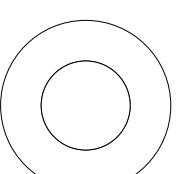
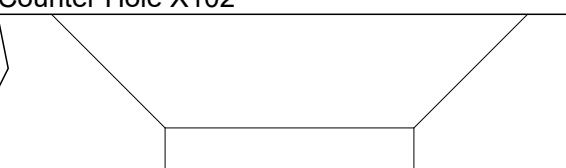
Counter Hole X101



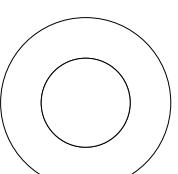
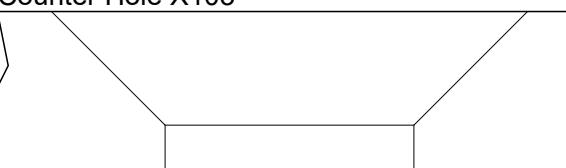
Counter Hole X100



Counter Hole X102

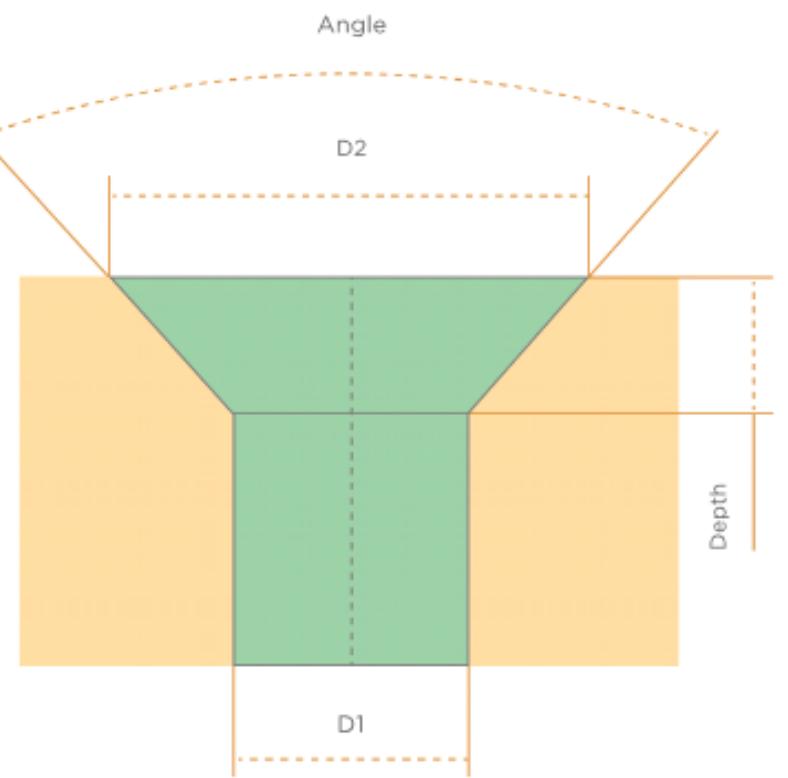


Counter Hole X103



Angle

Angle = 90°



D2 = 4.4mm

Depth = 1.05mm

D1 = 2.3mm