Impedance Measurement Strategy Document

This document outlines the actions required by the IPG firmware to implement impedance measurement.

Document Title: Impedance Measurement Strategy

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1. Circuit Overview and Signals

The stimulus stage generates a current pulse on any of the eight channels or the enclosure. The measurement circuit then acquires the voltage between the selected electrode pairs.

The stimulus generation is set by the pulse guard circuit and the DAC which controls the voltage control current source and it drives the current pulse to the electrodes or enclosure.

The impedance measurement circuit (Figure 1) consists of three stages:

- **Supply Control:** This circuit enables the 3V3 power rail, supplying power to the entire IMC.
- **Channel Selection:** This circuit selects the measurement nodes among the eight channels and the enclosure.
- **Amplification Circuits:** The selected nodes are fed into an amplification circuit, where a fully differential amplifier with a gain of 7.20 V/V amplifies the differential voltage between them. The outputs, IMP_INA and IMP_INB, connect to the microcontroller's ADC pins.

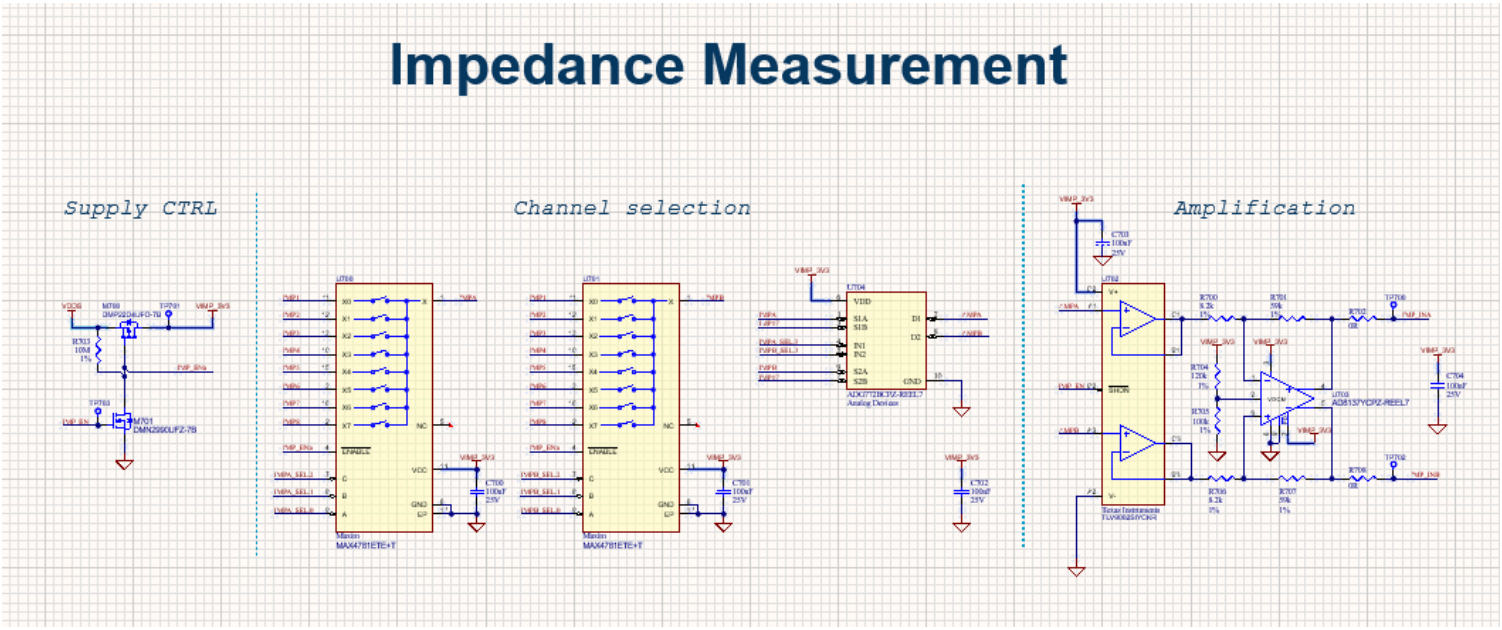

Figure 1. Impedance measurement circuit.

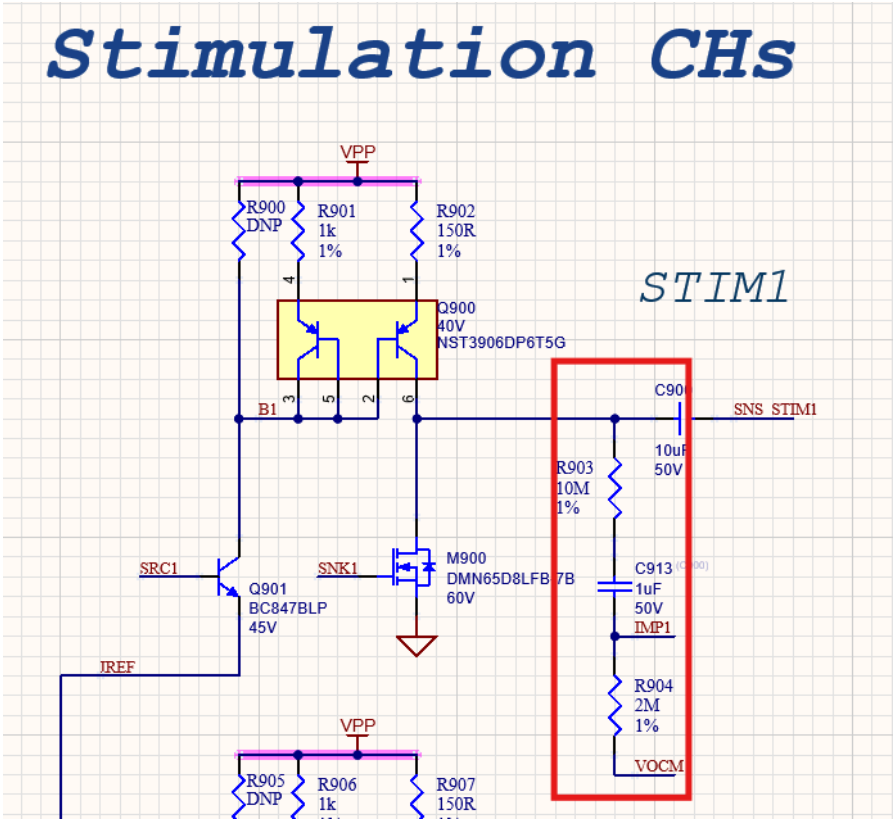

Figure 2. Input high pass filter circuit.

The signals involved in this process can be seen in the following table:

Label	Type	Description
Stimulus generation		
VPP	Power	Stimulation power rail.
VDDS		Digital power rail, used in the stimulus pulse generation.
STIM_EN	Input	Power up the current source.
I2C2		I2C bus used to control the DAC80502DRXT.
PG_START		Pulse Guard set.
AMPL_RSTn		
PH1_EN		
PH2_EN		
SRC[1..8]		Stimulation source channel selection.
SNK[1..8]		Stimulation sink channel selection.
SRC17		Eclosure as stimulation source selection.
SNK17		Eclosure as stimulation sink selection.
Voltage measurement		
VDDS	Power	Digital power rail, used to enable the measurement circuit and drive VIMP_3V3.
VIMP_3V3		3V3 power rail enabled by the IMP_EN signal. Used to supply the measurement circuit.
IMP_EN	Input	Impedance measurement enable.
IMPA_SEL		Node A of voltage amplification.
IMB_SEL		Node B of voltage amplification.
IMP_INA	Output	Node A of voltage measure.
IMP_INB		Node B of voltage measure.

Table 1: Signal description.

2. Stimulation Test Signal Characteristics

The stimulation signal used for impedance measurement must be biphasic, with a minimum pulse width of 0.5 ms and a maximum current of 1 mA.

3. Measurement Algorithm

The impedance measurement algorithm consists of three main steps: stimulation, measurement, and impedance calculation.

1. **Stimulation**:
   The load is stimulated using a biphasic signal with the specified pulse width, current amplitude, and other defined characteristics. This signal generates a current pulse of amplitude *Ip* through the load.
2. **Measurement**:
   The voltage across the load is obtained by measuring the absolute difference between the IMC outputs, IMP_INA and IMP_INB. This differential voltage signal is analyzed to identify relative maxima that correspond to positive stimulation pulses (excluding maxima caused by load-balancing pulses). The relevant maxima are then averaged over the number of pulses applied during stimulation, yielding the required measurement value *m*.
3. **Impedance Calculation**:
   Once the measurement *m* is obtained, it is adjusted to reflect the actual load voltage. This adjustment is performed by dividing *m* by the amplifier gain (7.2) and then multiplying the result by the attenuation factor of the high-pass filter (6). Finally, this adjusted voltage is divided by the stimulation current *Ip* to calculate the load impedance Z_{load}, as shown in Equation 1:

$$\left|Z_{load}\right| = \frac{m*6}{7.2 * Ip} \tag{1}$$

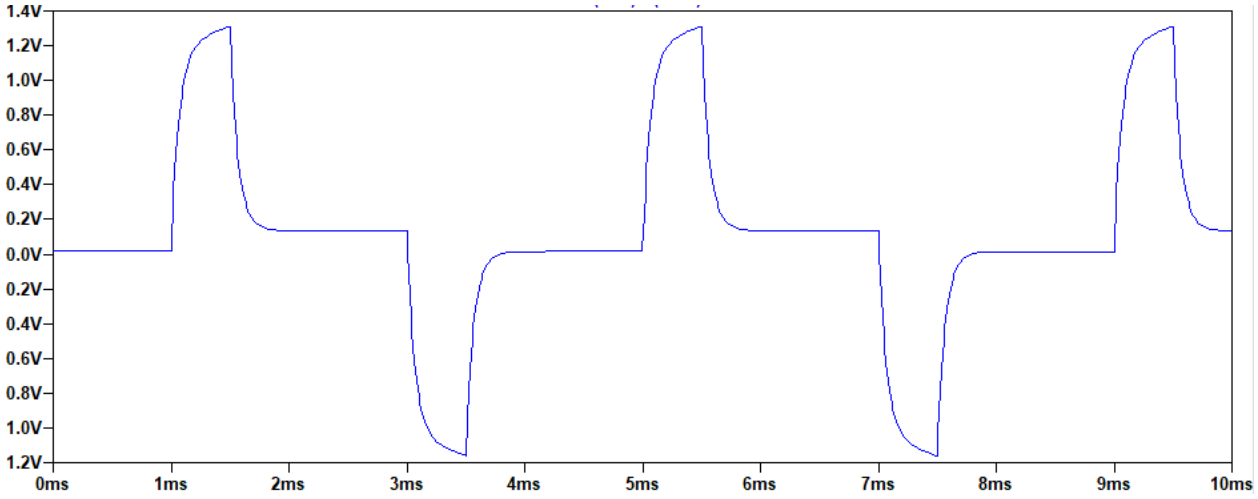

Figure 3. IMC output differential voltage (IMP_INA – IMP_INB)

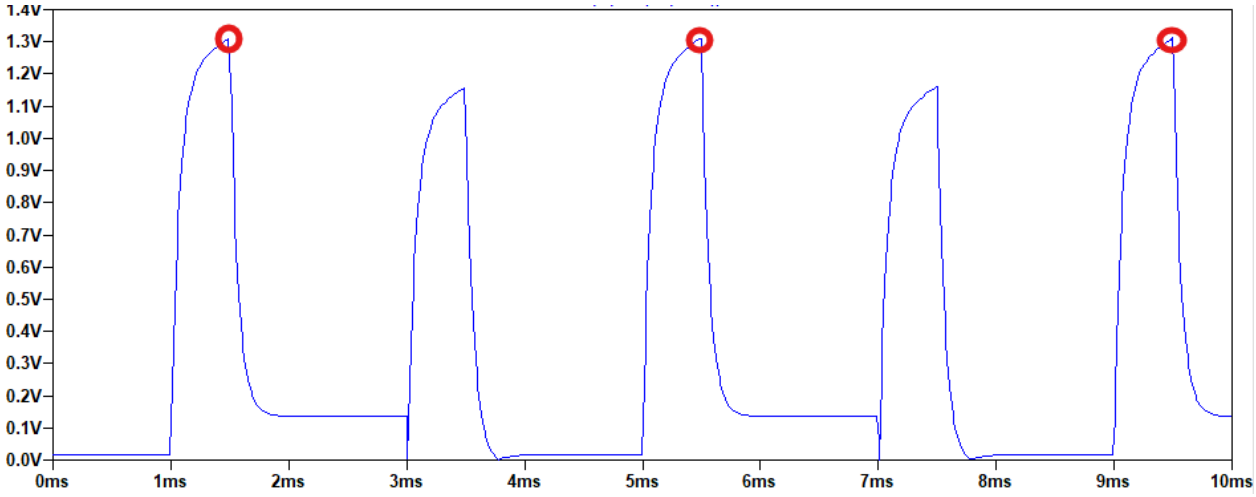

Figure 3. Absolut value of IMC output differential voltage (IMP_INA – IMP_INB) and its maximums.