Christoph Kassir

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Education

University of Toronto 2023 – 2027

B.A.Sc. Electrical and Computer Engineering *Toronto, ON*

- ECE295 Course **Award**, NSERC & 1st Year Research **Awards**, Dept & Faculty **Scholarships**, Dean's List (all)
- Courses: Analog Mixed-Signal, RF & Microwave, Digital, Converters, Semiconductors (Cadence, VNA, Sentaurus)

Experience

Hardware Engineer Intern Summer 2025 (4 months)

Myant Inc. & UofT Power Electronics Lab *Toronto, ON*

- Designed RTL control (SystemVerilog, Quartus) and PCB transformers (Altium, PLECS) for **APEC2025**.
- Co-designed 4-channel clinical heater PCB (Altium): USB-C PD, DC-DC, antenna matching, OV/OC protection.
- Co-designed neural-diagnoser PCB (Altium): AC-DC, DC-DC, digital delay circuits, OV/OC protection.
- Wrote Zephyr-RTOS BLE and PWM (nRF-SDK, C, Linux, Docker, Git). **1st major update since 2016**.

ML/AI Research Intern Contract 2025 (4 months)

Department of National Defense *Toronto, ON*

- Wrote Hidden-Markov-tuned transformers (PyTorch, Simulink): explainable-AI **VIEWS25 contract**.
- Wrote computer vision pipelines (OpenCV, Python): turbulent drone detection **CUAS25 challenge**.

Hardware Engineer Intern Summer 2024 (4 months)

T.R. Heart Research Center *Toronto, ON*

- Wrote DMA and interrupts (STM32CubeIDE, C) to **5× speed-up a smart ring**'s bare-metal SPI driver.
- Designed 2x breakout PCBs (Altium) for sensor ICs, debugged communications (Logic Analyzer).
- Wrote a genetic algorithm to **fully automate** DSP filter tuning (MATLAB) for sensor readings.

ML/AI Research Intern Summer 2023 (4 months)

P.M. Cancer Research Center *Toronto, ON*

- Wrote machine/deep learning models to validate imaging trials (TensorFlow, Sklearn, Git): **93-98% accuracy**.
- Wrote an AI contouring tool (OpenCV, Python, UNIX, Bash, Docker) to profile optic fibers: **89-99% accuracy**.

Projects

Zspice, the High-Performance Compute Software for CMOS Design

- Currently: Writing multi-threaded, custom-templated code (modern C++, ARM assembly) for the below.
- Done: Pseudo-code for netlisting, SPICE simulation solver, and GUI circuit placement, and device characteristics.
- Prep: *Analog IC Design, Verification, Layout* (Cadence Virtuoso) and *Analog Modeling with Verilog-A* [in progress].

FPGA: Digital Signal Processor Unit

- Fully-pipelined 8-point FFT DSP unit targeted for ASIC synthesis (Xilinx Vivado, SystemVerilog).
- Wrote a 3-case testbench and containerized solution (Bash, Docker) for Vivado installation on Apple Silicon.

PCB: Radio Modulator (ECE295 - Winner)

- Co-designed front-end PCB (Altium): active filters (LTSpice), differential routing. PyVisa test automation.
- Bare-metal programmed the PCB's ATMega (MPLab, C) to the extreme limit of producing 4 kHz+ signals.

Embedded: Wireless Audio Communications (ECE243)

- Programmed a custom 10 Hz peer-to-peer protocol on a soft processor (RISCV Assembly, C). 1000+ lines.
- Features a double-buffered VGA graphics GUI and hardware/software interrupts.

FPGA: Flappy Bird (ECE241)

- Wrote RTL code and testbenches (Verilog, TCL, Quartus, Modelsim) to run the game. 1500+ lines.
- Features memory IPs and FSMs for VGA graphics, speaker audio, PS2 input, and game logic.

PCB: High-Voltage EV Testing (UofT Formula SAE Team)

- Co-designed, soldered PCB (Altium) that validates the EV's insulation monitoring device. High-voltage testing.