7

FET Biasing

CHAPTER OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.

7.1 INTRODUCTION

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $V_{BE} = 0.7\text{ V}$, $I_C = \beta I_B$, and $I_C \cong I_E$. The link between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

Another distinct difference between the analysis of BJT and FET transistors is that:

The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\ \text{A} \tag{7.1}$$

and

$$I_D = I_S \tag{7.2}$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{7.3}$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \tag{7.4}$$

It is particularly important to realize that all of the equations above are for the *field-effect transistor only*! They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.

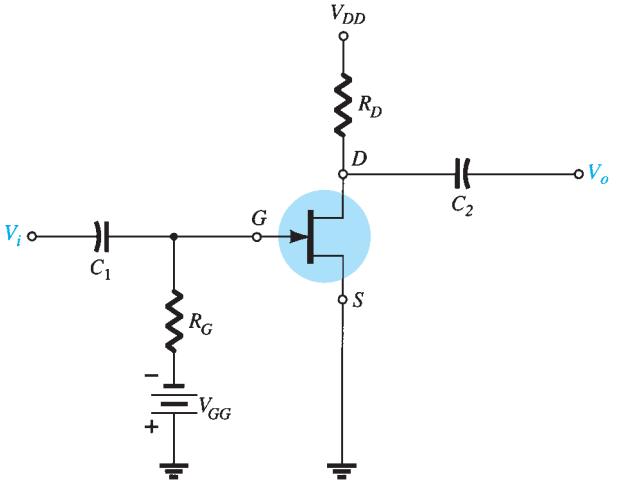


FIG. 7.1
Fixed-bias configuration.

The configuration of Fig. 7.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,

$$I_G \cong 0\text{ A}$$

and

$$V_{R_G} = I_G R_G = (0\text{ A})R_G = 0\text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

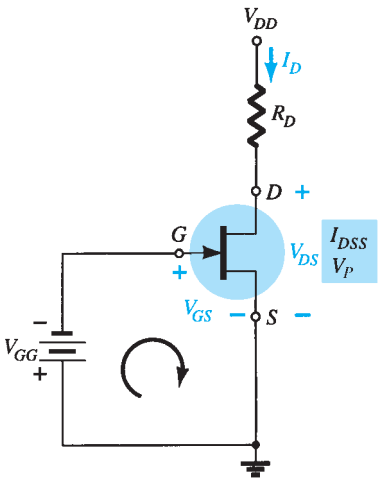


FIG. 7.2
Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \qquad \textbf{(7.5)}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 7.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

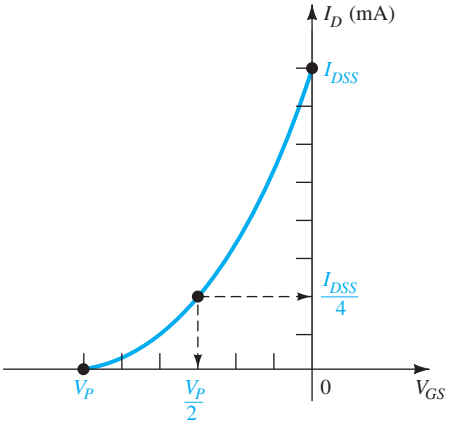


FIG. 7.3
Plotting Shockley's equation.

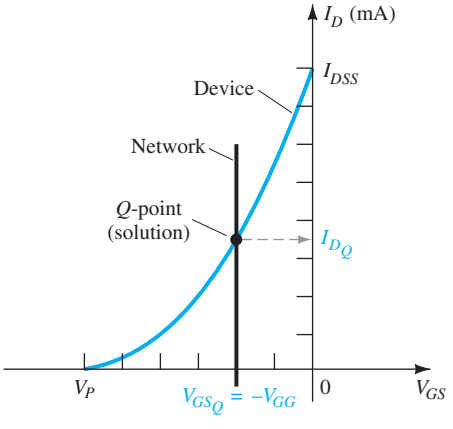


FIG. 7.4
Finding the solution for the fixed-bias configuration.

In Fig. 7.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.* The subscript Q will be applied to the drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 7.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis. It is important to realize

that once the network of Fig. 7.1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 7.5 are the quiescent values defined by Fig. 7.4.

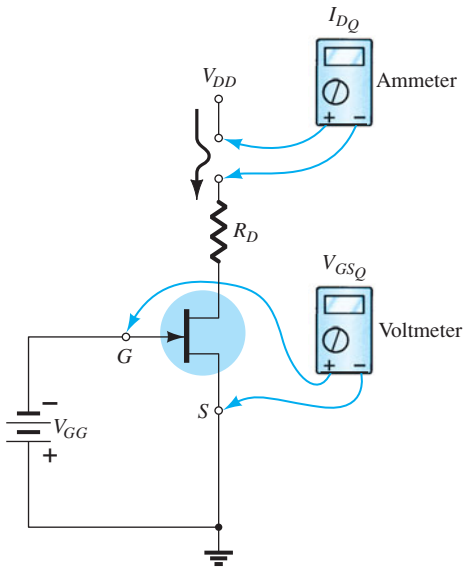


FIG. 7.5
Measuring the quiescent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{7.6}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$\boxed{V_S = 0\text{ V}} \tag{7.7}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V}$$

and

$$\boxed{V_D = V_{DS}} \tag{7.8}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V}$$

and

$$\boxed{V_G = V_{GS}} \tag{7.9}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

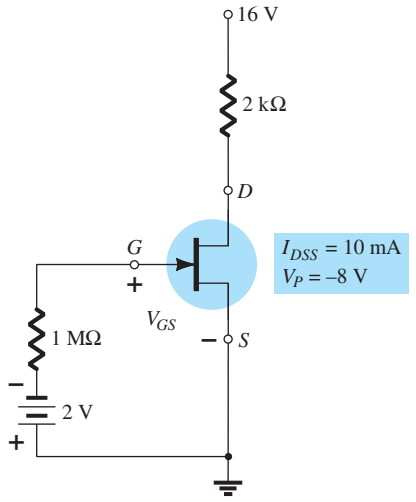


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without

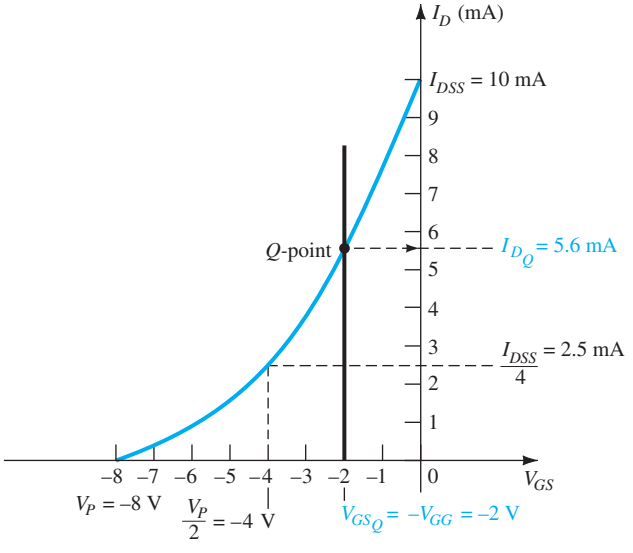


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 7.8.

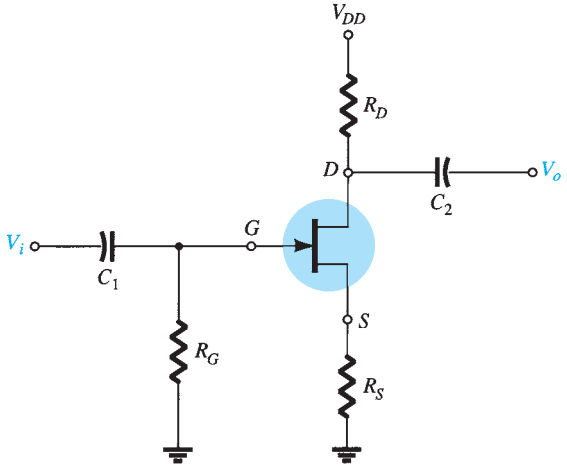


FIG. 7.8
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 7.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \qquad \textbf{(7.10)}$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

Equation (7.10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, I_D and V_{GS}, permitting either a mathematical or a graphical solution.

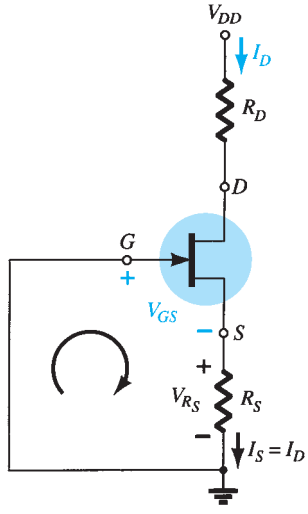


FIG. 7.9
DC analysis of the self-bias configuration.

A mathematical solution could be obtained simply by substituting Eq. (7.10) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 7.10. Since Eq. (7.10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0$ A since it results in $V_{GS} = -I_D R_S = (0\text{ A})R_S = 0$ V. For Eq. (7.10), therefore, one point on the straight line is defined by $I_D = 0$ A and $V_{GS} = 0$ V, as appearing on Fig. 7.10.

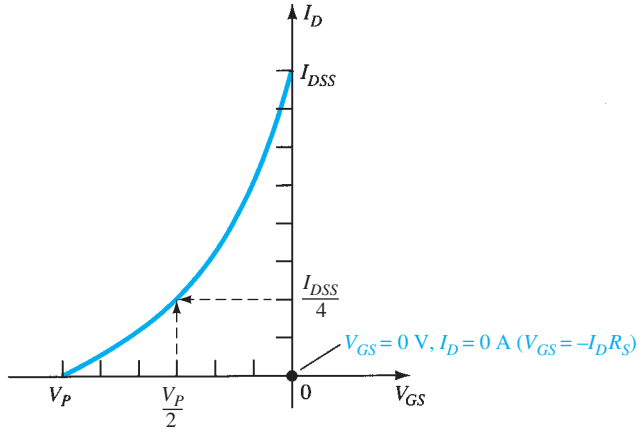


FIG. 7.10
Defining a point on the self-bias line.

The second point for Eq. (7.10) requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined using Eq. (7.10). The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit the drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

Then

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 7.11. The straight line as defined by Eq. (7.10) is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

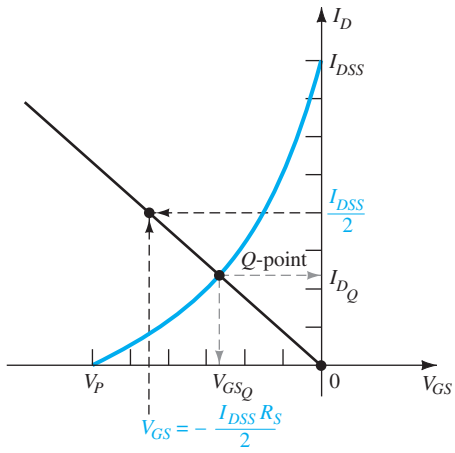


FIG. 7.11
Sketching the self-bias line.

but
$$I_D = I_S$$

and
$$V_{DS} = V_{DD} - I_D(R_S + R_D) \tag{7.11}$$

In addition,
$$V_S = I_D R_S \tag{7.12}$$
$$V_G = 0\text{ V} \tag{7.13}$$

and
$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D} \tag{7.14}$$

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

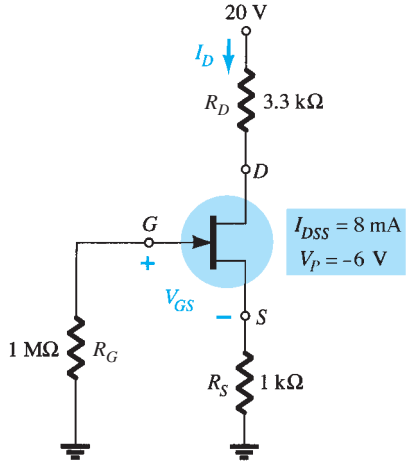


FIG. 7.12
Example 7.2.

Solution:

a. The gate-to-source voltage is determined by
$$V_{GS} = -I_D R_S$$
Choosing $I_D = 4$ mA, we obtain
$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$
The result is the plot of Fig. 7.13 as defined by the network.

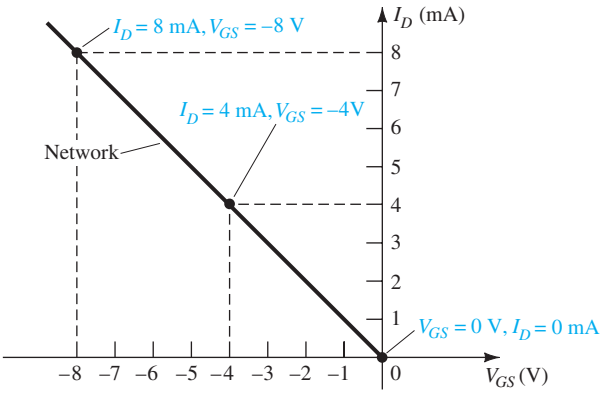


FIG. 7.13
Sketching the self-bias line for the network of Fig. 7.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (7.10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D determined graphically.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8$ mA$/4 = 2$ mA, and the plot of Fig. 7.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 7.13 on the device characteristics of Fig. 7.14 and finding the point of intersection of the two as indicated on Fig. 7.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6\ V}$$

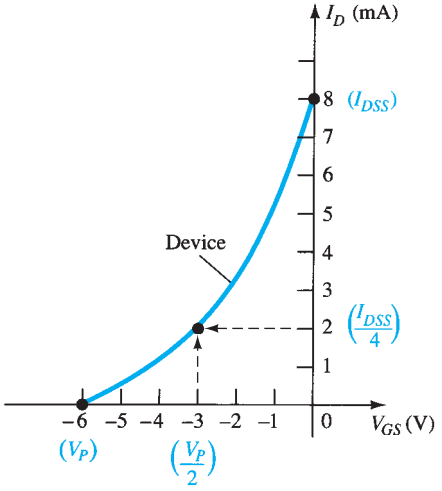


FIG. 7.14
Sketching the device characteristics for the JFET of Fig. 7.12.

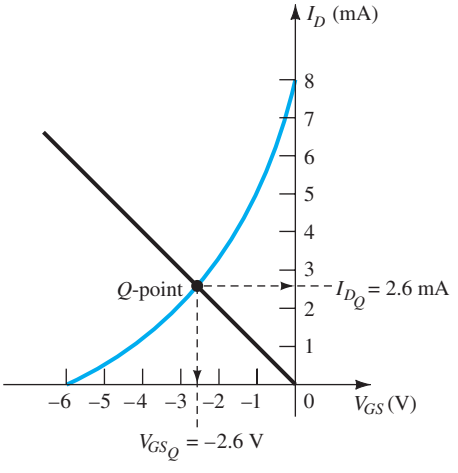


FIG. 7.15
Determining the Q-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. Eq. (7.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$$

$$= 20\text{ V} - 11.18\text{ V}$$

$$= \mathbf{8.82\ V}$$

d. Eq. (7.12): $V_S = I_D R_S$
$= (2.6\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.6\text{ V}}$

e. Eq. (7.13): $V_G = \mathbf{0\text{ V}}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\text{ V}}$
or $V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\text{ V}}$

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\ \Omega$.
b. $R_S = 10\text{ k}\Omega$.

Solution: Both $R_S = 100\ \Omega$ and $R_S = 10\text{ k}\Omega$ are plotted on Fig. 7.16.

a. For $R_S = 100\ \Omega$:

$$I_{D_Q} \cong \mathbf{6.4\text{ mA}}$$

and from Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\text{ V}}$$

b. For $R_S = 10\text{ k}\Omega$

$$V_{GS_Q} \cong \mathbf{-4.6\text{ V}}$$

and from Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\text{ mA}}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

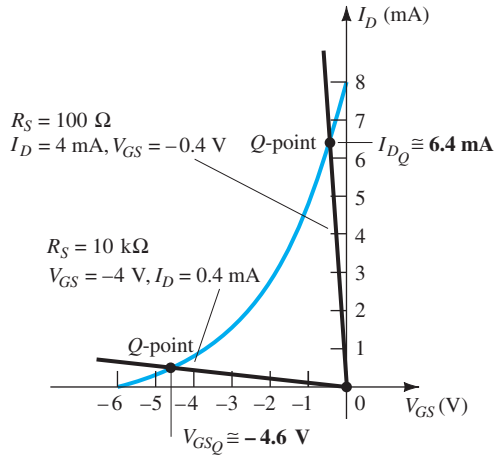


FIG. 7.16
Example 7.3.

7.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.17. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.

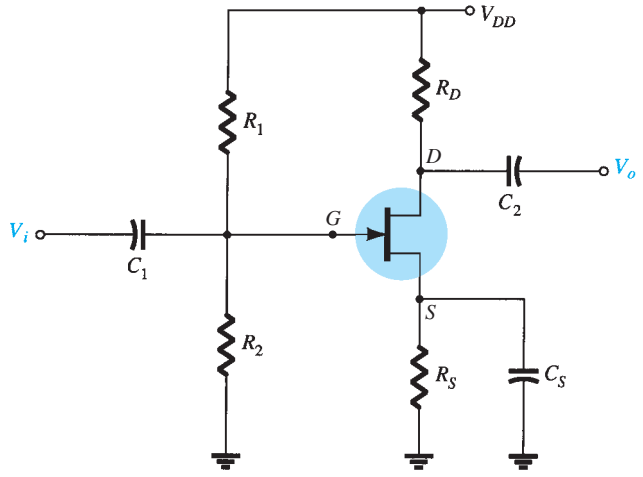


FIG. 7.17
Voltage-divider bias arrangement.

The network of Fig. 7.17 is redrawn as shown in Fig. 7.18 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent in Fig. 7.18b. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule and Fig. 7.18a as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{7.15}$$

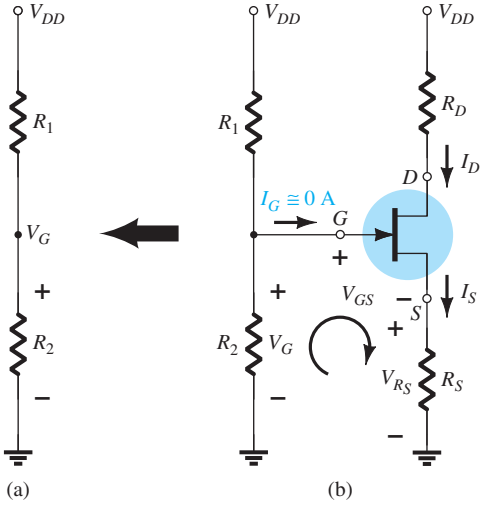


FIG. 7.18
Redrawn network of Fig. 7.17 for dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 7.18 results in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.19 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (7.16) and finding the resulting value of V_{GS} as follows:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= V_G - (0 \text{ mA}) R_S \end{aligned}$$

and

$$\boxed{V_{GS} = V_G|_{I_D = 0 \text{ mA}}} \tag{7.17}$$

The result specifies that whenever we plot Eq. (7.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 7.19.

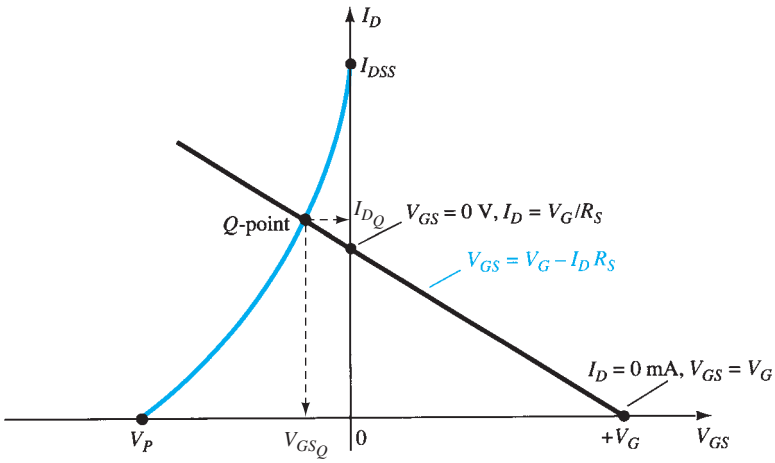


FIG. 7.19
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ 0 \text{ V} &= V_G - I_D R_S \end{aligned}$$

and

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0 \text{ V}}} \tag{7.18}$$

The result specifies that whenever we plot Eq. (7.16), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (7.18). This intersection also appears on Fig. 7.19.

The two points defined above permit the drawing of a straight line to represent Eq. (7.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as

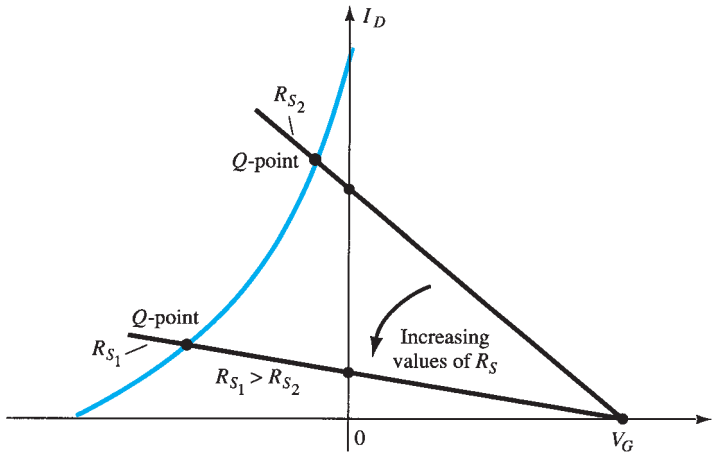


FIG. 7.20
Effect of R_S on the resulting Q-point.

shown in Fig. 7.20. It is fairly obvious from Fig. 7.20 that:

Increasing values of R_S result in lower quiescent values of I_D and declining values of V_{GS}.

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{7.19}$$

$$V_D = V_{DD} - I_D R_D \tag{7.20}$$

$$V_S = I_D R_S \tag{7.21}$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \tag{7.22}$$

EXAMPLE 7.4 Determine the following for the network of Fig. 7.21:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

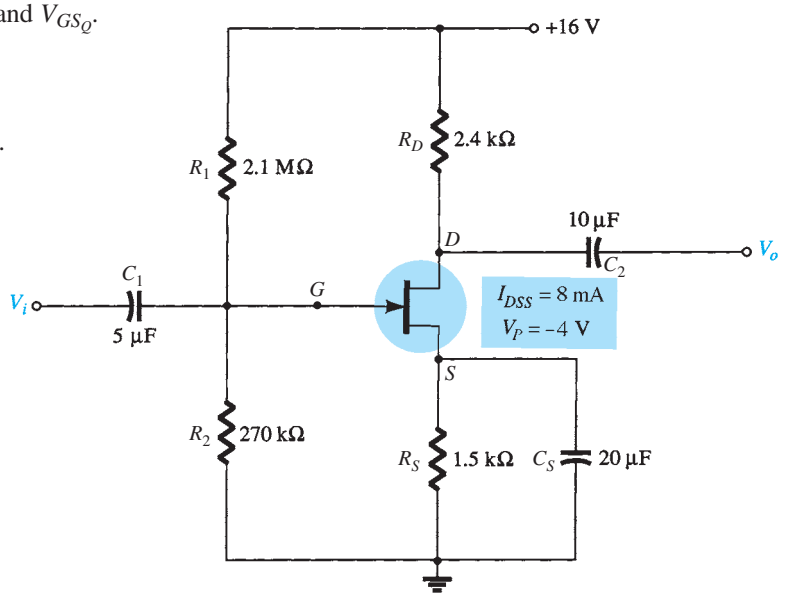


FIG. 7.21
Example 7.4.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

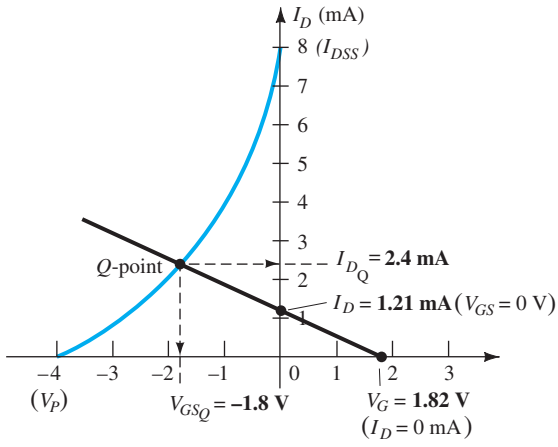


FIG. 7.22
Determining the Q-point for the network of Fig. 7.21.

When $I_D = 0\text{ mA}$,

$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0\text{ V}$,

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$

$= \mathbf{10.24\text{ V}}$

c. $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$

$= \mathbf{3.6\text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$

$= \mathbf{6.64\text{ V}}$

or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$

$= \mathbf{6.64\text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24\text{ V} - 1.82\text{ V}$$
$$= \mathbf{8.42\text{ V}}$$

7.5 COMMON-GATE CONFIGURATION

The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown in Fig. 7.23a. The network can also be drawn as shown in Fig. 7.23b.

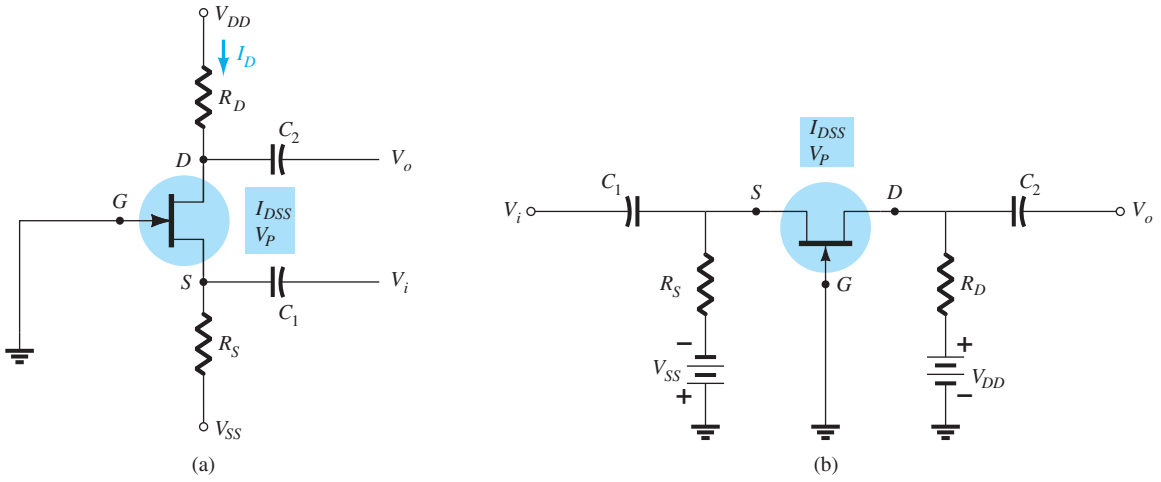


FIG. 7.23
Two versions of the common-gate configuration.

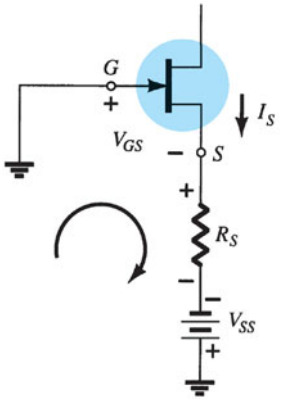


FIG. 7.24
Determining the network equation for the configuration of Fig. 7.23.

The network equation can be determined using Fig. 7.24.

Applying Kirchhoff's voltage law in the direction shown in Fig. 7.24 will result in

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

and

$$V_{GS} = V_{SS} - I_S R_S$$

but

$$I_S = I_D$$

so

$$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad \textbf{(7.23)}$$

Applying the condition $I_D = 0$ mA to Eq. 7.23 will result in

$$V_{GS} = V_{SS} - (0)R_S$$

and

$$\boxed{V_{GS} = V_{SS}|_{I_D=0\text{mA}}} \qquad \textbf{(7.24)}$$

Applying the condition $V_{GS} = 0$ V to Eq. 7.23 will result in

$$0 = V_{SS} - I_D R_S$$

and

$$\boxed{I_D = \left.\frac{V_{SS}}{R_S}\right|_{V_{GS}=0\text{ V}}} \qquad \textbf{(7.25)}$$

The resulting load-line appears in Fig. 7.25 intersecting the transfer curve for the JFET as shown in the figure.

The resulting intersection defines the operating current I_{D_Q} and voltage V_{D_Q} for the network as also indicated in the network.

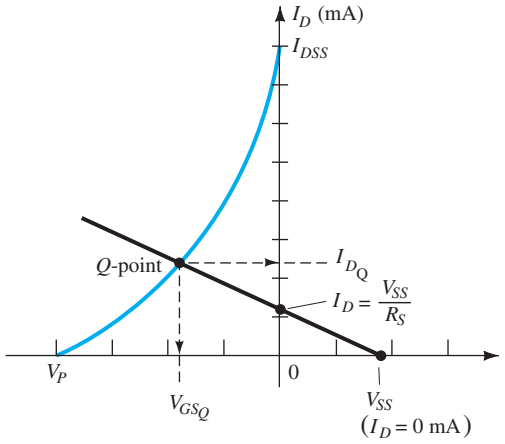


FIG. 7.25
Determining the Q-point for the network of Fig. 7.24.

Applying Kirchhoff's voltage law around the loop containing the two sources, the JFET and the resistors R_D and R_S in Fig. 7.23a and Fig. 7.23b will result in

$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting $I_S = I_D$ we have

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

so that

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \tag{7.26}$$

with

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{7.27}$$

and

$$\boxed{V_S = -V_{SS} + I_D R_S} \tag{7.28}$$

EXAMPLE 7.5 Determine the following for the common-gate configuration of Fig. 7.26:

a. V_{GS_Q}
b. I_{D_Q}
c. V_D
d. V_G
e. V_S
f. V_{DS}

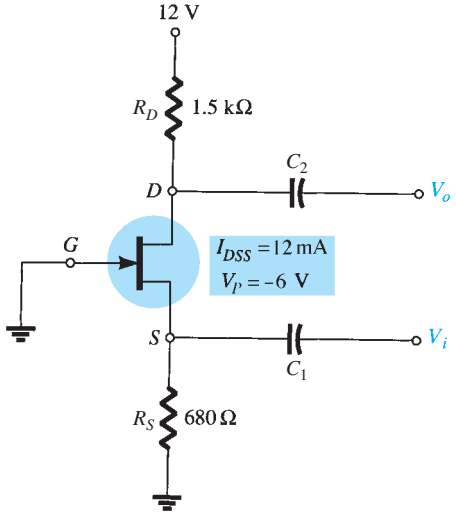


FIG. 7.26
Example 7.5.

Solution: Even though V_{SS} is not present in this common-gate configuration the equations derived above can still be used by simply substituting $V_{SS} = 0$ V into each equation in which it appears.

a. For the transfer characteristics Eq. 7.23 becomes

$$V_{GS} = 0 - I_D R_S$$

and

$$V_{GS} = -I_D R_S$$

For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing $I_D = 6$ mA and solving for V_{GS} will result in the following:

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 7.27.

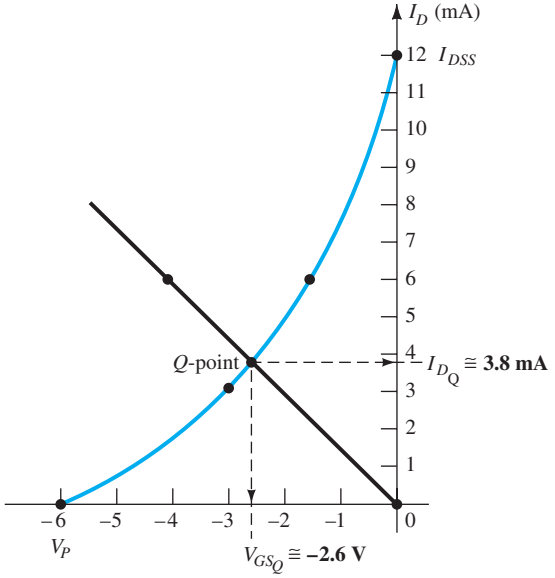


FIG. 7.27
Determining the Q-point for the network of Fig. 7.26.

The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}(\text{at } V_P/2)$$

and

$$V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = -1.8\text{ V}\ (\text{at } I_D = I_{DSS}/2)$$

The resulting solution is:

$$V_{GS_Q} \cong \mathbf{-2.6\ V}$$

b. From Fig. 7.27,

$$I_{D_Q} \cong \mathbf{3.8\ mA}$$

c. $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\ V}$

d. $V_G = \mathbf{0\ V}$

e. $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$
$= \mathbf{2.58\ V}$

f. $V_{DS} = V_D - V_S$
$= 6.3\text{ V} - 2.58\text{ V}$
$= \mathbf{3.72\ V}$

7.6 SPECIAL CASE: $V_{GS_Q} = 0$ V

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 7.28. Note that direct connection of the gate and source terminals to ground resulting in $V_{GS} = 0$ V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at $V_{GS_Q} = 0$ V as shown in Fig. 7.29.

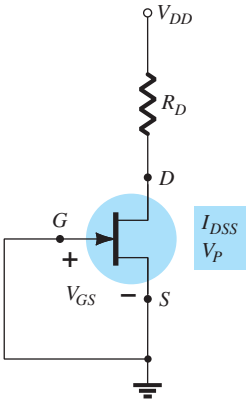


FIG. 7.28
Special case $V_{GS_Q} = 0$ V configuration.

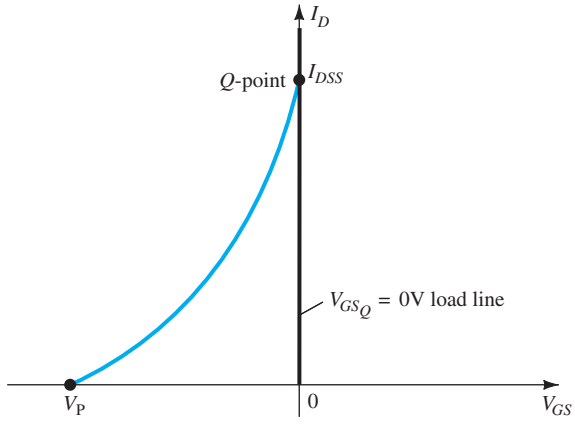


FIG. 7.29
Finding the Q-point for the network of Fig. 7.28.

Since the transfer curve of a JFET will cross the vertical axis at I_{DSS} the drain current for the network is set at that level.

Therefore,
$$I_{D_Q} = I_{DSS} \tag{7.29}$$

Applying Kirchhoff's voltage law:
$$V_{DD} - I_D R_D - V_{DS} = 0$$

and
$$V_{DS} = V_{DD} - I_D R_D \tag{7.30}$$

with
$$V_D = V_{DS} \tag{7.31}$$

and
$$V_S = 0\text{ V} \tag{7.32}$$

7.7 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

EXAMPLE 7.6 For the *n*-channel depletion-type MOSFET of Fig. 7.30, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

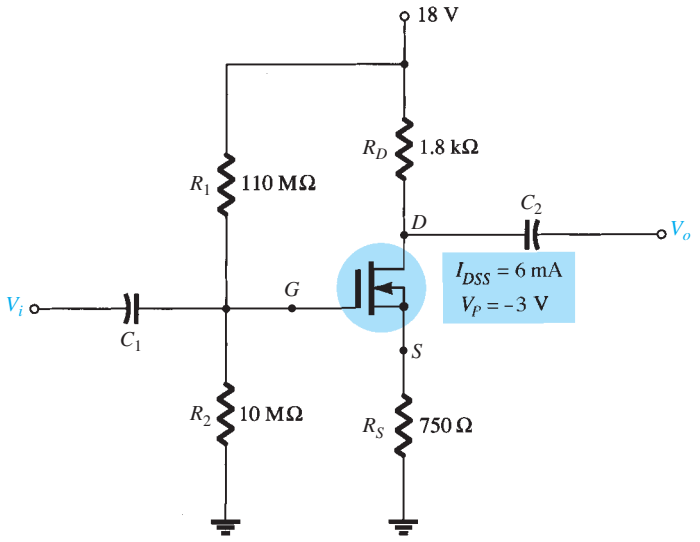


FIG. 7.30
Example 7.6.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}\,(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (7.16):}\quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

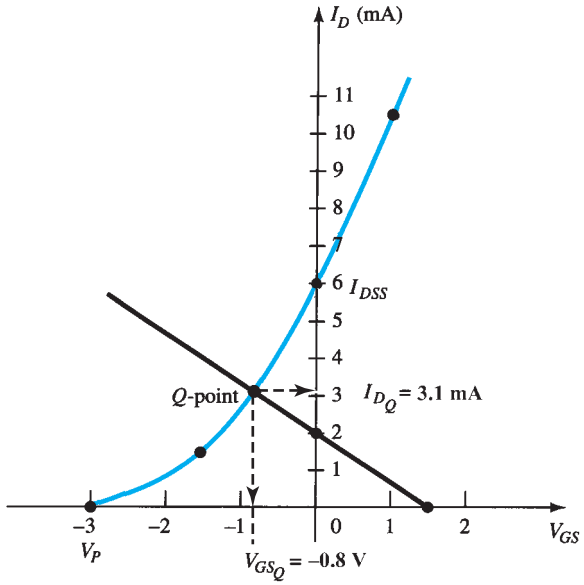


FIG. 7.31
Determining the Q-point for the network of Fig. 7.30.

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{750\ \Omega} = 2 \text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\ mA}$$
$$V_{GS_Q} = \mathbf{-0.8\ V}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18 \text{ V} - (3.1 \text{ mA})(1.8\ \text{k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\ V}$$

EXAMPLE 7.7 Repeat Example 7.6 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{150\ \Omega} = 10 \text{ mA}$$

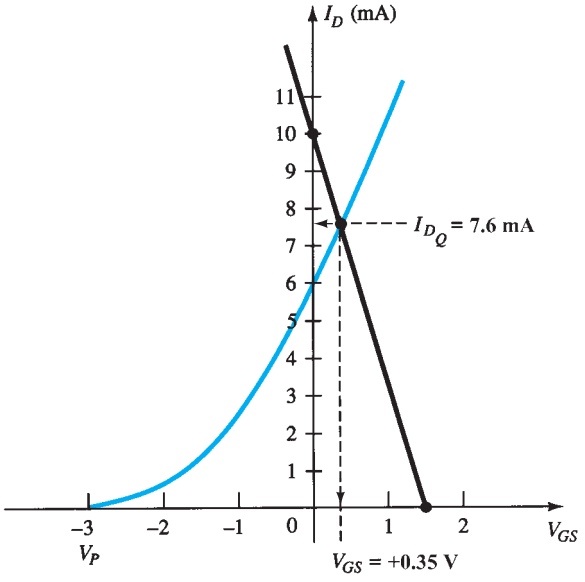


FIG. 7.32
Example 7.7.

The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\ mA}$$
$$V_{GS_Q} = \mathbf{+0.35\ V}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18 \text{ V} - (7.6 \text{ mA})(1.8\ \text{k}\Omega + 150\ \Omega)$$
$$= \mathbf{3.18\ V}$$

EXAMPLE 7.8 Determine the following for the network of Fig. 7.33:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

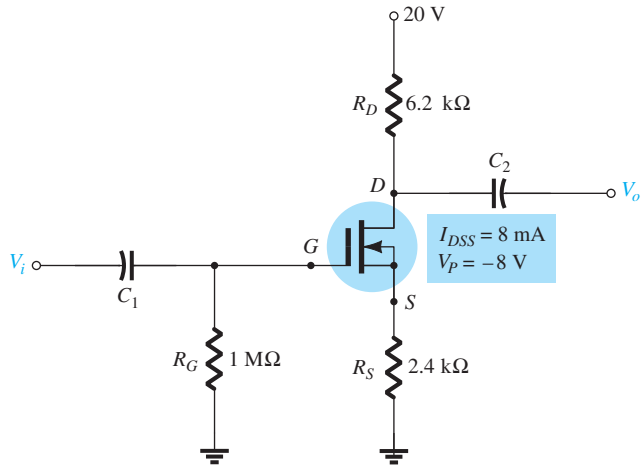


FIG. 7.33
Example 7.8.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$

$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$
$= \mathbf{9.46\text{ V}}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

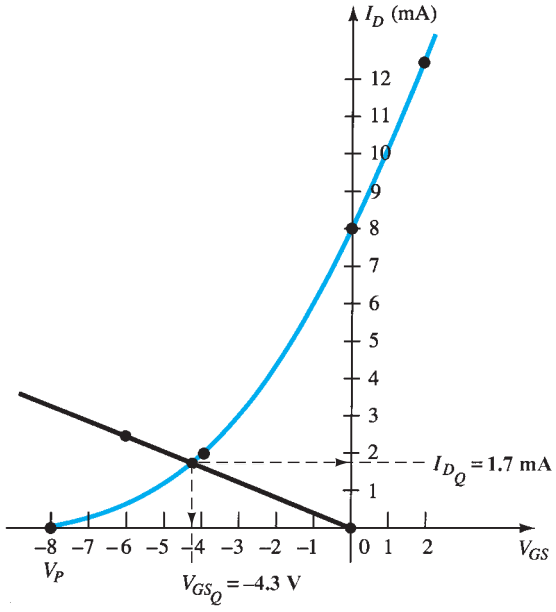


FIG. 7.34
Determining the Q-point for the network of Fig. 7.33.

EXAMPLE 7.9 Determine V_{DS} for the network of Fig. 7.35.

Solution: The direct connection between the gate and source terminals requires that

$$V_{GS} = 0 \text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0 \text{ V}}$$

and

$$I_{D_Q} = \mathbf{10 \text{ mA}}$$

There is therefore no need to draw the transfer curve, and

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega)$$
$$= 20 \text{ V} - 15 \text{ V}$$
$$= \mathbf{5 \text{ V}}$$

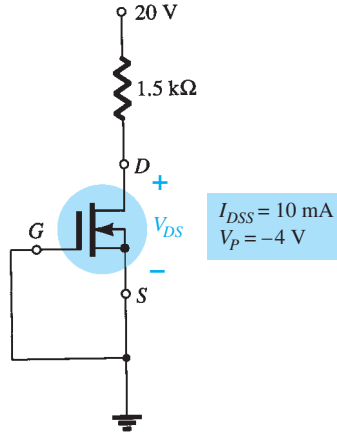


FIG. 7.35
Example 7.9.

7.8 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(\text{Th})}$, as shown in Fig. 7.36. For levels of V_{GS} greater than $V_{GS(\text{Th})}$, the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2 \qquad \textbf{(7.33)}$$

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(\text{on})}$) and its corresponding level of $V_{GS(\text{on})}$, two points are defined immediately as shown in Fig. 7.36. To complete the curve, the constant k of Eq. (7.33) must be determined from the specification sheet data by substituting into Eq. (7.33) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

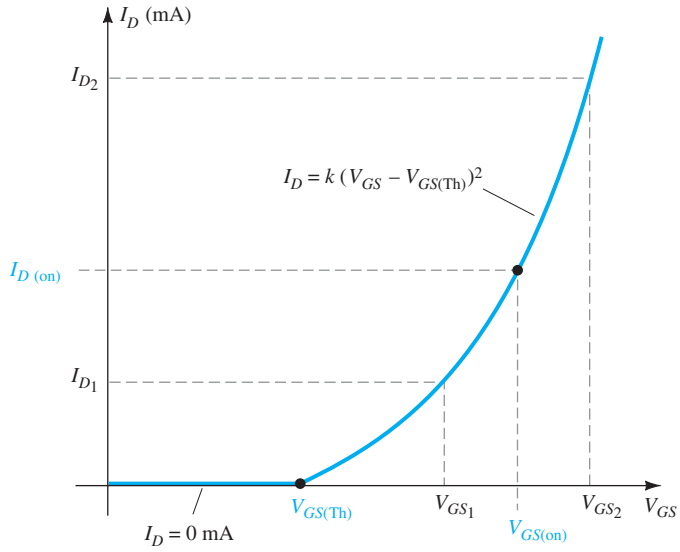


FIG. 7.36
Transfer characteristics of an n-channel enhancement-type MOSFET.

and
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2} \tag{7.34}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(Th)}$ and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ will provide a sufficient number of points to plot Eq. (7.33) (note I_{D_1} and I_{D_2} on Fig. 7.36).

Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 7.37. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA, $V_{R_G} = 0$ V and the dc equivalent network appears as shown in Fig. 7.38.

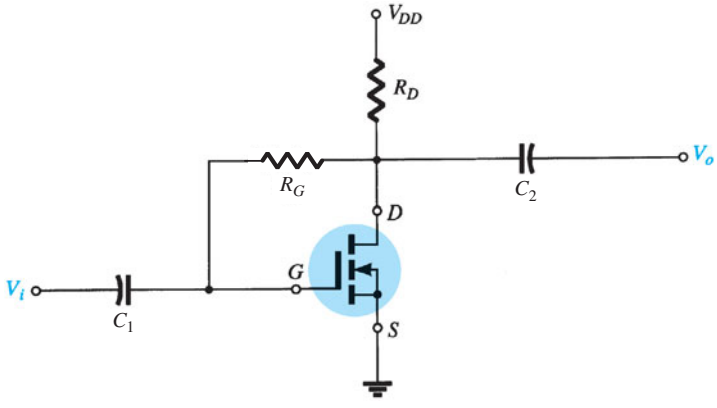


FIG. 7.37
Feedback biasing arrangement.

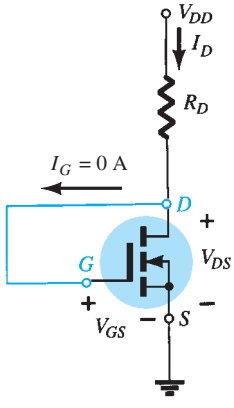


FIG. 7.38
DC equivalent of the network of Fig. 7.37.

A direct connection now exists between drain and gate, resulting in
$$V_D = V_G$$
and
$$V_{DS} = V_{GS} \tag{7.35}$$

For the output circuit,
$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (7.27):

$$V_{GS} = V_{DD} - I_D R_D \tag{7.36}$$

The result is an equation that relates I_D to V_{GS}, permitting the plot of both on the same set of axes.

Since Eq. (7.36) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0$ mA into Eq. (7.36) gives

$$V_{GS} = V_{DD}|_{I_D = 0\text{ mA}} \tag{7.37}$$

Substituting $V_{GS} = 0$ V into Eq. (7.36), we have

$$I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\text{ V}} \tag{7.38}$$

The plots defined by Eqs. (7.33) and (7.36) appear in Fig. 7.39 with the resulting operating point.

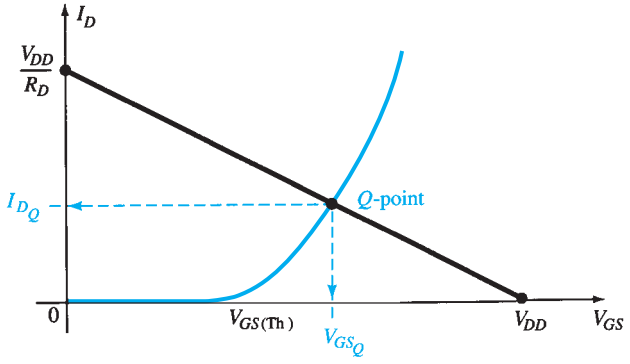


FIG. 7.39
Determining the Q-point for the network of Fig. 7.37.

EXAMPLE 7.10 Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 7.40.

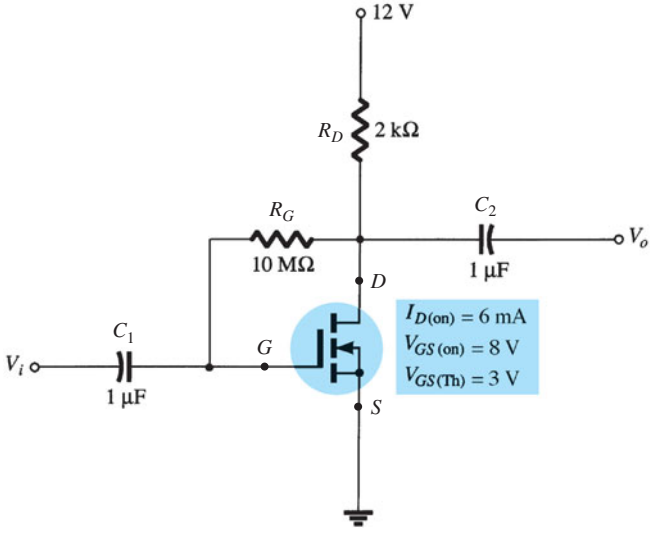


FIG. 7.40
Example 7.10.

Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. 7.41. Solving for k, we obtain

$$\text{Eq. (7.34):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\,A/V^2}$$

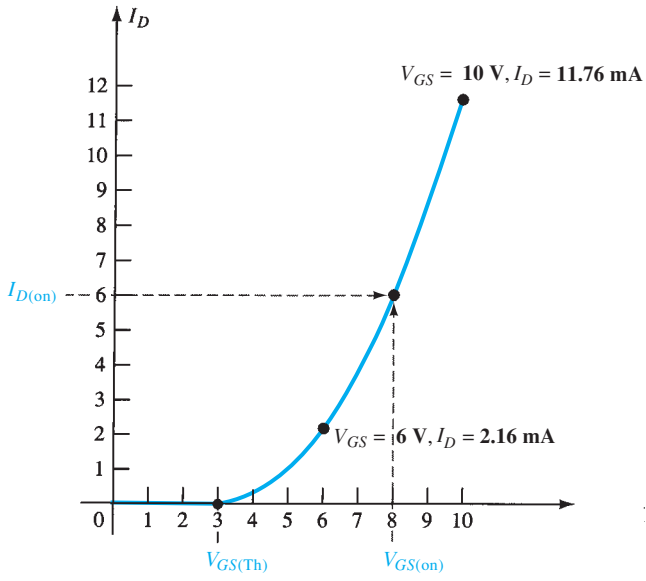


FIG. 7.41
Plotting the transfer curve for the MOSFET of Fig. 7.40.

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\text{ mA}$$

as shown on Fig. 7.41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76\text{ mA}$$

as also appearing on Fig. 7.41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.41.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$

$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

$$\text{Eq. (7.37):} \quad V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$

$$\text{Eq. (7.38):} \quad I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 7.42.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

and

$$V_{GS_Q} = 6.4\text{ V}$$

with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

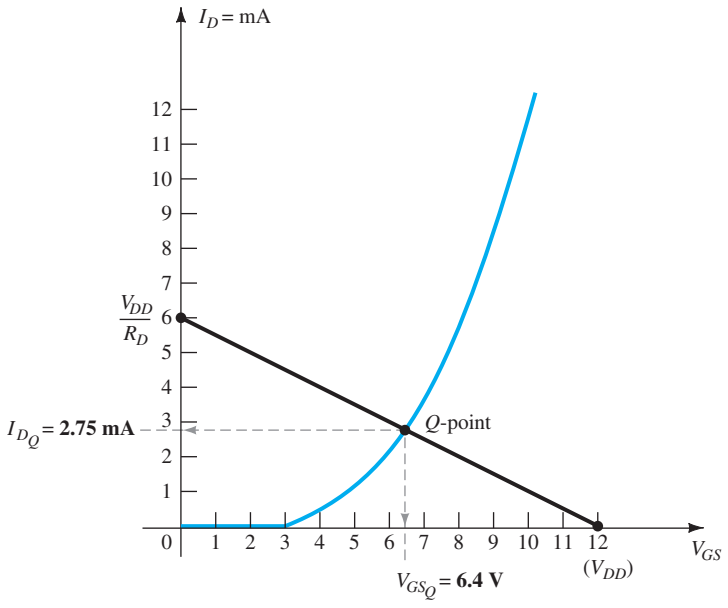


FIG. 7.42
Determining the Q-point for the network of Fig. 7.40.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.43. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{7.39}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$V_{GS} = V_G - I_D R_S \tag{7.40}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \tag{7.41}$$

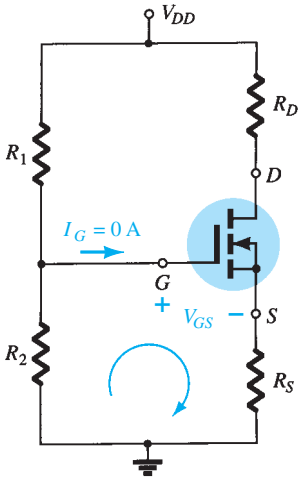


FIG. 7.43
Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (7.40) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

Solution:

Network

$$\text{Eq. (7.39):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$\text{Eq. (7.40):} \quad V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

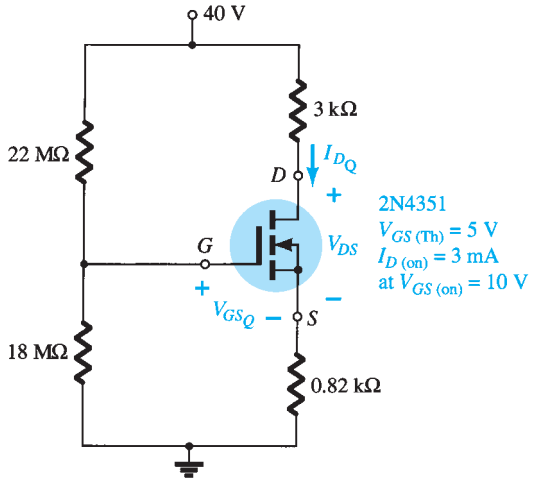


FIG. 7.44
Example 7.11.

When $I_D = 0$ mA,

$$V_{GS} = 18\text{ V} - (0\text{ mA})(0.82\text{ k}\Omega) = 18\text{ V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0$ V,

$$V_{GS} = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$
$$0 = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$
$$I_D = \frac{18\text{ V}}{0.82\text{ k}\Omega} = 21.95\text{ mA}$$

as appearing on Fig. 7.45.

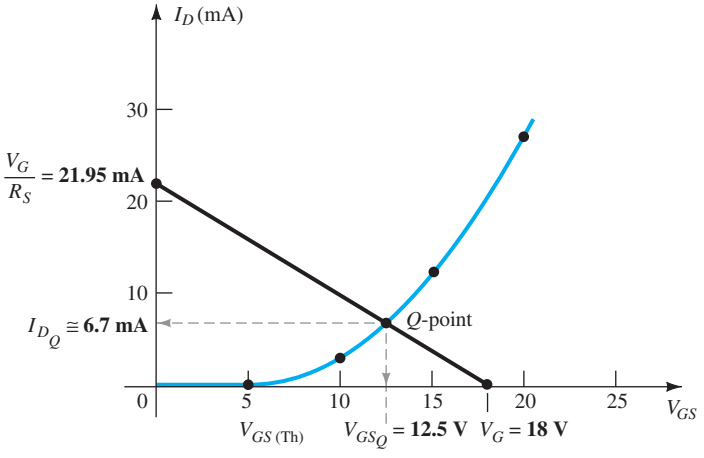


FIG. 7.45
Determining the Q-point for the network of Example 7.11.

Device

$$V_{GS(\text{Th})} = 5\text{ V}, \quad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

Eq. (7.34):
$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and
$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$
$$V_{GS_Q} = \mathbf{12.5\ V}$$

Eq. (7.41):
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$
$$= 40\ \text{V} - 25.6\ \text{V}$$
$$= \mathbf{14.4\ V}$$

7.9 SUMMARY TABLE

Table 7.1 reviews the basic results and demonstrates the similarity in approach for a number of FET configurations. It also reveals that the analysis of dc configurations for FETs is fairly straightforward. Once the transfer characteristics are established, the network bias line can be drawn and the Q-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

7.10 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 4 to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

EXAMPLE 7.12 Determine the levels of V_D and V_C for the network of Fig. 7.46.

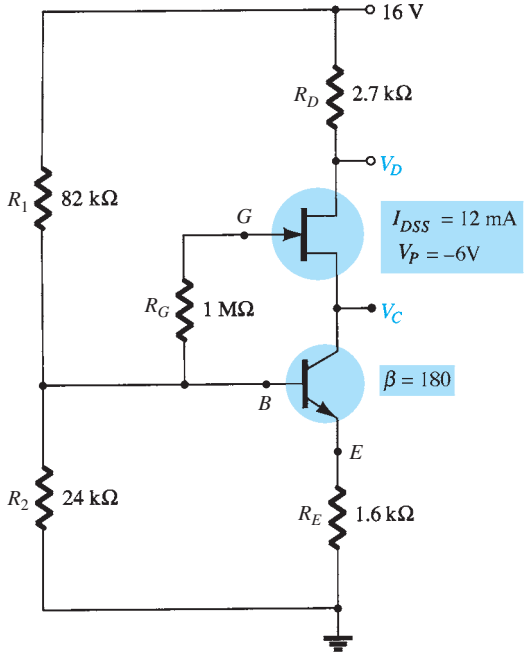
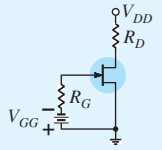
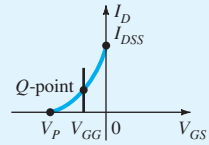
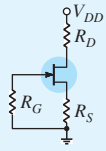
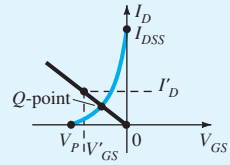
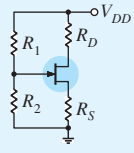
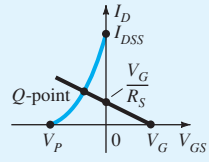
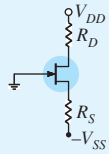
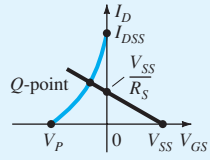
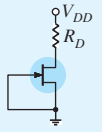
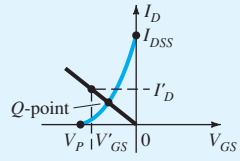
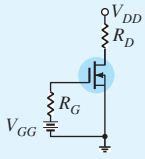
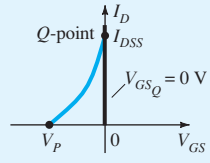
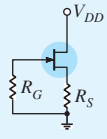
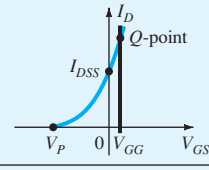
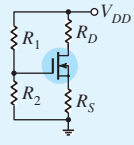
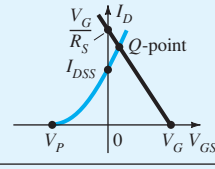
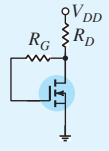
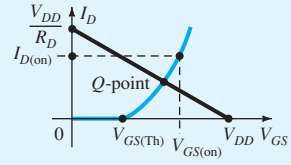
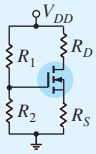
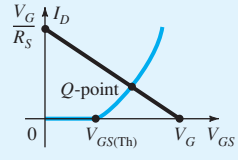


FIG. 7.46
Example 7.12.

TABLE 7.1

FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Solution: From experience we now realize that V_{GS} is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since V_{GS} is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ($\beta R_E = 180 \times 1.6\,\text{k}\Omega = 288\,\text{k}\Omega > 10R_2 = 240\,\text{k}\Omega$), permitting a determination of V_B using the voltage-divider rule on the input circuit.

For V_B,

$$V_B = \frac{24\,\text{k}\Omega(16\text{ V})}{82\,\text{k}\Omega + 24\,\text{k}\Omega} = 3.62\text{ V}$$

Using the fact that $V_{BE} = 0.7$ V results in

$$V_E = V_B - V_{BE} = 3.62\text{ V} - 0.7\text{ V} = 2.92\text{ V}$$

and

$$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92\text{ V}}{1.6\,\text{k}\Omega} = 1.825\text{ mA}$$

with

$$I_C \cong I_E = 1.825\text{ mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and

$$V_D = 16\text{ V} - I_D(2.7\,\text{k}\Omega) = 16\text{ V} - (1.825\text{ mA})(2.7\,\text{k}\Omega) = 16\text{ V} - 4.93\text{ V} = \mathbf{11.07\text{ V}}$$

The question of how to determine V_C is not as obvious. Both V_{CE} and V_{DS} are unknown quantities, preventing us from establishing a link between V_D and V_C or from V_E to V_D. A more careful examination of Fig. 7.46 reveals that V_C is linked to V_B by V_{GS} (assuming that $V_{R_G} = 0$ V). Since we know V_B if we can find V_{GS}, V_C can be determined from

$$V_C = V_B - V_{GS}$$

The question then arises as to how to find the level of V_{GS_Q} from the quiescent value of I_D. The two are related by Shockley's equation:

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

and V_{GS_Q} could be found mathematically by solving for V_{GS_Q} and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 7.47. The level of $I_{D_Q} = I_{S_Q} = I_{C_Q} = I_{E_Q}$ is then established by a horizontal line as shown in the same figure. V_{GS_Q} is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GS_Q} = \mathbf{-3.7\text{ V}}$$

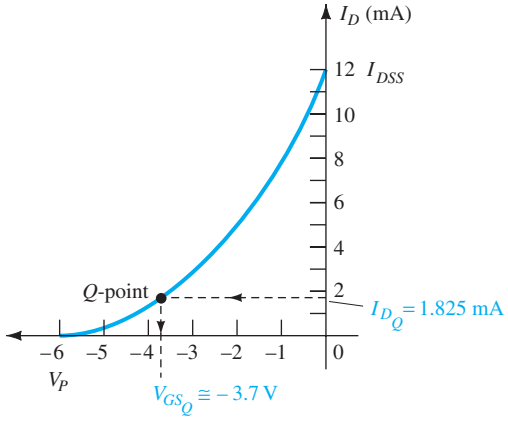


FIG. 7.47
Determining the Q-point for the network of Fig. 7.46.

The level of V_C is given by

$$V_C = V_B - V_{GS_Q} = 3.62\text{ V} - (-3.7\text{ V})$$
$$= \mathbf{7.32\text{ V}}$$

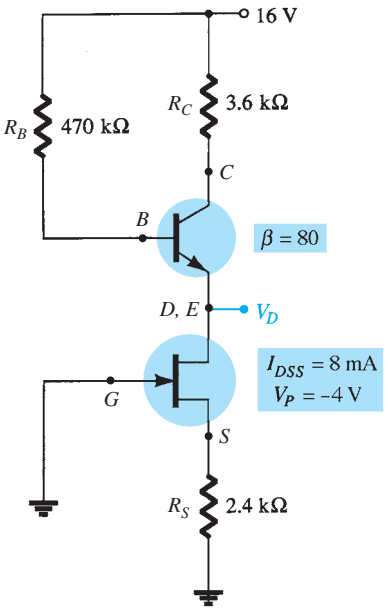


FIG. 7.48
Example 7.13.

EXAMPLE 7.13 Determine V_D for the network of Fig. 7.48.

Solution: In this case, there is no obvious path for determining a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, we can derive an equation for V_{GS} and determine the resulting quiescent point using graphical techniques. That is,

$$V_{GS} = -I_D R_S = -I_D(2.4\text{ k}\Omega)$$

resulting in the self-bias line appearing in Fig. 7.49, which establishes a quiescent point at

$$V_{GS_Q} = -2.4\text{ V}$$
$$I_{D_Q} = 1\text{ mA}$$

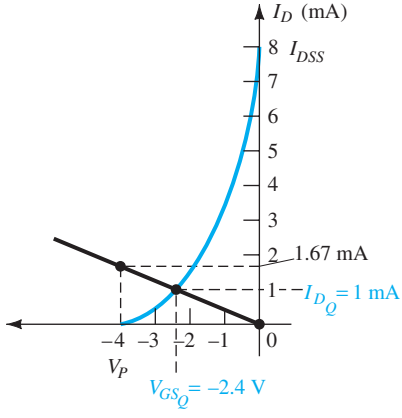


FIG. 7.49
Determining the Q-point for the network of Fig. 7.48.

For the transistor,

$$I_E \cong I_C = I_D = 1\text{ mA}$$

and

$$I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{80} = 12.5\ \mu\text{A}$$

$$V_B = 16\text{ V} - I_B(470\text{ k}\Omega)$$
$$= 16\text{ V} - (12.5\ \mu\text{A})(470\text{ k}\Omega) = 16\text{ V} - 5.88\text{ V}$$
$$= 10.12\text{ V}$$

and

$$V_E = V_D = V_B - V_{BE}$$
$$= 10.12\text{ V} - 0.7\text{ V}$$
$$= \mathbf{9.42\text{ V}}$$

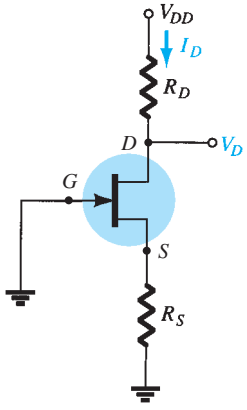


FIG. 7.50
Self-bias configuration to be designed.

7.11 DESIGN

The design process is a function of the area of application, level of amplification desired, signal strength, and operating conditions. The first step is normally to establish the proper dc levels of operation.

For example, if the levels of V_D and I_D are specified for the network of Fig. 7.50, the level of V_{GS_Q} can be determined from a plot of the transfer curve and R_S can then be determined from $V_{GS} = -I_D R_S$. If V_{DD} is specified, the level of R_D can then be calculated from $R_D = (V_{DD} - V_D)/I_D$. Of course, the values of R_S and R_D may not be standard commercial values, requiring that the nearest commercial values be employed. However, with the tolerance (range of values) normally specified for the parameters of a network,

the slight variation due to the choice of standard values will seldom cause a real concern in the design process.

The above is only one possibility for the design phase involving the network of Fig. 7.50. It is possible that only V_{DD} and R_D are specified together with the level of V_{DS}. The device to be employed may have to be specified along with the level of R_S. It appears logical that the device chosen should have a maximum V_{DS} greater than the specified value by a safe margin.

In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cutoff (V_P) regions. Levels of V_{GS_Q} close to $V_P/2$ or levels of I_{D_Q} near $I_{DSS}/2$ are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of I_D and V_{DS} as appearing on the specification sheet must not be exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as R_D, R_S, V_{DD}, and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \tag{7.42}$$

where V_R and I_R are often parameters that can be found directly from the specified voltage and current levels.

EXAMPLE 7.14 For the network of Fig. 7.51, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

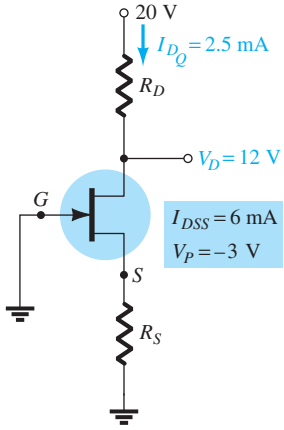


FIG. 7.51
Example 7.14.

Solution: As defined by Eq. (7.42),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\text{ V} - 12\text{ V}}{2.5\text{ mA}} = \frac{8\text{ V}}{2.5\text{ mA}} = \mathbf{3.2\,k\Omega}$$

Plotting the transfer curve in Fig. 7.52 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA results in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_D R_S$ establishes the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\text{ V})}{2.5\text{ mA}} = \mathbf{0.4\,k\Omega}$$

The nearest standard commercial values are

$$R_D = 3.2\,\text{k}\Omega \Rightarrow \mathbf{3.3\,k\Omega}$$
$$R_S = 0.4\,\text{k}\Omega \Rightarrow \mathbf{0.39\,k\Omega}$$

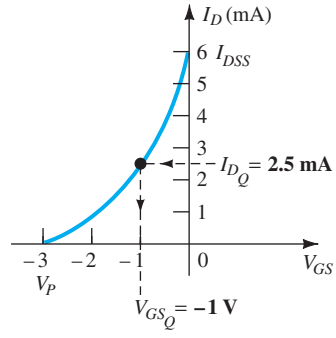


FIG. 7.52
Determining V_{GS_Q} for the network of Fig. 7.51.

EXAMPLE 7.15 For the voltage-divider bias configuration of Fig. 7.53, if $V_D = 12$ V and $V_{GS_Q} = -2$ V, determine the value of R_S.

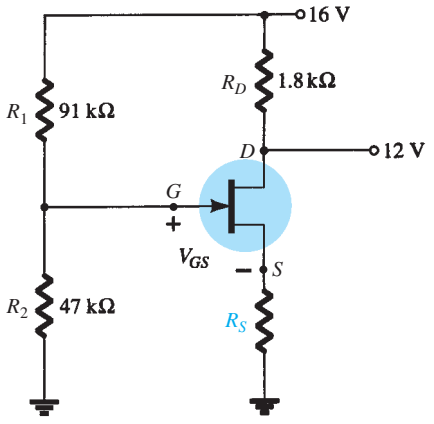


FIG. 7.53
Example 7.15.

Solution: The level of V_G is determined as follows:

$$V_G = \frac{47\text{ k}\Omega(16\text{ V})}{47\text{ k}\Omega + 91\text{ k}\Omega} = 5.44\text{ V}$$

with

$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$= \frac{16\text{ V} - 12\text{ V}}{1.8\text{ k}\Omega} = 2.22\text{ mA}$$

The equation for V_{GS} is then written and the known values substituted:

$$V_{GS} = V_G - I_D R_S$$

$$-2\text{ V} = 5.44\text{ V} - (2.22\text{ mA})R_S$$

$$-7.44\text{ V} = -(2.22\text{ mA})R_S$$

and

$$R_S = \frac{7.44\text{ V}}{2.22\text{ mA}} = \mathbf{3.35\text{ k}\Omega}$$

The nearest standard commercial value is 3.3 kΩ.

EXAMPLE 7.16 The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(\text{on})}$ for the network of Fig. 7.54. Determine the levels of V_{DD} and R_D.

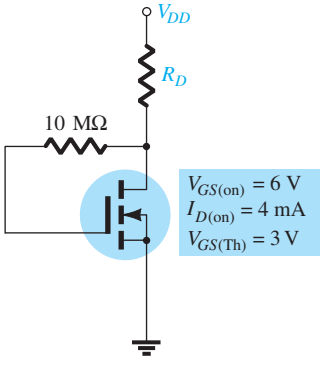


FIG. 7.54
Example 7.16.

Solution: Given $I_D = I_{D(\text{on})} = 4$ mA and $V_{GS} = V_{GS(\text{on})} = 6$ V, for this configuration,

$$V_{DS} = V_{GS} = \tfrac{1}{2}V_{DD}$$

and

$$6\text{ V} = \tfrac{1}{2}V_{DD}$$

so that

$$V_{DD} = \mathbf{12\text{ V}}$$

Applying Eq. (7.42) yields

$$R_D = \frac{V_{R_D}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(\text{on})}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(\text{on})}} = \frac{\frac{1}{2}V_{DD}}{I_{D(\text{on})}}$$

and

$$R_D = \frac{6\text{ V}}{4\text{ mA}} = \mathbf{1.5\text{ k}\Omega}$$

which is a standard commercial value.

7.12 TROUBLESHOOTING

How often has a network been carefully constructed only to find that when the power is applied, the response is totally unexpected and fails to match the theoretical calculations? What is the next step? Is it a bad connection? A misreading of the color code for a resistive element? An error in the construction process? The range of possibilities seems vast and often frustrating. The troubleshooting process first described in the analysis of BJT transistor configurations should narrow down the list of possibilities and isolate the problem area following a definite plan of attack. In general, the process begins with a rechecking of the network construction and the terminal connections. This is usually followed by the checking of voltage levels between specific terminals and ground or between terminals of the network. Seldom are current levels measured since such maneuvers require disturbing the network structure to insert the meter. Of course, once the voltage levels are obtained, current levels can be calculated using Ohm's law. In any case, some idea of the expected voltage or current level must be known for the measurement to have any importance. In total, therefore, the troubleshooting process can begin with some hope of success only if the basic operation of the network is understood along with some expected levels of voltage or current. For the *n*-channel JFET amplifier, it is clearly understood that the quiescent value of V_{GS_Q} is limited to 0 V or a negative voltage. For the network of Fig. 7.55, V_{GS_Q} is limited to negative values in the range 0 V to V_P. If a meter is hooked up as shown in Fig. 7.55, with the positive lead (normally red) to the gate and the negative lead (usually black) to the source, the resulting reading should have a negative sign and a magnitude of a few volts. Any other response should be considered suspicious and needs to be investigated.

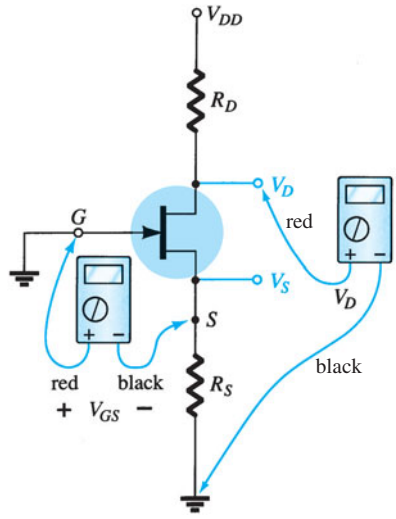


FIG. 7.55
Checking the dc operation of the JFET self-bias configuration.

The level of V_{DS} is typically between 25% and 75% of V_{DD}. A reading of 0 V for V_{DS} clearly indicates that either the output circuit has an "open" or the JFET is internally short-circuited between drain and source. If V_D is V_{DD} volts, there is obviously no drop across R_D, due to the lack of current through R_D, and the connections should be checked for continuity.

If the level of V_{DS} seems inappropriate, the continuity of the output circuit can easily be checked by grounding the negative lead of the voltmeter and measuring the voltage levels from V_{DD} to ground using the positive lead. If $V_D = V_{DD}$, the current through R_D may be zero, but there is continuity between V_D and V_{DD}. If $V_S = V_{DD}$, the device is not open between drain and source, but it is also not "on." The continuity through to V_S is confirmed, however. In this case, it is possible that there is a poor ground connection between R_S and ground that may not be obvious. The internal connection between the wire of the lead and the terminal connector may have separated. Other possibilities also exist, such as a shorted device from drain to source, but the troubleshooter will simply have to narrow down the possible causes for the malfunction.

The continuity of a network can also be checked simply by measuring the voltage across any resistor of the network (except for R_G in the JFET configuration). An indication of 0 V immediately reveals the lack of current through the element due to an open circuit in the network.

The most sensitive element in the BJT and JFET configurations is the amplifier itself. The application of excessive voltage during the construction or testing phase or the use of incorrect resistor values resulting in high current levels can destroy the device. If you question the condition of the amplifier, the best test for the FET is the curve tracer since it not only reveals whether the device is operable, but also its range of current and voltage levels. Some testers may reveal that the device is still fundamentally sound but do not reveal whether its range of operation has been severely reduced.

The development of good troubleshooting techniques comes primarily from experience and a level of confidence in what to expect and why. There are, of course, times when the reasons for a strange response seem to disappear mysteriously when you check a network. In such cases, it is best not to breathe a sigh of relief and continue with the construction. The cause for such a sensitive "make or break" situation should be found and corrected, or it may reoccur at the most inopportune moment.

7.13 *p*-CHANNEL FETs

The analysis thus far has been limited solely to *n*-channel FETs. For *p*-channel FETs, a mirror image of the transfer curves is employed, and the defined current directions are reversed as shown in Fig. 7.56 for the various types of FETs.

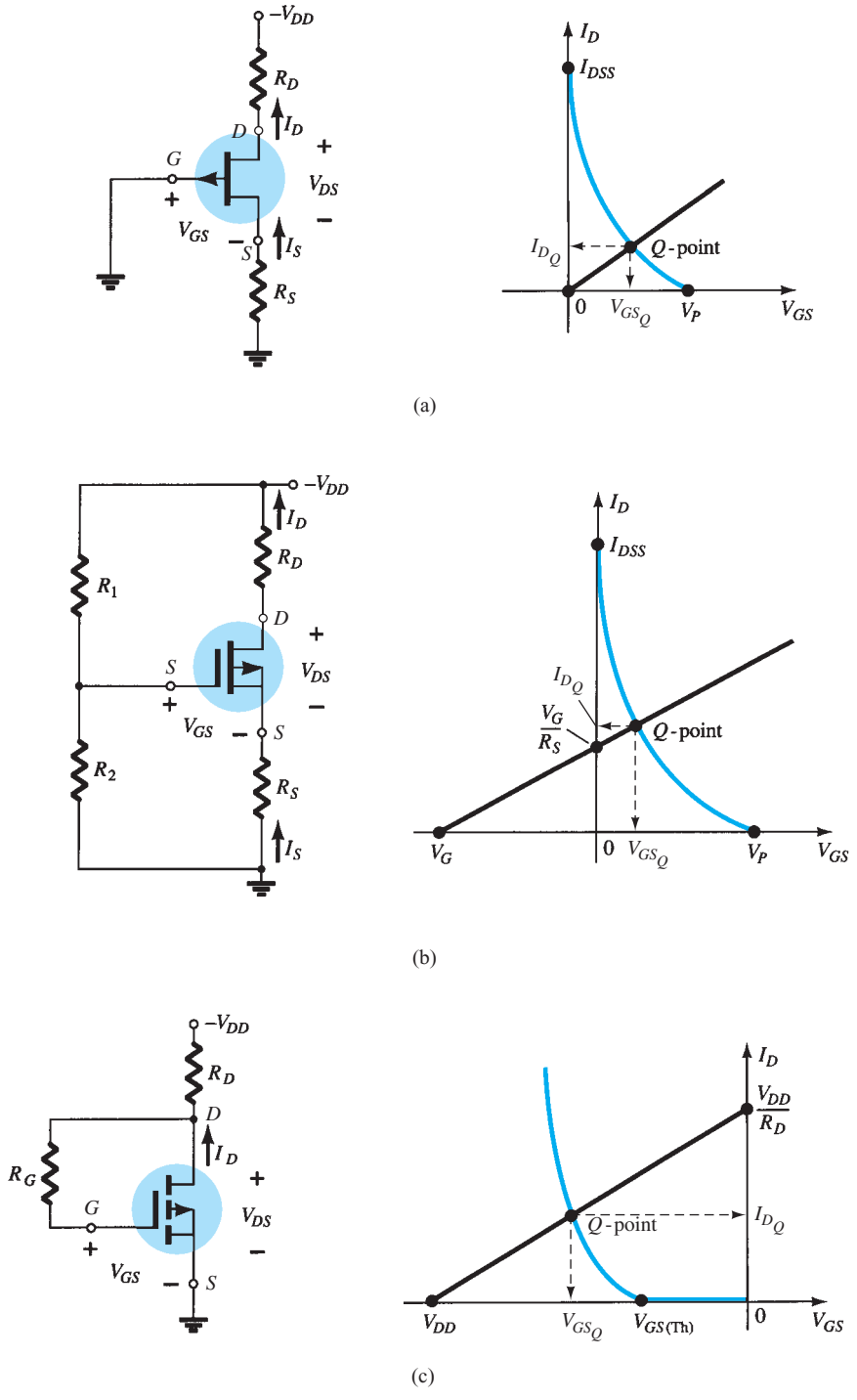


FIG. 7.56
p-Channel configurations: (a) JFET; (b) depletion-type MOSFET; (c) enhancement-type MOSFET.

Note for each configuration of Fig. 7.56 that each supply voltage is now a negative voltage drawing current in the indicated direction. In particular, note that the double-subscript notation for voltages continues as defined for the *n*-channel device: V_{GS}, V_{DS}, and so on. In this case, however, V_{GS} is positive (positive or negative for the depletion-type MOSFET) and V_{DS} negative.

Due to the similarities between the analysis of *n*-channel and *p*-channel devices, one can assume an *n*-channel device and reverse the supply voltage and perform the entire analysis. When the results are obtained, the magnitude of each quantity will be correct, although the current direction and voltage polarities will have to be reversed. However, the next example

will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.

EXAMPLE 7.17 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the *p*-channel JFET of Fig. 7.57.

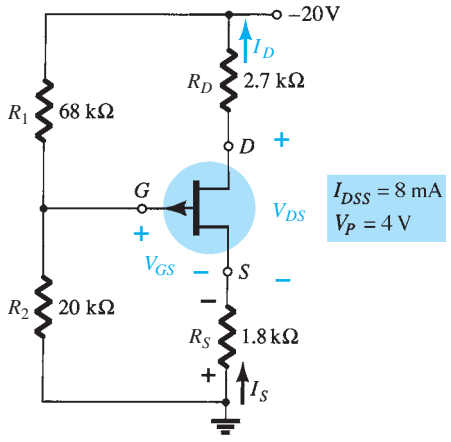


FIG. 7.57
Example 7.17.

Solution: We have

$$V_G = \frac{20\,\text{k}\Omega(-20\,\text{V})}{20\,\text{k}\Omega + 68\,\text{k}\Omega} = -4.55\,\text{V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0$ mA yields

$$V_{GS} = V_G = -4.55\,\text{V}$$

as appearing in Fig. 7.58.

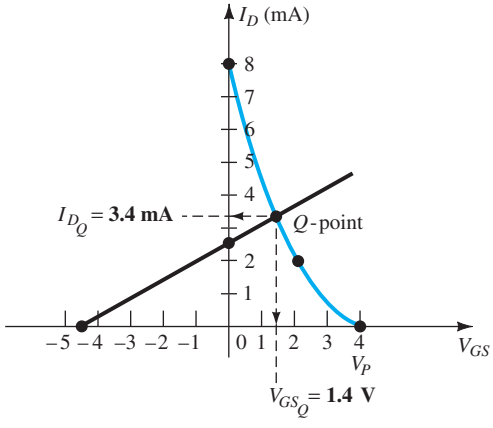


FIG. 7.58
Determining the Q-point for the JFET configuration of Fig. 7.57.

Choosing $V_{GS} = 0$ V, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\,\text{V}}{1.8\,\text{k}\Omega} = 2.53\,\text{mA}$$

as also appearing in Fig. 7.58.

The resulting quiescent point from Fig. 7.58 is given by

$$I_{D_Q} = \mathbf{3.4\ mA}$$
$$V_{GS_Q} = \mathbf{1.4\ V}$$

For V_{DS}, Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\ \text{V} + (3.4\ \text{mA})(2.7\ \text{k}\Omega + 1.8\ \text{k}\Omega) \\ &= -20\ \text{V} + 15.3\ \text{V} \\ &= \mathbf{-4.7\ V} \end{aligned}$$

7.14 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GS_Q}) is provided in Fig. 7.59. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled *m* can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled *M*, is employed along with the *m* scale to find the

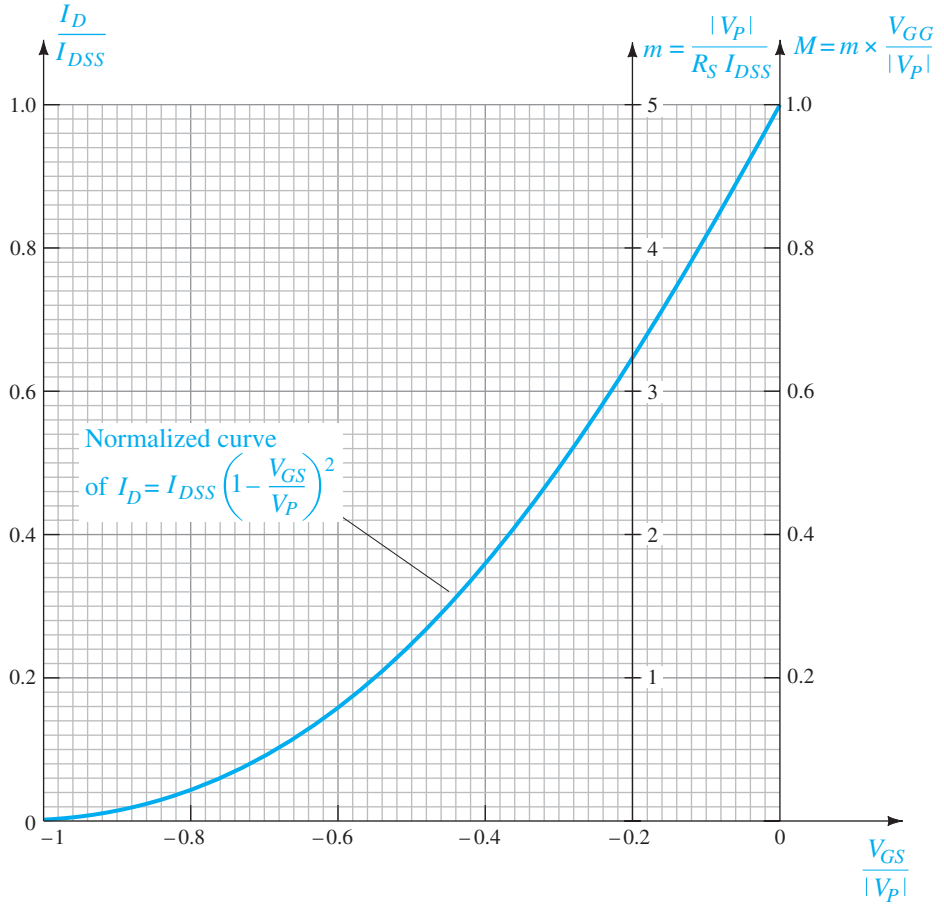


FIG. 7.59
Universal JFET bias curve.

solution to voltage-divider configurations. The scaling for m and M come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the m scale extends from 0 to 5 at $V_{GS}/|V_P| = -0.2$ and the M scale ranges from 0 to 1 at $V_{GS}/|V_P| = 0$, but rather on how to use the resulting scales to obtain a solution for the configurations. The equations for m and M are the following, with V_G as defined by Eq. (7.15):

$$m = \frac{|V_P|}{I_{DSS}R_S} \tag{7.43}$$

$$M = m \times \frac{V_G}{|V_P|} \tag{7.44}$$

with

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the m and M axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

EXAMPLE 7.18 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.60.

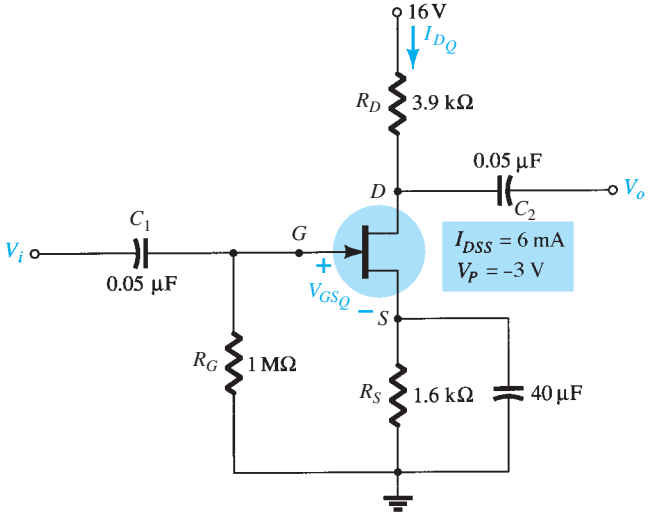


FIG. 7.60
Example 7.18.

Solution: Calculating the value of m, we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3\text{ V}|}{(6\text{ mA})(1.6\text{ k}\Omega)} = 0.31$$

The self-bias line defined by R_S is plotted by drawing a straight line from the origin through a point defined by $m = 0.31$, as shown in Fig. 7.61.

The resulting Q-point:

$$\frac{I_D}{I_{DSS}} = 0.18 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.575$$

The quiescent values of I_D and V_{GS} can then be determined as follows:

$$I_{D_Q} = 0.18I_{DSS} = 0.18(6\text{ mA}) = \mathbf{1.08\text{ mA}}$$

and

$$V_{GS_Q} = -0.575|V_P| = -0.575(3\text{ V}) = \mathbf{-1.73\text{ V}}$$

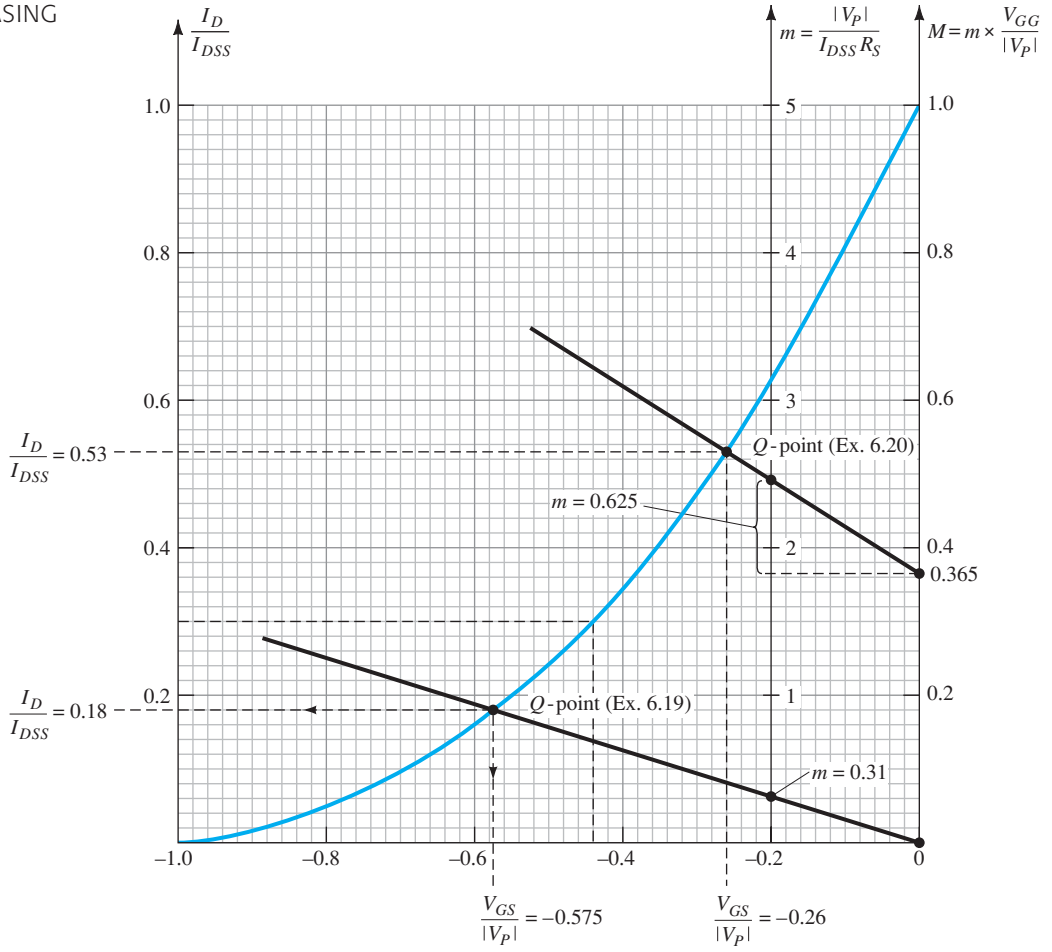


FIG. 7.61
Universal curve for Examples 7.18 and 7.19.

EXAMPLE 7.19 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.62.

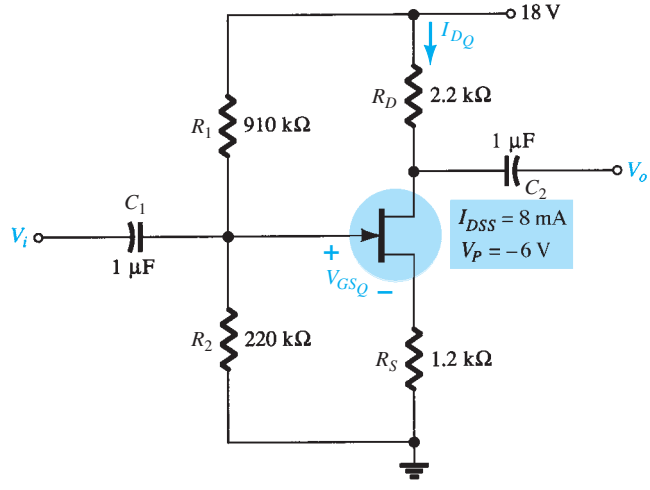


FIG. 7.62
Example 7.19.

Solution: Calculating m gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining V_G yields

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(220\,\text{k}\Omega)(18\text{ V})}{910\,\text{k}\Omega + 220\,\text{k}\Omega} = 3.5\text{ V}$$

Finding M, we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625\left(\frac{3.5\text{ V}}{6\text{ V}}\right) = 0.365$$

Now that m and M are known, the bias line can be drawn on Fig. 7.61. In particular, note that even though the levels of I_{DSS} and V_P are different for the two networks, the same universal curve can be employed. First find M on the M axis as shown in Fig. 7.61. Then draw a horizontal line over to the m axis and, at the point of intersection, add the magnitude of m as shown in the figure. Using the resulting point on the m axis and the M intersection, draw the straight line to intersect with the transfer curve and define the Q-point. That is,

$$\frac{I_D}{I_{DSS}} = 0.53 \qquad \text{and} \qquad \frac{V_{GS}}{|V_P|} = -0.26$$

and $$I_{D_Q} = 0.53 I_{DSS} = 0.53(8\text{ mA}) = \mathbf{4.24\text{ mA}}$$

with $$V_{GS_Q} = -0.26|V_P| = -0.26(6\text{ V}) = \mathbf{-1.56\text{ V}}$$

7.15 PRACTICAL APPLICATIONS

The applications described here take full advantage of the high input impedance of field-effect transistors, the isolation that exists between the gate and drain circuits, and the linear region of JFET characteristics that permit approximating the device by a resistive element between the drain and source terminals.

Voltage-Controlled Resistor (Noninverting Amplifier)

One of the most common applications of the JFET is as a variable resistor whose resistance value is controlled by the applied dc voltage at the gate terminal. In Fig. 7.63a, the linear region of a JFET transistor has been clearly indicated. Note that in this region the various curves all start at the origin and follow a fairly straight path as the drain-to-source voltage and drain current increase. Recall from your basic dc courses that **the plot of a fixed resistor is nothing more than a straight line with its origin at the intersection of the axes**.

In Fig. 7.63b, the linear region has been expanded to a maximum drain-to-source voltage of about 0.5 V. Note that even though the curves do have some curvature to them, they can easily be approximated by fairly straight lines, all having their origin at the intersection of the axes and a slope determined by the gate-to-source dc voltage. Recall from earlier discussions that **for an *I–V* plot where the current is the vertical axis and the voltage the horizontal axis, the steeper the slope, the less is the resistance; and the more horizontal the curve, the greater is the resistance**. The result is that a vertical line has 0 Ω resistance and a horizontal line has infinite resistance. At $V_{GS} = 0$ V, the slope is the steepest and the resistance the least. As the gate-to-source voltage becomes increasingly negative, the slope decreases until it is almost horizontal near the pinch-off voltage.

It is important to remember that this linear region is limited to levels of V_{DS} that are relatively small compared to the pinch-off voltage. In general, **the linear region of a JFET is defined by $V_{DS} \ll V_{DS_{max}}$ and $|V_{GS}| \ll |V_P|$**.

Using Ohm's law, let us calculate the resistance associated with each curve of Fig. 7.63b using the current that results at a drain-to-source voltage of 0.4 V.

$$V_{GS} = 0\text{ V}: \qquad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{4\text{ mA}} = \mathbf{100\ \Omega}$$

$$V_{GS} = -0.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{2.5\text{ mA}} = \mathbf{160\ \Omega}$$

$$V_{GS} = -1\text{ V}: \qquad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{1.5\text{ mA}} = \mathbf{267\ \Omega}$$

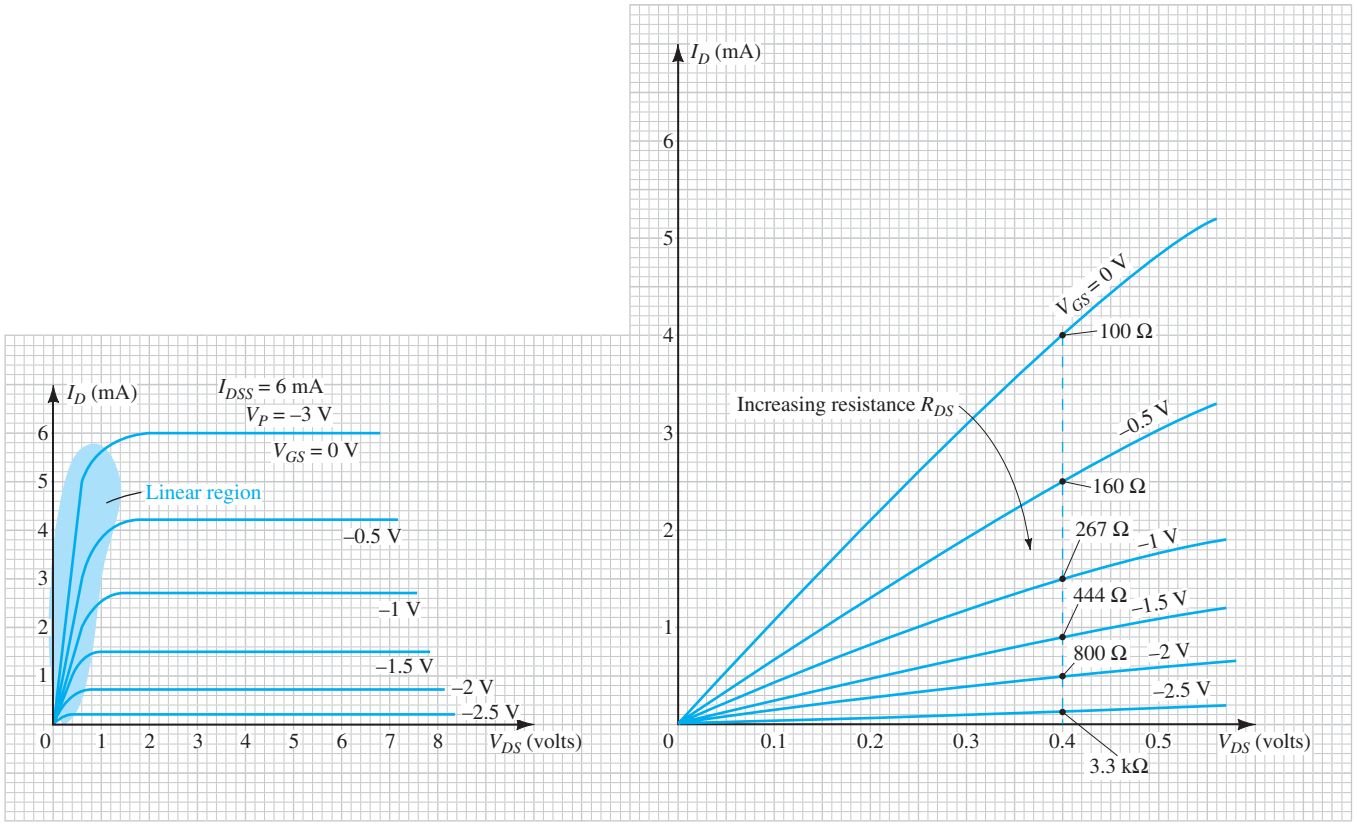


FIG. 7.63

JFET characteristics: (a) defining the linear region; (b) expanding the linear region.

$$V_{GS} = -1.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.9\text{ mA}} = \mathbf{444\ \Omega}$$

$$V_{GS} = -2\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.5\text{ mA}} = \mathbf{800\ \Omega}$$

$$V_{GS} = -2.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.12\text{ mA}} = \mathbf{3.3\ k\Omega}$$

In particular, note how **the drain-to-source resistance increases as the gate-to-source voltage approaches the pinch-off value**.

The results just obtained can be verified by Eq. (6.1) using the pinch-off voltage of -3 V and $R_o = 100\ \Omega$ at $V_{GS} = 0$ V. We have

$$R_{DS} = \frac{R_o}{\left(1 - \dfrac{V_{GS}}{V_P}\right)^2} = \frac{100\ \Omega}{\left(1 - \dfrac{V_{GS}}{-3\text{ V}}\right)^2}$$

$$V_{GS} = -0.5\text{ V}: \quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-0.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{144\ \Omega} \quad \text{(versus 160 } \Omega \text{ above)}$$

$$V_{GS} = -1\text{ V}: \quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-1\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{225\ \Omega} \quad \text{(versus 267 } \Omega \text{ above)}$$

$$V_{GS} = -1.5\text{ V}: \quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-1.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{400\ \Omega} \quad \text{(versus 444 } \Omega \text{ above)}$$

$$V_{GS} = -2\text{ V}: \quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-2\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{900\ \Omega} \quad \text{(versus 800 } \Omega \text{ above)}$$

$$V_{GS} = -2.5\text{ V}: R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-2.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{3.6\ k\Omega} \quad \text{(versus 3.3 k}\Omega \text{ above)}$$

Although the results are not an exact match, for most applications Equation (6.1) provides an excellent approximation to the actual resistance level for R_{DS}.

Keep in mind that **the possible levels of V_{GS} between 0 V and pinch-off are infinite**, resulting in the full range of resistor values between 100 Ω and 3.3 kΩ. In general, therefore, the above discussion is summarized by Fig. 7.64a. For $V_{GS} = 0$ V, the equivalence of Fig. 7.64b would result; for $V_{GS} = -1.5$ V, the equivalence of Fig. 7.64c; and so on.

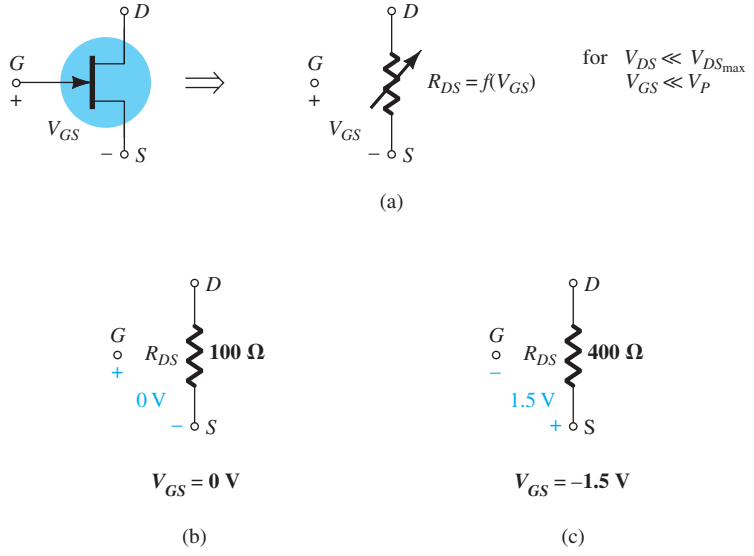


FIG. 7.64

JFET voltage-controlled drain resistance: (a) general equivalence; (b) with $V_{GS} = 0$ V; (c) with $V_{GS} = -1.5$ V.

Let us now investigate the use of this voltage-controlled drain resistance in the noninverting amplifier of Fig. 7.65a—**noninverting indicates that the input and output signals are in phase**. The op-amp of Fig. 7.65a is discussed in detail in Chapter 10, and the equation for the gain is derived in Section 10.4.

If $R_f = R_1$, the resulting gain is 2, as shown by the in-phase sinusoidal signals of Fig. 7.65a. In Fig. 7.65b, the variable resistor has been replaced by an *n*-channel JFET. If $R_f = 3.3\text{ k}\Omega$ and the transistor of Fig. 7.63 were employed, the gain could extend from $1 + 3.3\text{ k}\Omega/3.3\text{ k}\Omega = 2$ to $1 + 3.3\text{ k}\Omega/100\ \Omega = 34$ for V_{GS} varying from −2.5 V to 0 V, respectively. In general, therefore, the gain of the amplifier can be set at any value between 2 and 34 by simply controlling the applied dc biasing voltage. The effect of this type of control can be extended to an extensive variety of applications. For instance, if the battery voltage of a radio should start to drop due to extended use, the dc level at the gate of the controlling JFET will drop, and the level of R_{DS} will decrease also. A drop in R_{DS} will result in an increase in gain for the same value of R_f, and the output volume of the radio can be maintained. A number of oscillators (networks designed to generate sinusoidal signals of specific frequencies) have a resistance factor in the equation for the frequency generated. If the frequency generated should start to drift, a feedback network can be designed that changes the dc level at the gate of a JFET and therefore its drain resistance. If that drain resistance is part of the resistance factor in the frequency equation, the frequency generated can be stabilized or maintained.

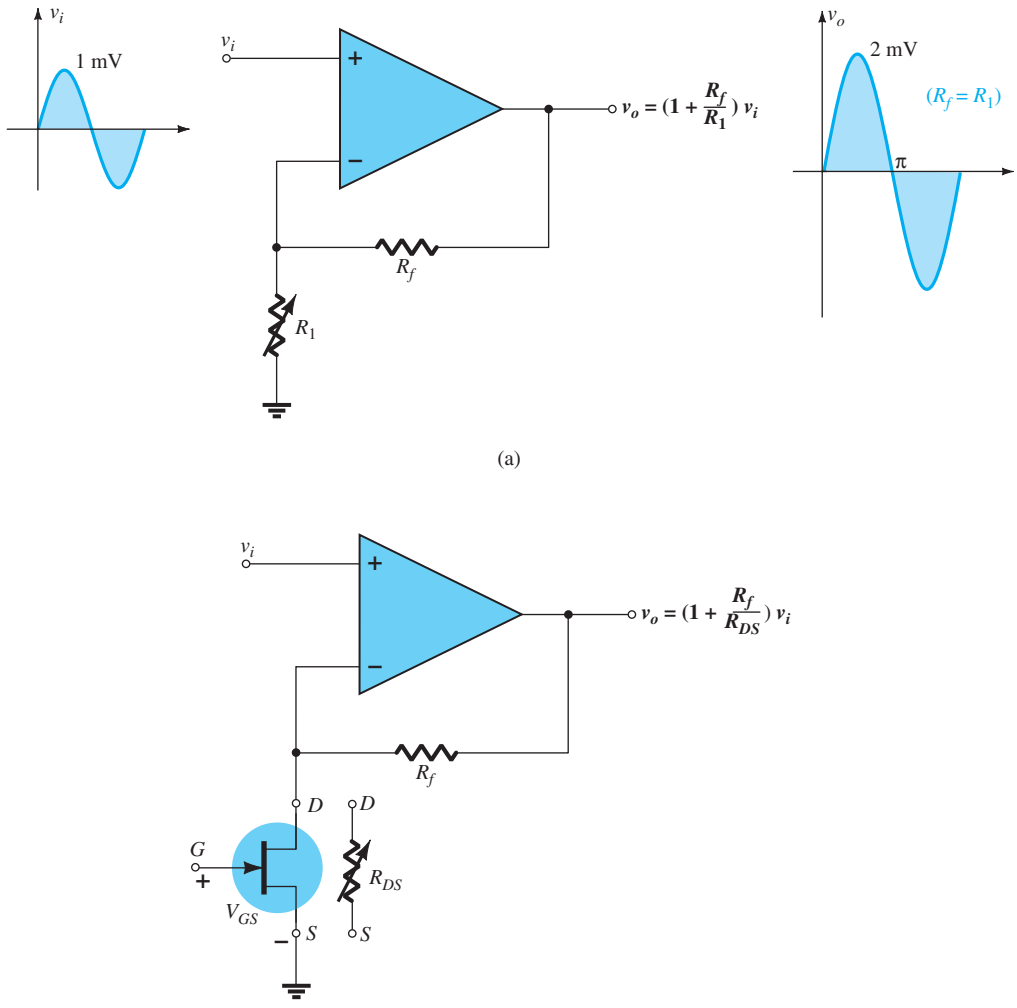


FIG. 7.65

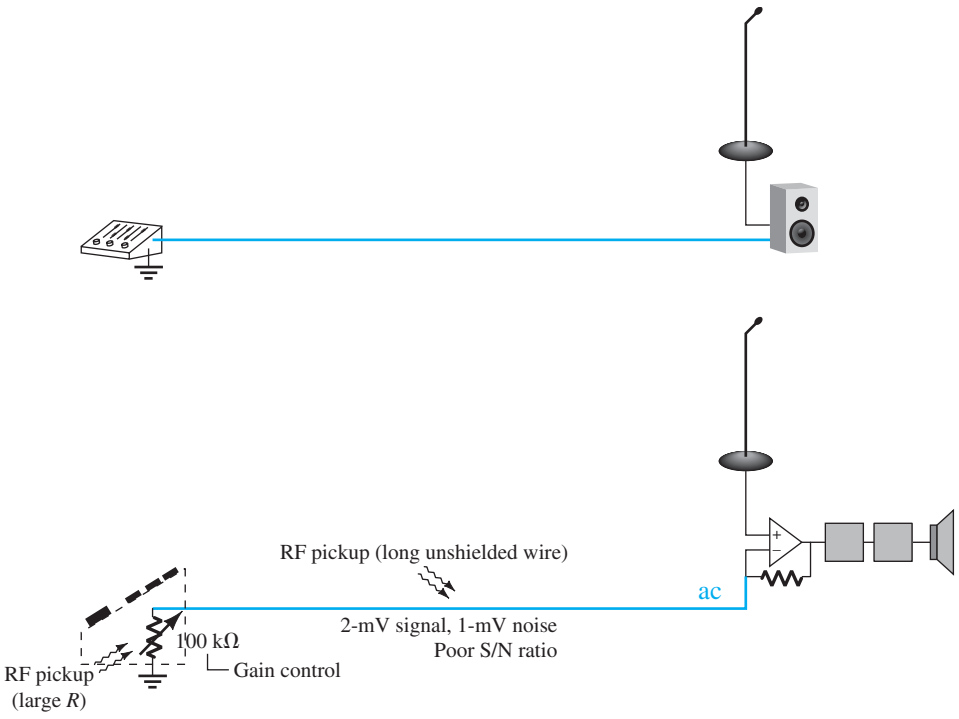
(a) Noninverting op-amp configuration; (b) using the voltage-controlled drain-to-source resistance of a JFET in the noninverting amplifier.

One of the most important factors that affect the stability of a system is temperature variation. As a system heats up, the usual tendency is for the gain to increase, which in turn will usually cause additional heating and may eventually result in a condition referred to as "thermal runaway." Through proper design, a thermistor can be introduced that will affect the biasing level of a voltage-controlled variable JFET resistor. As the resistance of the thermistor drops with increase in heat, the biasing control of the JFET can be such that the drain resistance changes in the amplifier design to reduce the gain—establishing a balancing effect.

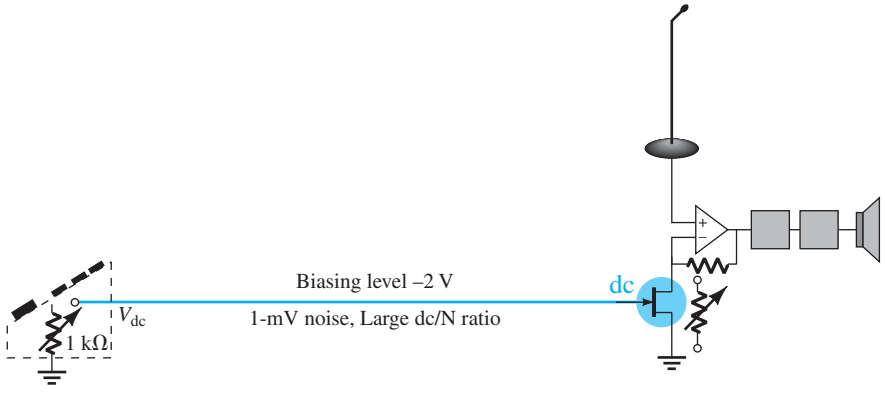
Before leaving the subject of thermal problems, note that some design specifications (often military type) require that systems that are overly sensitive to temperature variations be placed in a "chamber" or "oven" to establish a constant heat level. For instance, a 1-W resistor may be placed in an enclosed area with an oscillator network to establish a constant ambient heat level in the region. The design then centers on this heat level, which would be so high compared to the heat normally generated by the components that the variations in temperature levels of the elements could be ignored and a steady output frequency assured.

Other areas of application include any form of volume control, musical effects, meters, attenuators, filters, stability designs, and so on. One general advantage of this type of stability is that it avoids the need for expensive regulators (Chapter 15) in the overall design, although it should be understood that the purpose of this type of control mechanism is to "fine-tune" rather than to provide the primary source of stability.

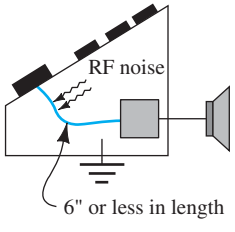
For the noninverting amplifier, **one of the most important advantages associated with using a JFET for control is the fact that it is dc rather than ac control**. For most systems, dc control not only results in a reduced chance of adding unwanted noise to the system, but also lends itself well to remote control. For example, in Fig. 7.66a, a remote control panel controls the amplifier gain for the speaker by an ac line connected to the variable resistor.



(a)



(b)



(c)

FIG. 7.66

Demonstrating the benefits of dc control: system with (a) ac control; (b) dc control; (c) RF noise pickup.

The long line from the amplifier can easily pick up noise from the surrounding air as generated by fluorescent lights, local radio stations, operating equipment (even computers), motors, generators, and so on. The result may be a 2-mV signal on the line with a 1-mV noise level—a terrible signal-to-noise ratio, which would only contribute to further deterioration of the signal coming in from the microphone due to the loop gain of the amplifier. In Fig. 7.66b, a dc line controls the gate voltage of the JFET and the variable resistance of the noninverting amplifier. Even though the dc line voltage on the line may be only −2 V, a ripple of 1 mV picked up by the long line will result in a very large signal-to-noise ratio, which could essentially be ignored in the distortion process. In other words, the noise on the dc line would simply move the dc operating point slightly on the device characteristics and would have almost no effect on the resulting drain resistance—isolation between the noise on the line and the amplifier response would be almost ideal.

Even though Figures 7.66a and 7.66b have a relatively long control line, the control line may only be 6″ long, as shown in the control panel of Fig. 7.66c, where all the elements of the amplifier are housed in the same container. Consider, however, **that just 1″ is enough to pick up RF noise**, so dc control is a favorable characteristic for almost any system. Furthermore, since the control resistance in Fig. 7.66a is usually quite large (hundreds of kilohms), whereas the dc voltage control resistors of the dc system of Fig. 7.66b are usually quite small (a few kilohms), the volume control resistor for the ac system will absorb a great deal more ac noise than the dc design. This phenomenon is a result of the fact that **RF noise signals in the air have a very high internal resistance, and therefore the larger the pickup resistance, the greater is the RF noise absorbed by the receiver**. Recall Thévenin's theorem, which states that for maximum power transfer, the load resistance should equal the internal resistance of the source.

As noted above, **dc control lends itself to computer and remote control systems** since they operate off specific fixed dc levels. For instance, when an infrared (IR) signal is sent out by a remote control to the receiver in a TV or VCR, the signal is passed through a decoder–counter sequence to define a particular dc voltage level on a staircase of voltage levels that can be fed into the gate of the JFET. For a volume control, that gate voltage may control the drain resistance of a noninverting amplifier controlling the volume of the system.

Timer Network

The high isolation between gate and drain circuits permits the design of a relatively simple timer such as shown in Fig. 7.67. The switch is a normally open (NO) switch, which, when closed, will short out the capacitor and cause its terminal voltage to quickly drop to 0 V. The switching network can handle the rapid discharge of voltage across the capacitor

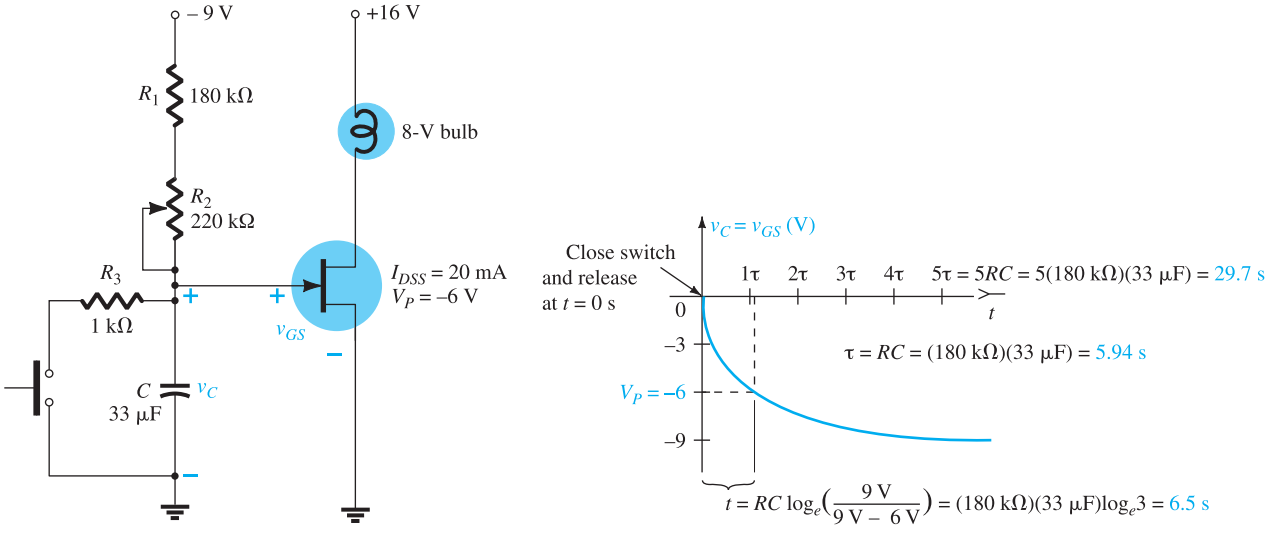


FIG. 7.67
JFET timer network.

because the working voltages are relatively low and the discharge time is extremely short. Some would say it is a poor design, but in the practical world it is frequently used and not looked on as a terrible crime.

When power is first applied, the capacitor will respond with its short-circuit equivalence since the **voltage across the capacitor cannot change instantaneously**. The result is that the gate-to-source voltage of the JFET will immediately be set to 0 V, the drain current I_D will equal I_{DSS}, and the bulb will turn on. However, with the switch in the normally open position, the capacitor will begin to charge to -9 V. **Because of the parallel high input impedance of the JFET, it has essentially no effect on the charging time constant of the capacitor**. Eventually, when the capacitor reaches the pinch-off level, the JFET and bulb will turn off. In general, therefore, when the system is first turned on, the bulb will light for a very short period of time and then turn off. It is now ready to perform its timing function.

When the switch is closed, it will short out the capacitor ($R_3 \ll R_1, R_2$) and will set the voltage at the gate to 0 V. The resulting drain current is I_{DSS}, and the bulb will burn brightly. When the switch is released, the capacitor will charge toward -9 V, and eventually when it reaches the pinch-off level, the JFET and bulb will turn off. The period during which the bulb is on will be determined by the time constant of the charging network, determined by $\tau = (R_1 + R_2)C$ and the level of the pinch-off voltage. The more negative the pinch-off level, the longer the bulb will be on. Resistor R_1 is included to be sure that there is some resistance in the charging circuit when the power is turned on. Otherwise, a very heavy current could result that might damage the network. Resistor R_2 is a variable resistor, so the "on" time can be controlled. Resistor R_3 was added to limit the discharge current when the switch is closed. When the switch across the capacitor is closed, the discharge time of the capacitor will be only $5\tau = 5RC = 5(1\ \text{k}\Omega)(33\ \mu\text{F}) = 165\ \mu\text{s} = 0.165\ \text{ms} = 0.000165$ s. In summary, therefore, when the switch is pressed and released, the bulb will come on brightly, and then, as time goes on, it will become dimmer until it shuts off after a period of time determined by the network time constant.

One of the most obvious applications of such a timing system is in a hallway or travel corridor where you want light for a short period of time so that you can pass safely but then want the system to turn off on its own. When you enter or leave a car, you may want a light on for a short period of time but don't want to worry about turning it off. There are endless possibilities for a timing network such as just described. Just consider the variety of other electrical or electronic systems that you would like to turn on for specific periods of time, and the list of uses grows exponentially.

One might ask why a BJT would not be a good alternative to the JFET for the same application. First, the input resistance of the BJT may be only a few kilohms. That would affect not only the time constant of the charging network, but also the maximum voltage to which the capacitor could charge. Just draw an equivalent network with the transistor replaced by a 1-kΩ resistor, and the above will immediately become clear. In addition, the control levels will have to be designed with a great deal more care since the BJT transistor turns on at about 0.7 V. The voltage swing from off to on is only 0.7 V rather than 4 V for the JFET configuration. One final note: You might have noticed the absence of a series resistor in the drain circuit for the situation when the bulb is first turned on and the resistance of the bulb is very low. The resulting current could be quite high until the bulb reaches its rated intensity. However, again, as described above for the switch across the capacitor, if the energy levels are small and the duration of stress minimal, such designs are often accepted. If there were any concern, adding a resistor of 0.1 to 1 Ω in series with the bulb would provide some security.

Fiber Optic Systems

The introduction of fiber optic technology has had a dramatic effect on the communications industry. The information-carrying capacity of fiber optic cable is significantly greater than that provided by conventional methods with individual pairs of wire. In addition, the cable size is reduced, the cable is less expensive, crosstalk due to electromagnetic effects between current-carrying conductors is eliminated, and noise pickup due to external disturbances such as lightning are eliminated.

The fiber optic industry is based on the fact that information can be transmitted on a beam of light. Although the speed of light through free space is 3×10^8 meters per second,

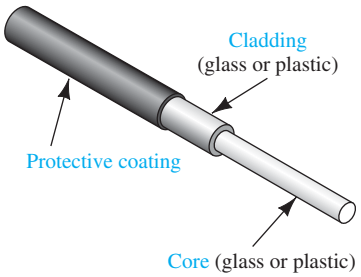


FIG. 7.68
Basic elements of a fiber optic cable.

or approximately 186,000 miles per second, its speed will be reduced by encounters with other media, causing reflection and refraction. When light information is passed through a fiber optic cable, it is expected to bounce off the walls of the cable. However, the angle at which the light is injected into the cable is critical, as is the actual design of the cable. In Fig. 7.68, the basic elements of a fiber optic cable are defined. The glass or plastic core of the cable can be as small as 8 μm, which is close to 1/10 the diameter of a human hair. The core is surrounded by an outer layer called the *cladding*, which is also made of glass or plastic, but has a different refractive index to ensure that the light in the core that hits the outer surface of the core is reflected back into the core. A protective coating is then added to protect the two layers from outside environmental effects.

Most optical communication systems work in the infrared frequency range, which extends from 3×10^{11} Hz to 5×10^{14} Hz. This spectrum is just below the visible light spectrum, which extends from 5×10^{14} Hz to 7.7×10^{14} Hz. For most optical systems the frequency range of 1.87×10^{14} Hz to 3.75×10^{14} Hz is used. Because of the very high frequencies, each carrier can be modulated by hundreds or thousands of voice channels simultaneously. In addition, very high speed computer transmission is a possibility, although one must be sure that the electronic components of the modulators can also operate successfully at the same frequency. For distances over 30 nautical miles, repeaters (a combination receiver, amplifier, and transmitter) must be used, which require an additional electrical conductor in the cable that carries a current of about 1.5 A at 2500 V.

The basic components of an optical communication system are shown in Fig. 7.69. The input signal is applied to a light modulator whose sole purpose is to convert the input signal to one of corresponding levels of light intensity to be directed down the length of fiber optic cable. The information is then carried through the cable to the receiving station, where a light demodulator converts the varying light intensities back to voltage levels that match those of the original signal.

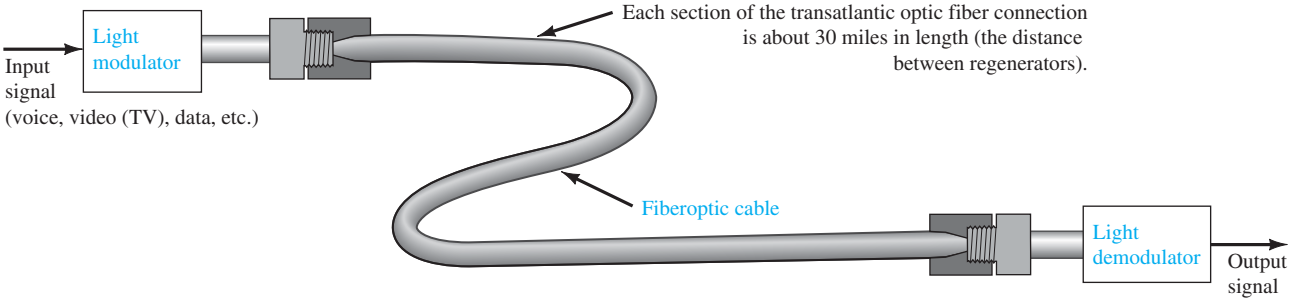


FIG. 7.69
Basic components of an optical communication system.

An electronic equivalent for the transmission of computer transistor-transistor-logic (TTL) information is provided in Fig. 7.70a. With the Enable control in the "on" or 1-state, the TTL information at the input to the AND gate can pass through to the gate of the JFET configuration. The design is such that the discrete levels of voltage associated with the TTL logic will turn the JFET on and off (perhaps 0 V and -5 V, respectively, for a JFET with $V_P = -4$ V). The resulting change in current levels will result in two distinct levels of light intensity from the LED (Section 1.16) in the drain circuit. That emitted light will then be directed through the cable to the receiving station, where a photodiode (Section 16.6) will react to the incident light and permit different levels of current to pass through as established by V and R. The current for photodiodes is a reverse current having the direction shown in Fig. 7.70a, but in the ac equivalent the photodiode and the resistor R are in parallel as shown in Fig. 7.70b, establishing the desired signal with the polarity shown at the gate of the JFET. Capacitor C is simply an open circuit to dc to isolate the biasing arrangement for the photodiode from the JFET and a short circuit as shown for the signal v_s. The incoming signal will then be amplified and will appear at the drain terminal of the output JFET.

As mentioned above, all the elements of the design, including the JFETs, LED, photodiode, capacitors, and so on, must be carefully chosen to ensure that they function properly

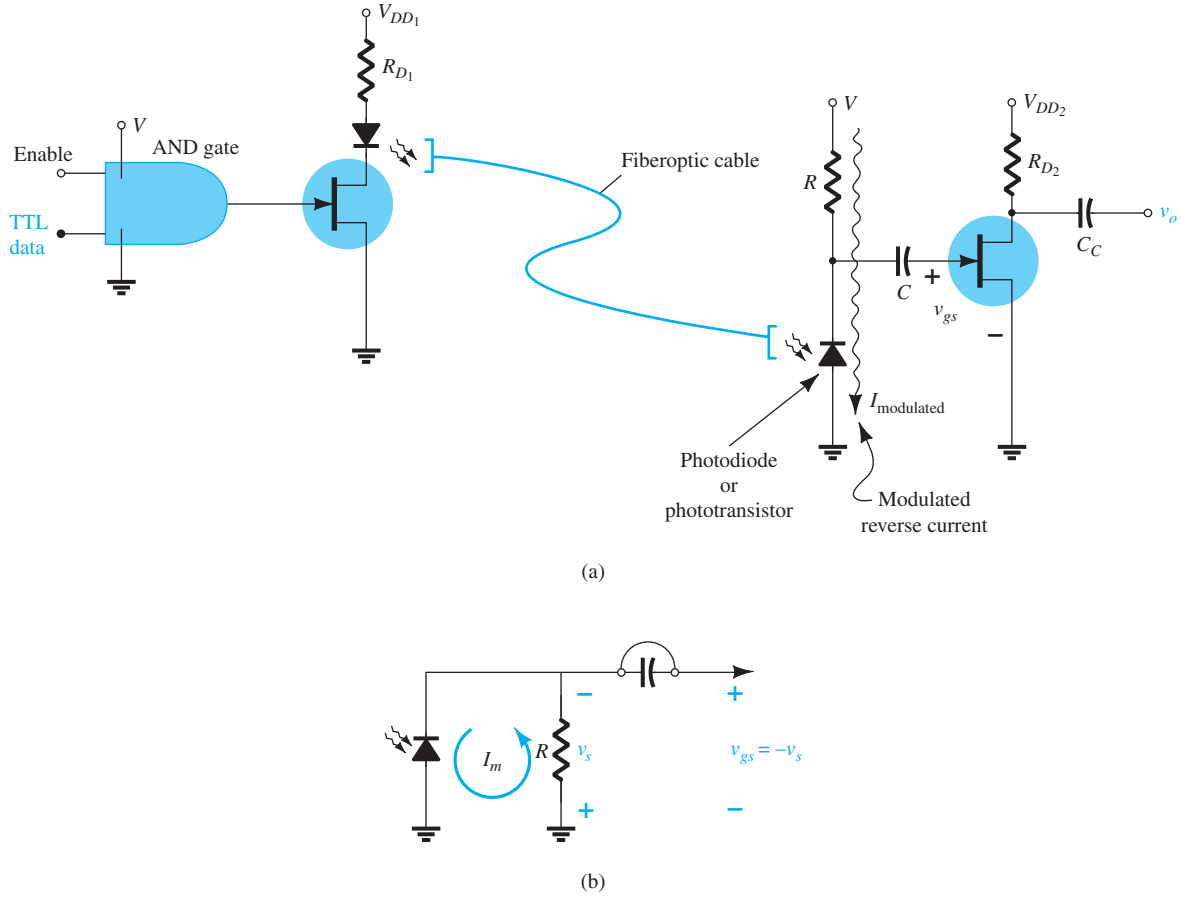


FIG. 7.70

TTL fiber optic communication channel: (a) JFET design; (b) passing on the signal generated across the photodiode.

at the high frequency of transmission. In fact, laser diodes are frequently used instead of LEDs in the modulator because they work at higher information rates and higher powers and have lower coupling and transmission losses. However, laser diodes are a great deal more expensive and more temperature sensitive, and they typically have a shorter lifetime than LEDs. For the demodulator side, the photodiodes are either of the pin photodiode or the avalanche photodiode variety. The *pin* abbreviation comes from the *p-i*ntrinsic-*n* construction process, and the term *avalanche* from the rapidly growing ionization process that develops during operation.

In general, the JFET is excellent for this application because of its high isolation at the input side and its ability to quickly "snap" from one state to the other due to the TTL input. At the output side the isolation blocks any effect of the demodulator sensing circuit from affecting the ac response, and it provides some gain for the signal before it is passed on to the next stage.

MOSFET Relay Driver

The MOSFET relay driver to be described in this section is an excellent example of how the FETs can be used to **drive high-current/high-voltage networks without drawing current or power from the driving circuit. The high input impedance of FETs essentially isolates the two parts of the network without the need for optical or electromagnetic linkages**. The network to be described can be used for a variety of applications, but our application will be limited to an alarm system activated when someone or something passes the plane of the transmitted light.

The IR (infrared—not visible) LED of Fig. 7.71 is directing its light through a directional funnel to hit the face of a photoconductive cell (Section 16.7) of the controlling network. The photoconductive cell has a range of resistance from about 200 kΩ as its dark

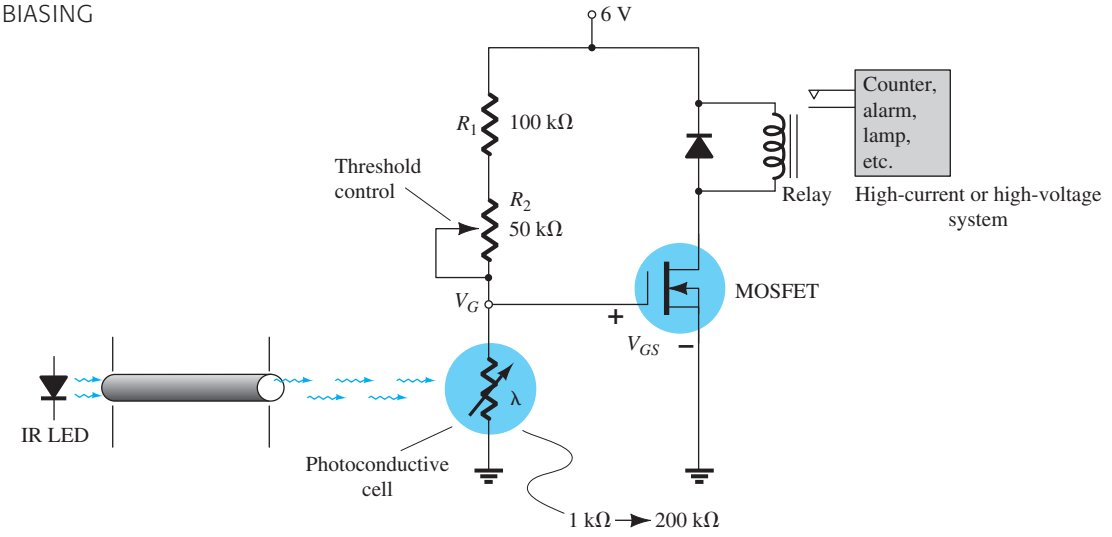


FIG. 7.71
MOSFET relay driver.

resistance level down to less than 1 kΩ at high illumination levels. Resistor R_1 is a variable resistance that can be used to set the threshold level of the depletion-type MOSFET. A medium-power MOSFET was employed because of the high level of drain current through the magnetizing coil. The diode is included as a protective device for reasons discussed in detail in Section 2.11.

When the system is on and the light consistently hitting the photoconductive cell, the resistance of the cell may drop to 10 kΩ. At this level an application of the voltage-divider rule will result in a voltage of about 0.54 V at the gate terminal (with the 50-kΩ potentiometer set to 0 kΩ). The MOSFET will be on, but not at a drain current level that will cause the relay to change state. When someone passes by, the light source will be cut off, and the resistance of the cell may quickly (in a few microseconds) rise to 100 kΩ. The voltage at the gate will then rise to 3 V, turning on the MOSFET and activating the relay and turning on the system under control. An alarm circuit has its own control design to ensure that it will not turn off when light returns to the photoconductive cell.

In essence, therefore, we have controlled a high-current network with a relatively small dc voltage level and a rather inexpensive design. The only obvious flaw in the design is the fact that the MOSFET will be on even when there is no intrusion. This can be remedied through the use of a more sophisticated design, but keep in mind that **MOSFETs are typically low-power-consumption devices**, so the power loss, even over time, is not that great.

7.16 SUMMARY

Important Conclusions and Concepts

1. A fixed-bias configuration has, as the label implies, a **fixed** dc voltage applied from gate to source to establish the operating point.
2. The **nonlinear** relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution (involving the solution of two simultaneous equations) be used to determine the quiescent point of operation.
3. All voltages with a single subscript define a voltage from a specified point to **ground**.
4. The self-bias configuration is determined by an equation for V_{GS} that will *always* pass through the origin. Any other point determined by the biasing equation will establish a **straight** line to represent the biasing network.
5. For the voltage-divider biasing configuration, one can always assume that the gate current is 0 A to permit an **isolation** of the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be **positive for an *n*-channel JFET** and **negative for a *p*-channel JFET. Increasing values of** R_S result in **lower quiescent values of** I_D and more **negative values of** V_{GS} **for an *n*-channel JFET**.

6. The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an I_D level **above** the I_{DSS} value.
7. The characteristics and method of analysis applied to enhancement-type MOSFETs are **entirely different** from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current is 0 A.
8. When analyzing networks with a variety of devices, first work with the region of the network that will provide a **voltage or current level** using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.
9. The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind, remember that a resistance level is defined by the **voltage across the resistor divided by the current** through the resistor. In the design process, both of these quantities are often available for a particular resistive element.
10. The ability to troubleshoot a network requires a **clear**, **firm understanding** of the terminal behavior of each of the devices in the network. That knowledge will provide an **estimate** of the working voltage levels of specific points of the network, which can be checked with a voltmeter. The ohmmeter section of a multimeter is particularly helpful in ensuring that there is a **true connection** between all the elements of the network.
11. The analysis of *p*-channel FETs is the same as that applied to *n*-channel FETs except for the fact that all the voltages will have the **opposite polarity** and the currents the **opposite direction**.

Equations

JFETs/depletion-type MOSFETs:

$$\text{Fixed-bias configuration: } V_{GS} = -V_{GG} = V_G$$

$$\text{Self-bias configuration: } V_{GS} = -I_D R_S$$

$$\text{Voltage-divider biasing: } V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

Enhancement-type MOSFETs:

$$\text{Feedback biasing: } V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$

$$\text{Voltage-divider biasing: } V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

7.17 COMPUTER ANALYSIS

PSpice Windows

JFET Voltage-Divider Configuration The results of Example 7.19 will now be verified using PSpice Windows. The network of Fig. 7.72 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL** library, and **Edit-PSpice model** is used to set **Beta** to 0.222 mA/V^2 and **Vto** to −6 V. The **Beta** value is determined using beta = I_{DSS}/V_P^2 Eq. (6.17) and the provided I_{DSS} and V_P. The results of the **Simulation** appear in Fig. 7.73 with the dc bias voltage and current levels. The resulting drain current is 4.225 mA, compared to the calculated level of 4.24 mA—an excellent match. The voltage V_{GS} is 3.504 V − 5.070 V = −1.57 V versus the calculated level of −1.56 V in Example 7.19—another excellent match.

Combination Network Next, the result of Example 7.12 with both a transistor and JFET will be verified. For the transistor **Bf** is set to 180, whereas for the JFET, **Beta** is set to 0.333 mA/V^2 and **Vto** to −6 V as called for in the example. The results for all the dc levels appear in Fig. 7.73. Note again the excellent comparison with the calculator solution, with V_D at 11.44 V compared to 11.07 V, $V_S = V_C$ at 7.138 V compared to 7.32 V, and V_{GS} at 3.380 V − 7.138 V = −3.76 V compared to −3.7 V.

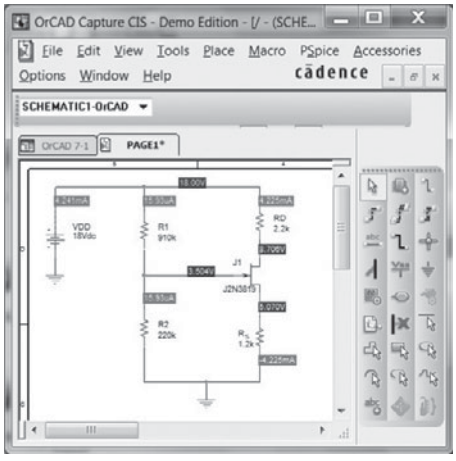


FIG. 7.72
JFET voltage-divider configuration with PSpice Windows results for current and voltage levels.

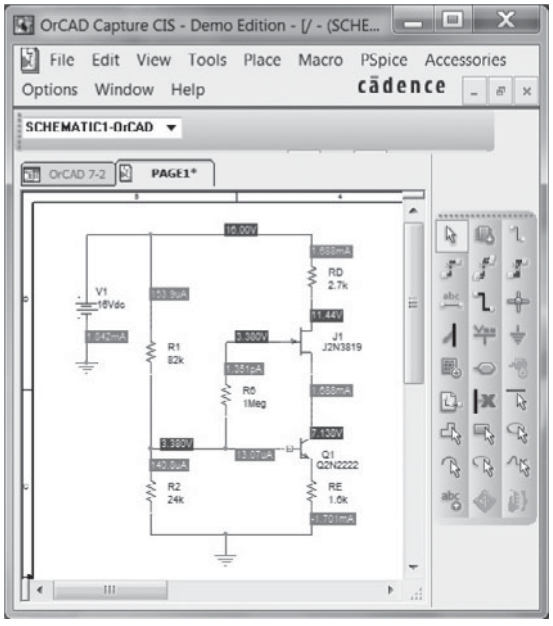


FIG. 7.73
Verifying the hand-calculated solution of Example 7.12 using PSpice Windows.

Multisim

The results of Example 7.2 will now be verified using Multisim. The construction of the network of Fig. 7.74 is essentially the same as applied in the BJT chapters. The JFET is obtained by selecting **Transistor**, the fourth key down on the first vertical toolbar. A **Select a Component** dialog box will appear, in which **JFET_N** can be selected under the **Family** listing. A long **Component** list appears, in which **2N3821** is selected for this application. An **OK**, and it can be placed on the screen. After double-clicking the symbol on the screen, a **JFET_N** dialog box will appear in which **Value** can be selected, followed

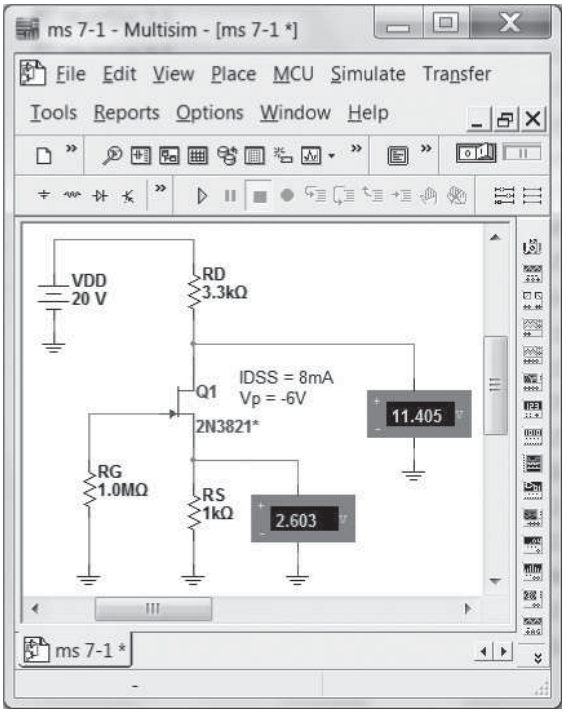


FIG. 7.74
Verifying the results of Example 7.2 using Multisim.

by **Edit Model**. An **Edit Model** dialog box will appear in which **Beta** and **Vto** can be set to **0.222 mA/V²** and **−6 V**, respectively. The value of **Beta** is determined using Eq. (6.17) and the parameters of the network as follows:

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{8\text{ mA}}{|-6\text{ V}|^2} = \frac{8\text{ mA}}{36\text{ V}^2} = 0.222\text{ mA/V}^2$$

Once the change is made, be sure to select **Change Part Model** before leaving the dialog box. The **JFET_N** dialog box will appear again, but an **OK**, and the changes will be made. The labels **IDSS = 8 mA** and **Vp = −6 V** are added using **Place-Text**. A blinking vertical bar will appear marking the place where the label can be entered. Once entered, it can easily be moved by simply clicking the area and dragging it to the desired position while holding the clicker down.

Using the **Indicator** option on the first vertical toolbar displays the drain and source voltages as shown in Fig. 7.74. In both cases the **VOLTMETER_V** option was chosen in the **Select a Component** dialog box.

Selecting **Simulate-Run** or moving the switch to the **1** position results in the display of Fig. 7.74. Note that V_{GS} at −2.603 V is an exact match with the hand-calculated solution of −2.6 V. Although the indicator is connected from source to ground, be aware that this is also the gate-to-source voltage because the voltage drop across the 1-MΩ resistor is assumed to be 0 V. The level of 11.405 V at the drain is very close to the hand-calculated solution of 11.42 V—in all, a complete verification of the results of Example 7.2.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.75:
   - **a.** Sketch the transfer characteristics of the device.
   - **b.** Superimpose the network equation on the same graph.
   - **c.** Determine I_{D_Q} and V_{DS_Q}.
   - **d.** Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

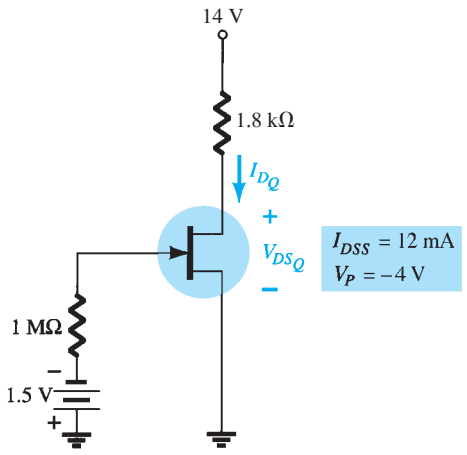


FIG. 7.75
Problems 1 and 37.

2. For the fixed-bias configuration of Fig. 7.76, determine:
   - **a.** I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
   - **b.** Repeat part (a) using a graphical approach and compare results.
   - **c.** Find V_{DS}, V_D, V_G, and V_S using the results of part (a).
3. Given the measured value of V_D in Fig. 7.77, determine:
   - **a.** I_D.
   - **b.** V_{DS}.
   - **c.** V_{GG}.

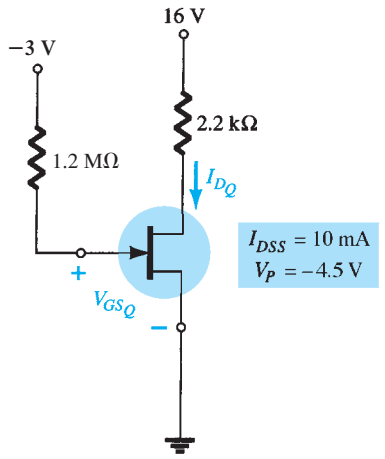


FIG. 7.76
Problem 2.

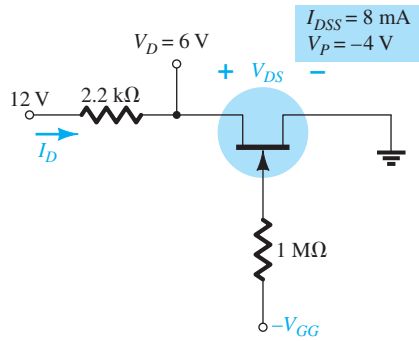


FIG. 7.77
Problem 3.

4. Determine V_D and V_{GS} for the fixed-bias configuration of Fig. 7.78.

5. Determine V_D and V_{GS} for the fixed-bias configuration of Fig. 7.79.

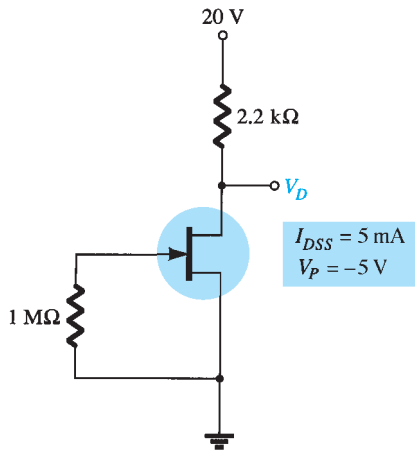


FIG. 7.78
Problem 4.

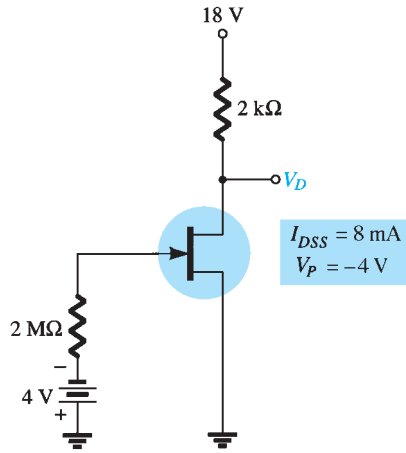


FIG. 7.79
Problem 5.

7.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 7.80:
- **a.** Sketch the transfer curve for the device.
- **b.** Superimpose the network equation on the same graph.
- **c.** Determine I_{D_Q} and V_{GS_Q}.
- **d.** Calculate V_{DS}, V_D, V_G, and V_S.

***7.** Determine I_{D_Q} for the network of Fig. 7.80 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 7.81, determine:
- **a.** V_{GS_Q} and I_{D_Q}.
- **b.** V_{DS}, V_D, V_G, and V_S.

9. Given the measurement $V_S = 1.7$ V for the network of Fig. 7.82, determine:
- **a.** I_{D_Q}.
- **b.** V_{GS_Q}.
- **c.** I_{DSS}.
- **d.** V_D.
- **e.** V_{DS}.

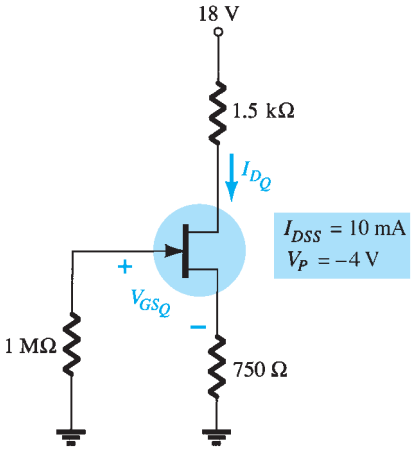


FIG. 7.80
Problems 6, 7, and 38.

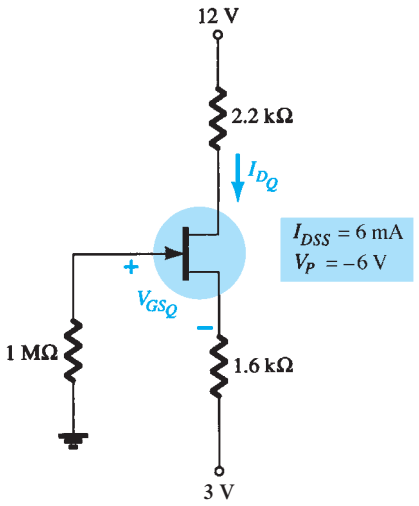


FIG. 7.81
Problem 8.

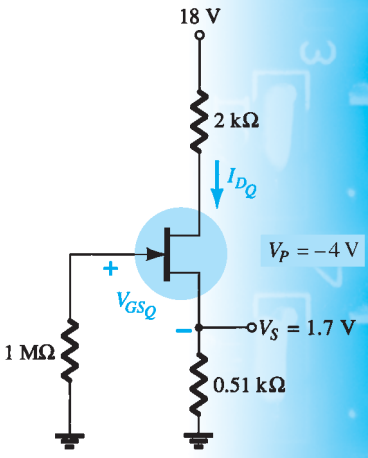


FIG. 7.82
Problem 9.

***10.** For the network of Fig. 7.83, determine:
- **a.** I_D.
- **b.** V_{DS}.
- **c.** V_D.
- **d.** V_S.

***11.** Find V_S for the network of Fig. 7.84.

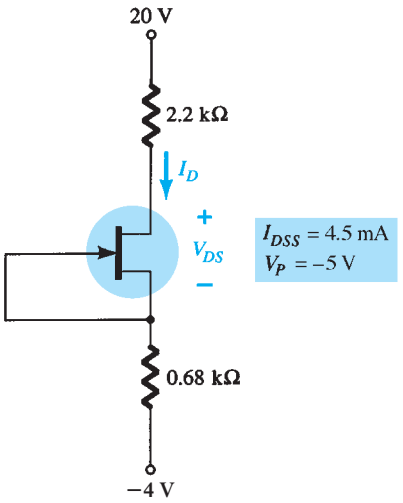


FIG. 7.83
Problem 10.

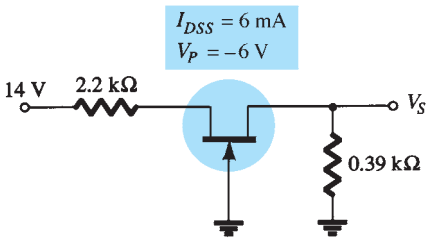


FIG. 7.84
Problem 11.

7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.85, determine:
- **a.** V_G.
- **b.** I_{D_Q} and V_{GS_Q}.
- **c.** V_D and V_S.
- **d.** V_{DS_Q}.

13. **a.** Repeat Problem 12 with $R_S = 0.51\,\text{k}\Omega$ (about 50% of the value of that of Problem 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
- **b.** What is the minimum possible value of R_S for the network of Fig. 7.85?

14. For the network of Fig. 7.86, $V_D = 12$ V. Determine:
- **a.** I_D.
- **b.** V_S and V_{DS}.
- **c.** V_G and V_{GS}.
- **d.** V_P.

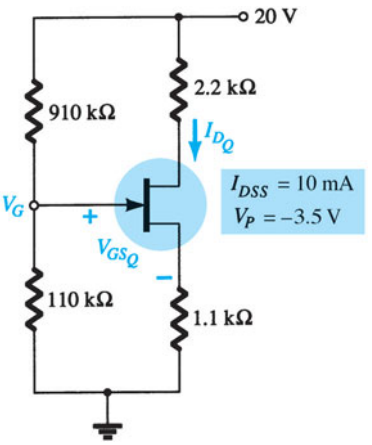


FIG. 7.85
Problems 12 and 13.

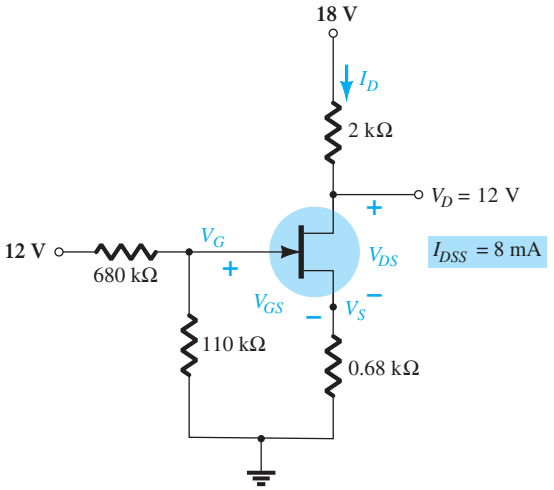


FIG. 7.86
Problem 14.

15. Determine the value of R_S for the network of Fig. 7.87 to establish $V_D = 10$ V.

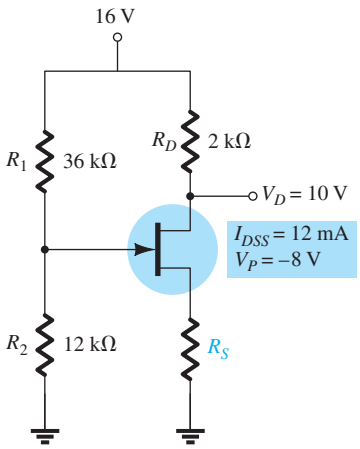


FIG. 7.87
Problem 15.

7.5 Common-Gate Configuration

***16.** For the network of Fig. 7.88, determine:

a. I_{D_Q} and V_{GS_Q}.

b. V_{DS} and V_S.

***17.** Given $V_{DS} = 4$ V for the network of Fig. 7.89, determine:

a. I_D.

b. V_D and V_S.

c. V_{GS}.

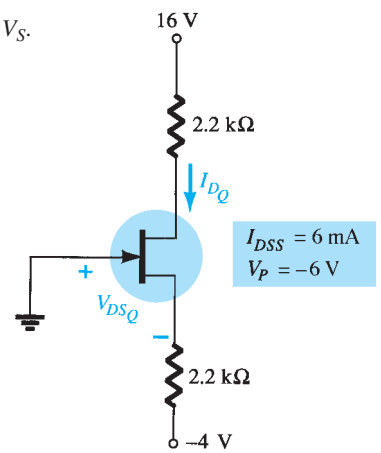


FIG. 7.88
Problems 16 and 39.

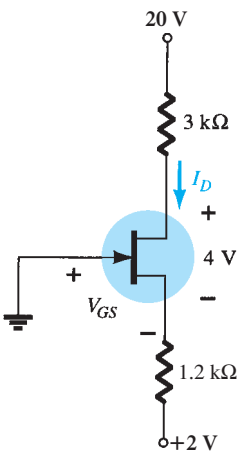


FIG. 7.89
Problem 17.

7.6 Special Case: $V_{GS_Q} = 0$ V

18. For the network of Fig. 7.90.
- **a.** Find I_{D_Q}.
- **b.** Determine V_{D_Q} and V_{DS_Q}.
- **c.** Find the power supplied by the source and dissipated by the device.

19. Determine V_D and V_{GS} for the network of Fig. 7.91 using the provided information.

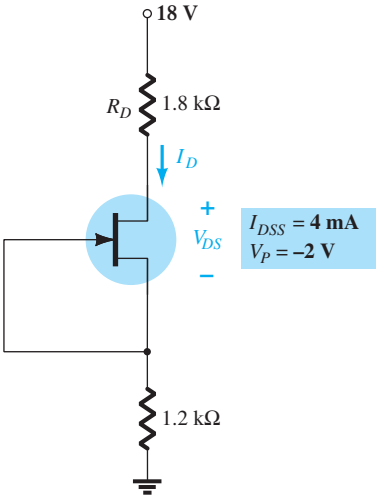


FIG. 7.90
Problem 18.

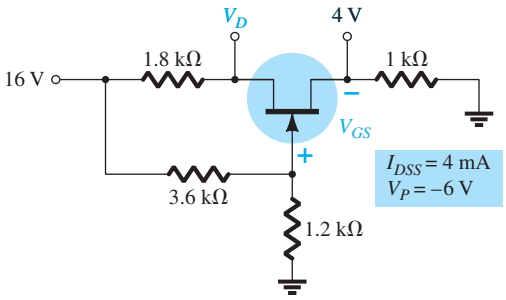


FIG. 7.91
Problem 19.

7.7 Depletion-Type MOSFETs

20. For the self-bias configuration of Fig. 7.92, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS} and V_D.

***21.** For the network of Fig. 7.93, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS} and V_S.

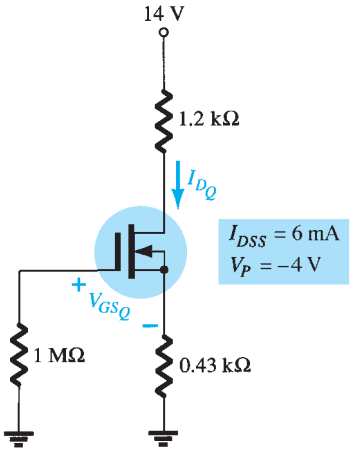


FIG. 7.92
Problem 20.

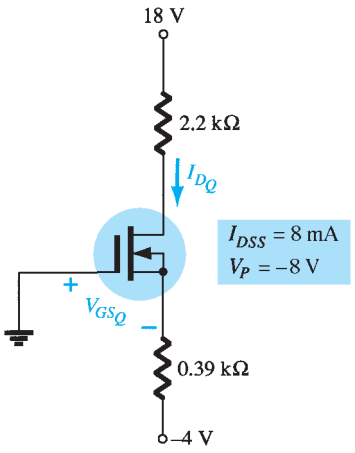


FIG. 7.93
Problem 21.

7.8 Enhancement-Type MOSFETs

22. For the network of Fig. 7.94, determine:
- **a.** I_{D_Q}.
- **b.** V_{GS_Q} and V_{DS_Q}.
- **c.** V_D and V_S.
- **d.** V_{DS}.

23. For the voltage-divider configuration of Fig. 7.95, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_D and V_S.

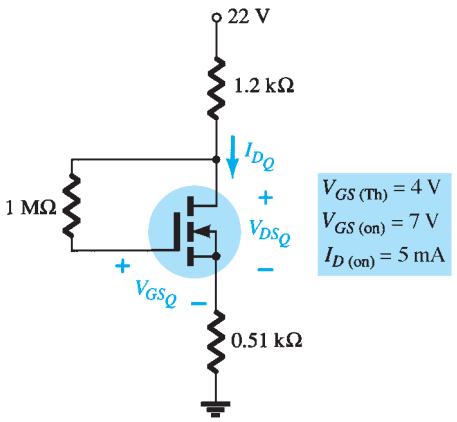


FIG. 7.94
Problem 22.

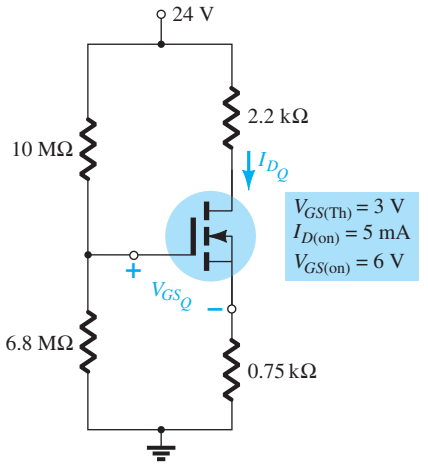


FIG. 7.95
Problem 23.

7.10 Combination Networks

***24.** For the network of Fig. 7.96, determine:

a. V_G.
b. V_{GS_Q} and I_{D_Q}.
c. I_E.
d. I_B.
e. V_D.
f. V_C.

***25.** For the combination network of Fig. 7.97, determine:

a. V_B and V_G.
b. V_E.
c. I_E, I_C, and I_D.
d. I_B.
e. V_C, V_S, and V_D.
f. V_{CE}.
g. V_{DS}.

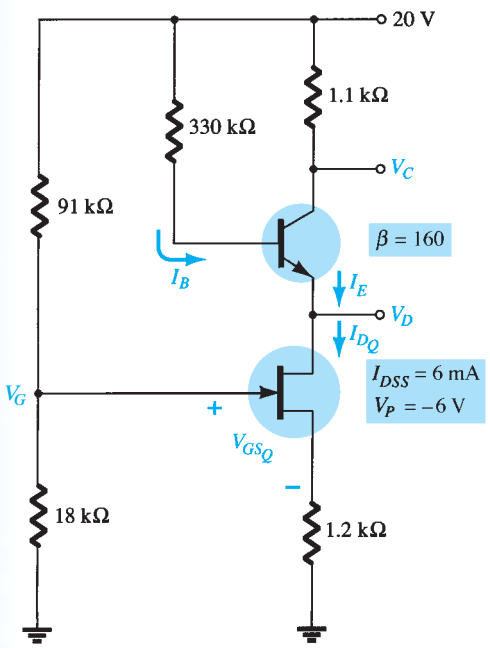


FIG. 7.96
Problem 24.

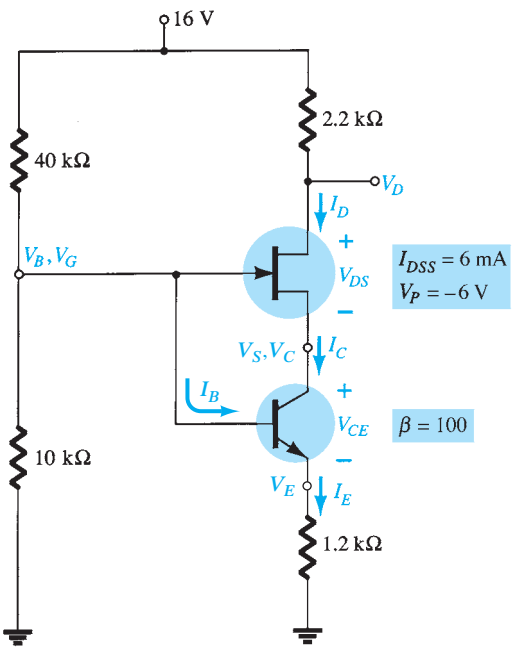


FIG. 7.97
Problem 25.

7.11 Design

*26. Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

*27. Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22\ \text{M}\Omega$. Use standard values.

28. Design a network such as appears in Fig. 7.39 using an enhancement-type MOSFET with $V_{GS(\text{Th})} = 4$ V and $k = 0.5 \times 10^{-3}\ \text{A/V}^2$ to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

7.12 Troubleshooting

*29. What do the readings for each configuration of Fig. 7.98 suggest about the operation of the network?

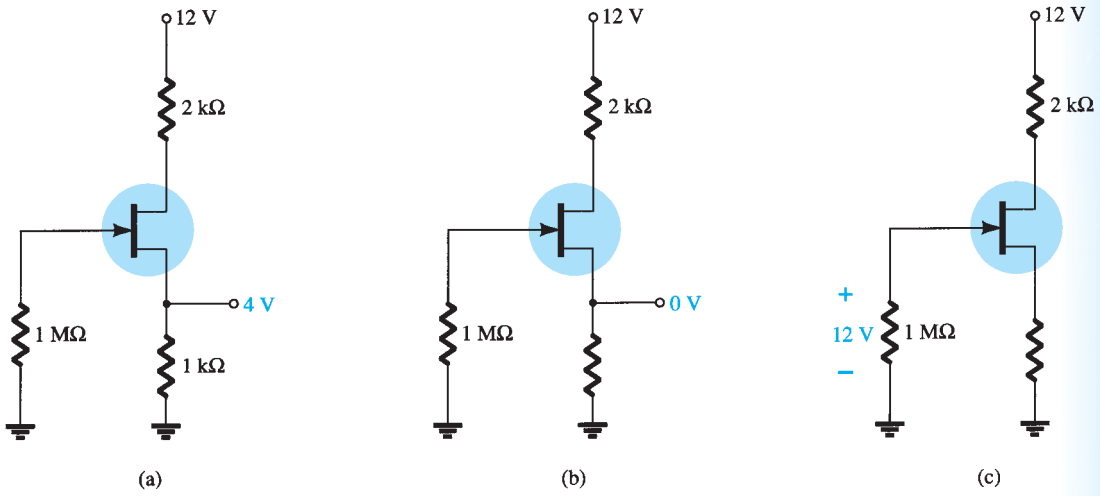


FIG. 7.98
Problem 29.

*30. Although the readings of Fig. 7.99 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

*31. The network of Fig. 7.100 is not operating properly. What is the specific cause for its failure?

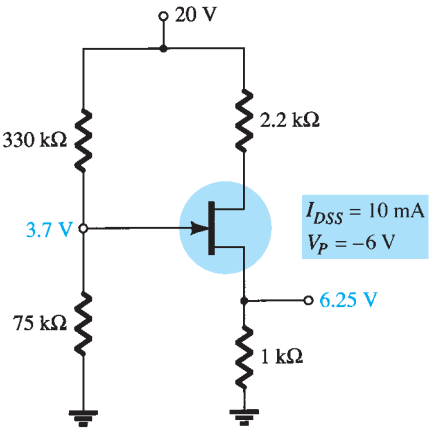


FIG. 7.99
Problem 30.

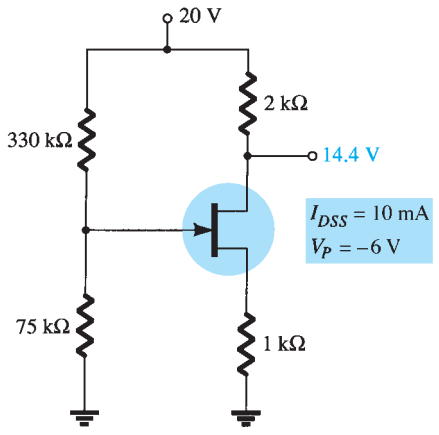


FIG. 7.100
Problem 31.

7.13 *p*-Channel FETs

32. For the network of Fig. 7.101, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS}.
- **c.** V_D.

33. For the network of Fig. 7.102, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS}.
- **c.** V_D.

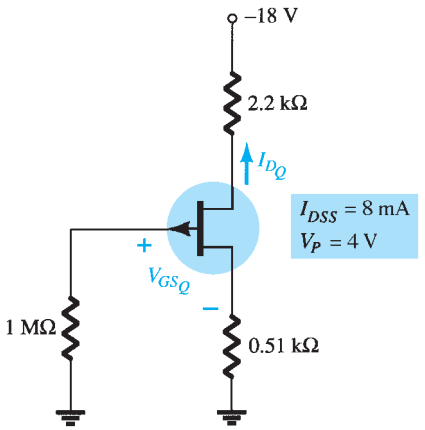


FIG. 7.101
Problem 32.

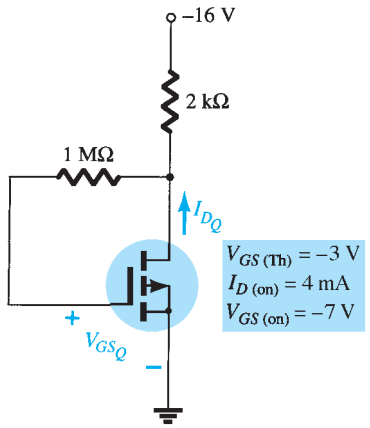


FIG. 7.102
Problem 33.

7.14 Universal JFET Bias Curve

34. Repeat Problem 1 using the universal JFET bias curve.

35. Repeat Problem 6 using the universal JFET bias curve.

36. Repeat Problem 12 using the universal JFET bias curve.

37. Repeat Problem 16 using the universal JFET bias curve.

7.15 Computer Analysis

38. Perform a PSpice Windows analysis of the network of Problem 1.

39. Perform a PSpice Windows analysis of the network of Problem 6.

40. Perform a Multisim analysis of the network of Problem 16.

41. Perform a Multisim analysis of the network of Problem 33.