Title: AI Powered EDA Tools: Current Trends and Future Directions

1.Introduction

Importance of EDA for modern chip complexity

Motivation for AI in EDA

Overview of paper goals and scope

2.Background: Classical EDA Flow and AI Basics

Overview of digital design steps: specification → RTL → synthesis → placement & routing → verification

Key bottlenecks in traditional EDA

Basic AI/ML concepts relevant for EDA: supervised learning, reinforcement learning, graph neural networks (GNNs)

3.AI for Digital Physical Design

AI in placement and floor planning (RL-based methods)

Congestion and routing prediction using ML

Timing and power estimation

Benefits of AI in improving speed and quality

4.Graph Based Models and Open Datasets

Circuits/netlists as graphs and role of GNNs

Importance of public datasets (e.g., CircuitNet)

Benchmarks like ChiPBench for end to end evaluation

5.AI for Verification and High-Level Design

ML to accelerate functional verification (test ranking, failure prediction)

Generative AI (LLMs) for RTL and script generation

Challenges of correctness and reliability

6.AI for Analog and Mixed-Signal Design

Complexity and challenges in analog design

ML based surrogate models and optimization

RL and evolutionary algorithms for device sizing

7.Challenges and Future Directions

Data scarcity and generalization

Trust, explainability, and integration issues

Vision for AI-native EDA and tighter AI-tool synergy

Need for better datasets and benchmarks

8.Conclusion

Summary of AI benefits and current uses in EDA

Remaining challenges and research needs

Importance of AI knowledge for future hardware engineers

Outlook on AI-native EDA impact