Hardware Review Report

Version 1.0
Espressif Systems

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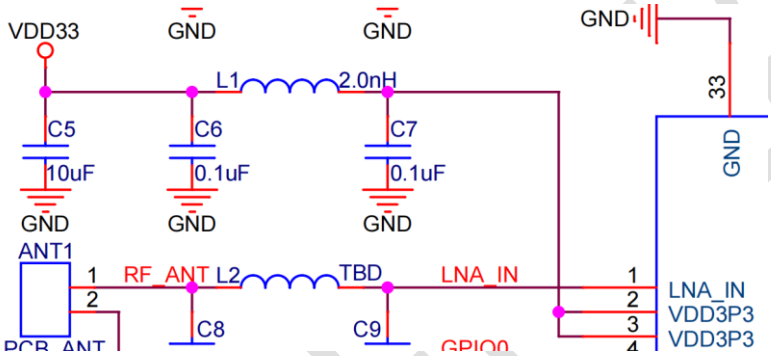
1. Schematics

1.1. Power and Ground

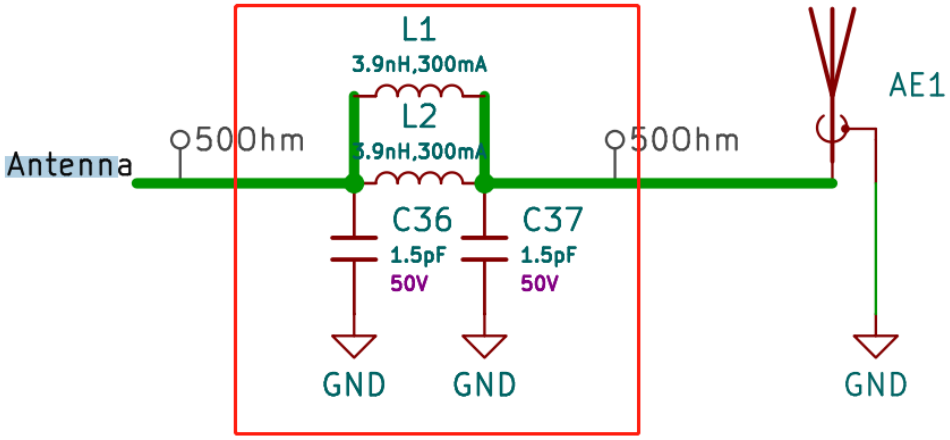
a. Please make sure the power supply current for ESP32-C3 is not less than 500 mA.

b. Please refer to the circuit below to draw circuit at pin 2,3.



1.2. RF

a. Please note this CLC is to tune C3 and it should be placed close to C3. But one inductor is enough, please remove one inductor.



b. At the same time, to ensure radiation performance, please add another CLC at antenna side.

c. Please note that the matching values need to be confirmed after actual testing.

d. It is suggested to add an ESD diode close to antenna.

1.3. Clock

a. Please note that the final values of the series inductor and the capacitance on both sides of crystal will be confirmed after actual testing.

b. The accuracy of the 40 MHz crystal is recommended to be at least ± 10 ppm at room temperature.

1.4. Reset/Enable

a. Please note that the power-up/down sequence in the data sheet is the sufficient condition for a successful boot-up, so it is suggested to tune RC values referred to the figure below.

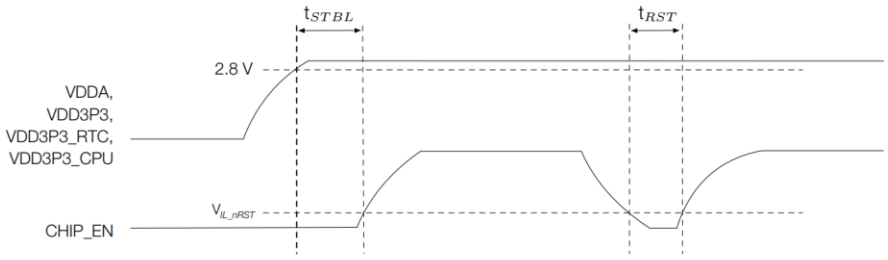
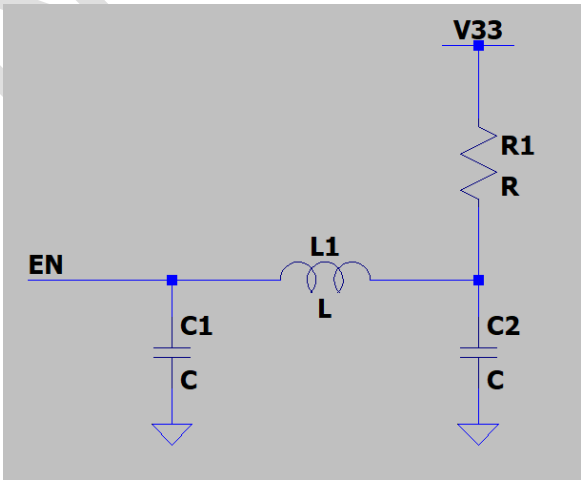


Figure 2-4. Visualization of Timing Parameters for Power-up and Reset

Table 2-8. Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDA, VDD3P3, VDD3P3_RTC, and VDD3P3_CPU to stabilize before the CHIP_EN pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_EN to stay below V_{IL_nRST} to reset the chip (see Table 4-4)	50

b. It is suggested to add another CL before RC to optimize EMC performance. The capacitor is close to the CHIP_EN pin. There is no need to install it first. Use a 0 Ω resistor for the inductor.



c. If the power supply in the application is slow or requires frequent power on and off or the power supply is not stable enough, RC alone may not be able to meet the needs. Please reserve a reset chip

or watchdog chip to ensure that the chip can be reset by hardware in case of an abnormality. It is recommended that the threshold value of the reset chip be selected around 3.0 V. Or you can place a reset button, or use other MCU to control the reset pin.

1.5. Sleep/Wake up

a. If there is need to wake up from sleep or work in sleep mode, please choose RTC GPIO.

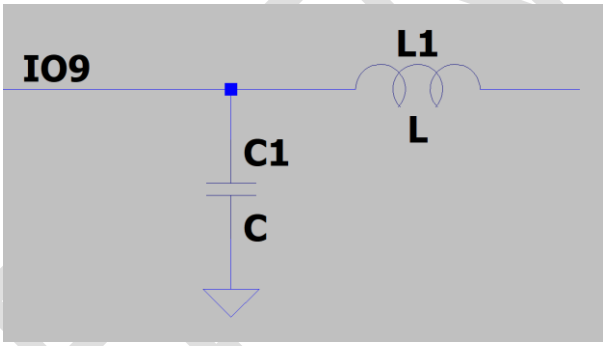
1.6. External RC

a. NA

1.7. I/O

a. Please confirm that the GPIO input of ESP32-C3 does not exceed 3.6 V.

b. It is suggested to add a CL to GPIO9 close to the chip to optimize EMC performance. The capacitor is close to the GPIO9 pin. There is no need to install components first. Use a 0 Ω resistor for the inductor.



1.8. Flash/PSRAM

a. NA

1.9. UART

a. OK

1.10. Package

a. OK

1.11. Others

a. NA

2. PCB

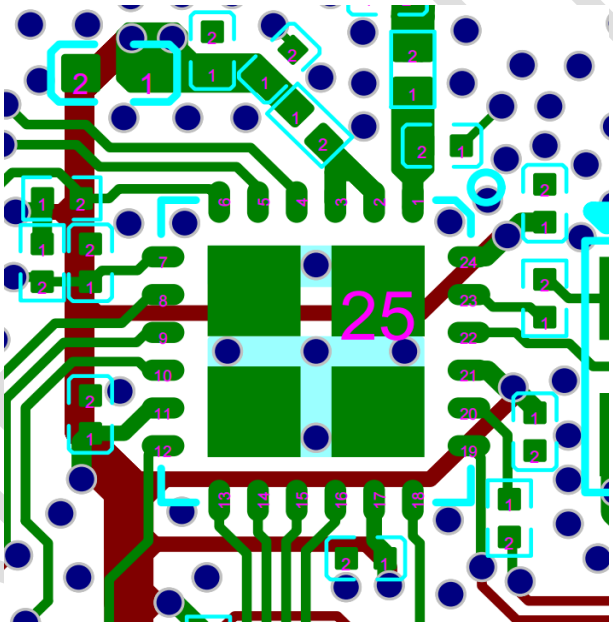
2.1. PCB Check

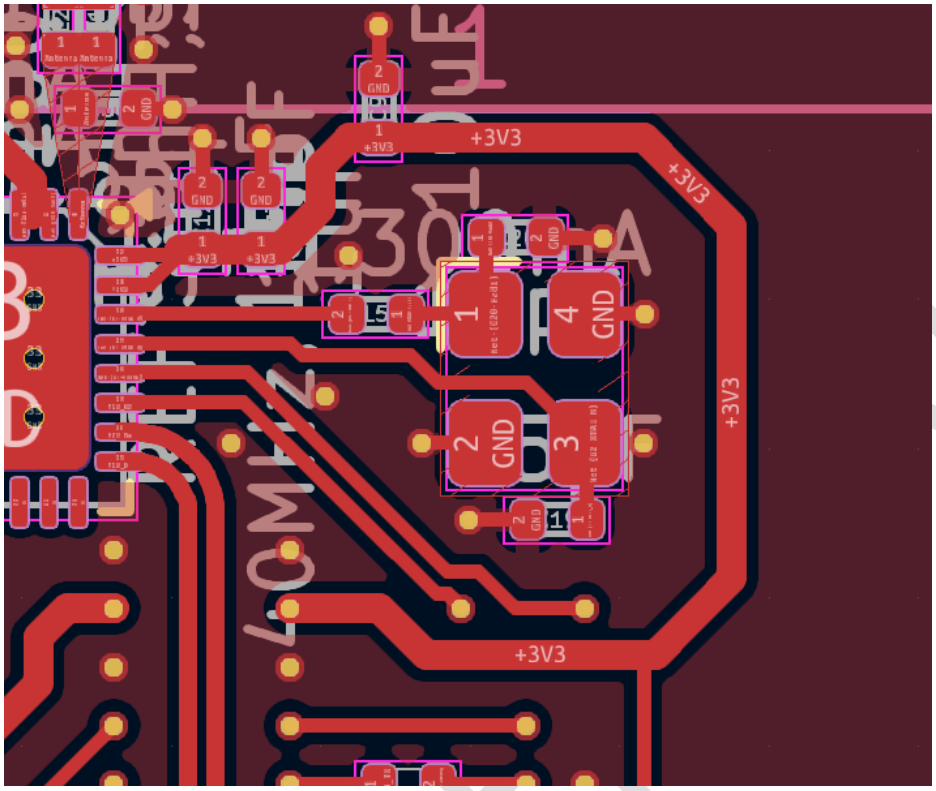
a. FR4 material is recommended for PCB board.

b. It is preferred to use four-layer board.

2.2. Power and Ground

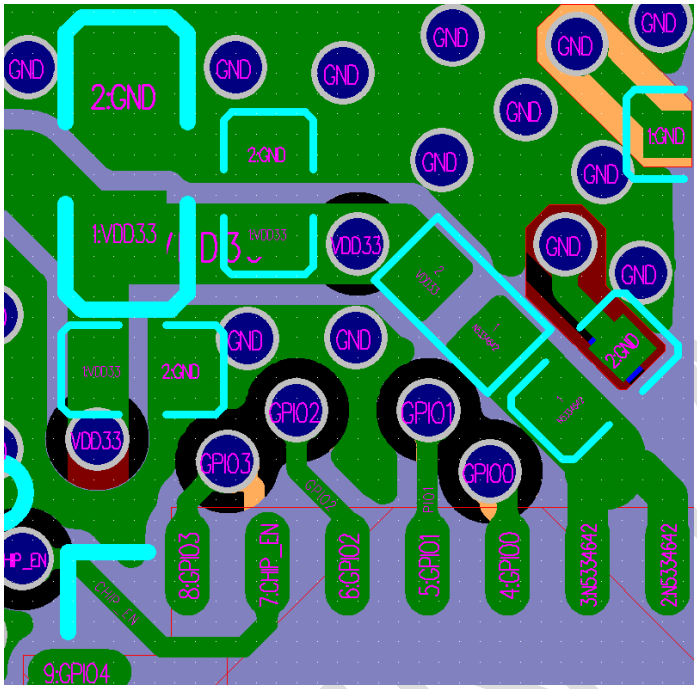
a. Please route power traces on the bottom layer like this way in the figure below to avoid routing power traces around the crystal.



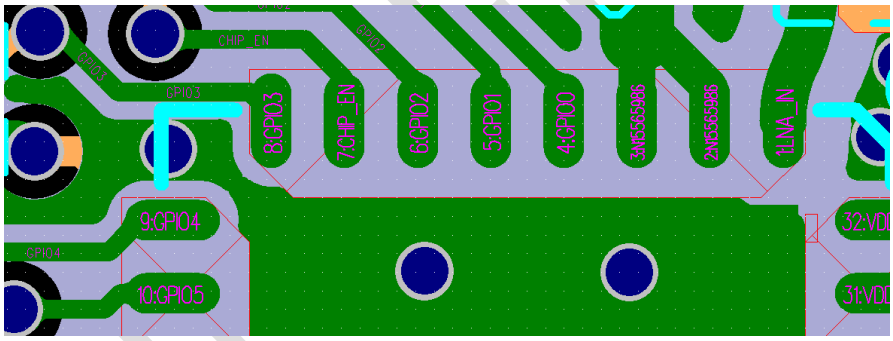


b. Except for the power traces of pins 2 and 3, which need to be at least 15 mil, the width of other power pins traces only needs to be 10 mil. Pay attention to the good grounding around the power traces.

c. Pins 2 and 3 can be routed at a 45-degree angle, and the RF routing next to them could be routed at a 45-degree angle toward the other side, and the distance between the two can be increased. Please use 0201 footprint as minimum footprint, then please place the power circuits of pins 2 and 3 closer to the pins and surround these power traces with enough ground. After using 0201, you can add stub traces on the first capacitor to bottom layer to suppress harmonics.



d. It is recommended to connect the EPAD to outside ground copper.

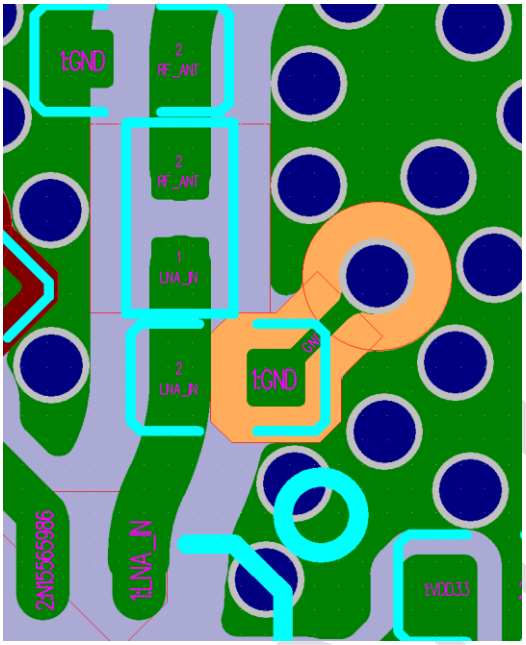


e. The components are suggested to connect ground in the flood over way not in the diagonal way.

2.3. RF

a. Please note that all RF traces should have 50 ohms impedance control in process. Please note the width could not vary, this will affect the impedance control.

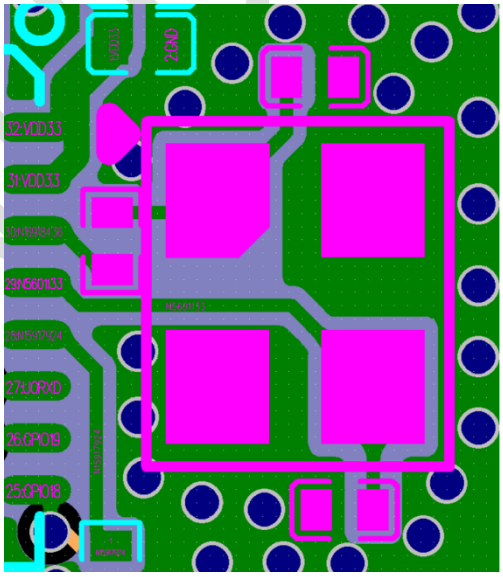
b. Please use CLC with one inductor to tune C3. Please use 0201 matching components and place them close to the pin. Please place CLC in a Z shape, that is, the two capacitors should not face in the same direction to reduce mutual interference. Please add a stub trace at the first capacitor to suppress high-frequency harmonics. The impedance of the stub trace is about 100 Ω ± 10 %.



c. Please note that PCB antenna needs to be tested by simulation and actual board. Please add another CLC close to antenna.

2.4. Clock

a. Please place the series component close to the ESP32-C3 chip pins. Please add more ground via around crystal and do not route power traces around the crystal.



2.5. Reset/Enable

a. Please place RC close to the CHIP_EN pin.

2.6. External RC

a. NA

2.7. I/O

a. Please place the RC circuit reserved on the USB line close to the ESP32-C3 chip side.

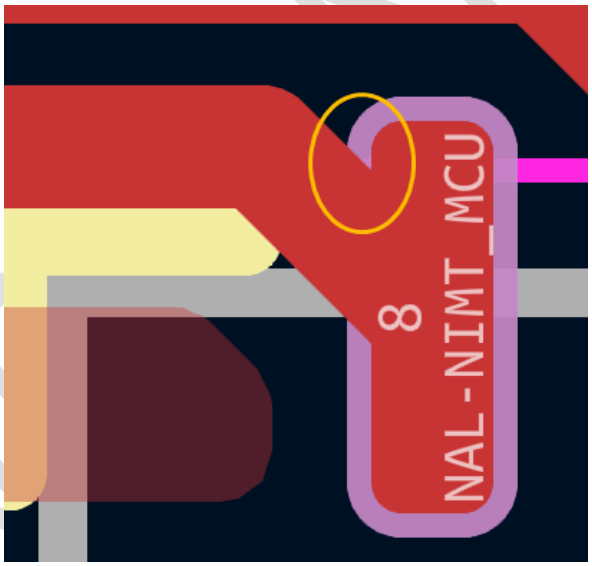
2.8. UART Layout

a. Please place the 499 Ω resistor in series close to the U0TXD pin.

b. Please reduce the length of the UART0 trace on the top layer as much as possible, and surround the ground around them.

2.9. Others

a. Please check the entire board and avoid acute angles for traces.



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