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Multi-dimensional grids/blocks, coalescence

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Objectives

- Use the indexing of grids/blocks 2 or 3 dims Realize
- "fast" access the global memory of the GPU First TP on
- matrix multiplication



Outline

- Multi-dimensional indexing of blocks and threads
- Coalescence
- Practical: Multiplication of matrices



Outline

- Multi-dimensional indexing of blocks and threads
- Coalescence
- Practical: Multiplication of matrices

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Multiplication of an array 3D by blocks

Recapultative of the example of the multiplication of an array by blocks

```
#include < cstdio>
# include" cuda b'
# define N 1024
float A [ N 1 :
float c = 2.0:
__d e v i c e_float dA [ N ] :
-- globa-l-widmultiplyArray(intn,floatc)
  inti = blockldx.x:
  dA[i] * = c:
int main (int arg c, char * * a r g v)
  for (int i = 0 : i < N : i + +) { A [i] = i : }
  // Copy the table to the GPU
  cudaMemcpyToSymbol (dA, A, N * sizeof (float), 0,
       cuda Memcpy HostTo Device ):
  multiplyArray <<< N.1>>> (N.c):
  // Copy the array multiplies to the CPU
  cudaMemcpvFromSymbol (A, dA, N * sizeof ( float ) , 0 ,
       cuda Memcov Device To Host ) :
  return 0:
```

- Multiply a 1D array by a grid of blocks.
- Each block multiplies 1 element. Run
- the kernel with N blocks.
- **Question:** What would happen if the etait plut ot AIMIM?



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Multiplying a 2D array by blocks

Multiply each element of an array A[N][N] by a scalar c

```
#include < cstdio>
# include" cuda . h'
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e vice float dA [N][N]:
-- globa-l-widmultiplyArray2D(intn,floatc)
  int i = blockldx.x/n:
  int i = blockldx.x% n:
  dA[i][i] * = c:
int main (int arg c, char * * a r g v)
  // Initialization
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) \{ A[i][j] = i + j; \}
  // Copy the table to the GPU
  cudaMemcpvToSymbol (dA , A, N * N * sizeof (float) , 0 ,
       cuda Memcov HostTo Device ) :
  multiply Array 2 D <<< N * N, 1>>> (N, c);
  // Copy the array multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA , N * N * sizeof (float), 0,
       cuda Memcov Device To Host ) :
  printf("%f\n", A[1][2]);
```

Each block multiplies 1 element.

- You have to throw N2 blocks in
- total.
- Every N consecutive blocks multiply a line of A.

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A division and a modulus to find *i* and *j*



```
#include < cstdio>
# include" cuda . h'
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e vice float dA [N][N]:
__globa_l_widmultiplyArray2D(intn.floatc)
  dA[blockidx.x][blockidx.y]
int main (int arg c. char * * a r g v)
  for (int i = 0; i < N; i + +) {
{ // Initialization
     for (int i = 0 : i < N : i + +) { A [i1[i] = i + i : }
  // Copy the table to the GPU
  cudaMemcpyToSymbol (dA, A, N * N * sizeof (float), 0,
       cuda Memcpy HostTo Device );
  dim3 d i m Gr i d :
  dim Grid.x = N
  dim Grid.y = N;
  dim Grid.z = 1:
  multiplyArray2D <<< dim Grid.1>>> (N.c):
  // Copy the array multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA , N * N * sizeof (float), 0,
       cuda Memcov Device To Host ) :
  printf("%f\n", A[11[21):
  return 0;
```

- dim3 defines a 3D indexing topology (dim3.{x,y,z}).
- Set **dim3.z = 1** for 2D.
 The total number of blocks is equal **t**he
- multiplication of dimensions.
- No division or modulus to find i and j





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e vice float dA [N][N]:
-- globa-l-widmultiplyArray2D(intn,floatc)
  int i = blockldx.x;
  int j = blockldx.y * block Dim.x + threadIdx.x;
  if(j < n) \{ dA[i][j] * = c; \}
int main (int argc. char * * argv)
  // Initialization
  for (int i = 0; i < N; i + +) {
     for (int i = 0 : i < N : i + +) { A [i1[i] = i + i : }
  // Copy the table to the GPU
  cudaMemcpyToSymbol (dA, A, N * N * sizeof (float), 0,
       cuda Memcov HostTo Device ) :
  int b l o c k S i z e = 1 0 2 4 :
  dim3 d i m Gr i d:
  dim Grid.x = N:
  dim Grid.y = N / block Size;
  dim Grid.z = 1;
  multiply Array 2 D <<< dim Grid, block Size >>> (N, c);
  cudaMemcpvFromSvmbol (A, dA , N * N * sizeof (float), 0,
       cuda Memcov Device To Host ) :
  printf("%f\n", A[11[21):
  return 0;
```

- Each block multiplies blockSize elements. Each
- thread multiplies 1 element.
- Threads work on consecutive elements in a line.
- You have to run N2/blockSize blocks in
- total. Each block multiplies a subline of A.
 - Check the overflow of the array.





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e vice float dA [N][N]:
  int j = blockldx.y;
  if (i < n) { dA [i][j] * = c; }
int main (int argc. char * * argv)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) \{ A[i][j] = i + j; \}
  // Copy the table to the GPU
  cudaMemcpyToSymbol ( dA , A, N * N * sizeof ( float ) , 0 ,
       cuda Memcov HostTo Device ) :
  int b l o c k S i z e = 1 0 2 4 :
  dim3 d i m Gr i d :
  dim Grid.x = N / blockSize
  : dim Grid. v = N:
  dim Grid.z = 1;
  multiplyArray2D <<< dim Grid.blockSize>>> (N.c)
  // Copy the array multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA , N * N * sizeof (float), 0,
       cuda Memcov Device To Host ) :
  printf("%f\n", A[1][2]);
  return 0;
```

- Each thread multiplies 1 element.
- It is necessary to launch N2/blockSize blocks
- in total. Threads work on consecutive elements in a **column**.
- Each block multiplies a sub-column of A.
- Which is better (subline vs. subcolumn)?
- What happens if A has few rows/columns?





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A[N][N]:
float c = 2.0:
__d e vice float dA [N][N]:
__global_widmultiplyArray2D(intn.floatc)
  int block Dim Sqrt = (int) sqrt((float) block Dim.x);
  inti = blockldx.x * block Dim Sgrt + threadIdx.x / block Dim Sgr
  intj = blockIdx.y * blockDimSqrt+threadIdx.x%blockDimSq
  if (i < n && j < n) { dA [i][j] * = c; }</pre>
int main (int arg c, char * * a r g v)
  for (int i = 0; i < N; i + +) {
     for (int i = 0 : i < N : i + +) { A [i1[i] = i + i : }
  // Copy the table to the GPU
  cudaMemcpvToSvmbol ( dA , A, N * N * sizeof ( float ) , 0 ,
       cuda Memcov HostTo Device ) :
  int block Size = 1024:
  dim3 d i m Gr i d :
  d i m Gr i d . x = N / 3 2 :
  d i m Gr i d . v = N / 3 2
  dim Grid z = 1:
Copy the amaymultiplies to the CPU
  ENGLAMETROS AS AS AS AS IN Grid NO LOCK SIZING TO SIN (N. S) :
       cuda Memcov Device To Host )
  printf("%f\n", A[11[21);
  return 0 :
```

- Distribute 1024 threads in 2D.
- Each block takes care of one
 - 32×32 sub-matrix.
- Threads consecutifs is working on a subline.
- Finding i and j does not require division and modulus.



```
#include < cstdio>
# include" cuda . h
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e v i c e float dA [ N ] [ N ] ;
-- globa-l-widmultiplyArray2D(intn,floatc)
  int block Dim Sqrt = (int) sqrt ((float) block Dim.x);
  int i = blockldx.x * block Dim Sqrt + threadIdx.x % block Dim Sqrt
  ; int j = blockIdx.y * blockDimSqrt+threadIdx.x/blockDimSqrt
  ; if (i < n && j < n) { dA[i][j] * = c;}
int main (int arg c. char * * a r g v)
  // Initialization
  for (int i = 0; i < N; i + +) {
    for (int j = 0; j < N; j ++) \{ A[i][j] = i + j; \}
  // Copy the table to the GPU
  cudaMemcpvToSymbol ( dA , A, N * N * sizeof ( float ) , 0 ,
       cuda Memcov HostTo Device ) :
  int block Size = 1024:
  dim3 d i m Gr i d :
  d i m Gr i d . x = N / 3 2 :
  d i m Gr i d . v = N / 3 2 :
  dim Grid.z = 1:
  multiplyArray2D <<< dim Grid, blockSize >>> (N, c):
  // Copy the array multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA , N * N * sizeof (float), 0,
       cuda Memcov Device To Host ) :
  printf("%f\n", A[11[21):
  return 0 :
```

- Distribute 1024 threads in 2D.
- Each block takes care of a 32 × 32 sub-matrix.
- Threads consecutifs is working on a sub-column.
- Finding i and j does not require division and modulus.
- Which one is better (subline vs. subcolumn access)?





```
#include < c s t d i o >
# indude" cuda . h
# define N 2048
float A [ N ] [ N ]
: float c = 2 . 0 :
__d e vice_float dA [N][N]:
-- globa-l-voidmultiply Array 2 D (int n. float c)
  inti = blockldx.x * block Dim.x + threadldx.x
  : int i = b | o c k | d x . v * block Dim . v + t h r e a d | d x .
, y; if (i < n && j < n) { dA[i][j] * = c;}
int main (int argc, char * * argv)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j + +) {A[i][j] = i + j; }
  // Copy the table to the GPU
  cudaMemcpyToSymbol (dA, A, N * N * sizeof (float), 0,
       cuda Memcov HostTo Device ) :
  dim3 dim Block
  dim Block x = 32;
  dim Block , v = 3 2 :
  dim\ Block.z = 1;
  dim3 dim Grid
  dim Grid . x = N / 3 2;
  dim Grid . v = N / 3.2 *
  \dim Grid \cdot z = 1:
  multiply Array 2 D <<< d im Grid, dim Block >>> (N, c):
  // Copy the amay multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
  return 0:
```

- Using a dim3 for 2D indexing of threads.
- Consecutive threads in threadIdx.x are executed in a warp (then in threadIdx.y, then into threadIdx.z).
- So each warp has access b sub-column of A.





Multiply each element of an array A[N][N] by a scalar c

```
#include < cstdio>
# indude" cuda . h
# define N 2048
float A [ N ] [ N ]
: float c = 2 . 0 :
__d e vice_float dA [N][N]:
-- globalwoidmultiplyArray2D(intn,floatc)
  int i = blockldx.x * block Dim.y + threadldx.y
  : int i = blockldx.v*blockDim.x+threadldx.
  x : if(i < n & i < n & i < n) { dA[i][j] * = c; }
int main (int argc, char * * argv)
  for (int i = 0; i < N; i + +) {
    for (int j = 0; j < N; j + +) {A[i][j] = i + j; }
  // Copy the table to the GPU
  cudaMemcpyToSymbol (dA, A, N * N * sizeof (float), 0,
       cuda Memcov HostTo Device ) :
  dim3 dim Block
  dim Block x = 32
  dim Block , v = 3 2 :
  \dim Block \cdot z = 1;
  dim3 dim Grid
  \dim Grid \cdot x = N / 3.2
  dim Grid . v = N / 3 2 :
  \dim Grid.z = 1
  multiply Array 2 D <<< d im Grid, dim Block >>> (N, c):
  // Copy the amay multiplies to the CPU
  cudaMemcpvFromSvmbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
```

Use a dim3 for 2D thread indexing.

- Consecutive threads in threadIdx.x are executed in a warp (then in threadIdx.y, then into threadIdx.z).
- So each warp has access b subline of A.
 - Which one is better?





Grid and block size limits

For a grid, you must use

- **dim3.x** \leq ²³¹ 1
- **dim3.y** ≤ 65535
- dim3.z ≤ 65535

For a block, you must use

- $dim3.x \le 1024$
- **dim3.y** ≤ 1024
- dim3.z ≤ 64
- Total number of threads ≤ 1024

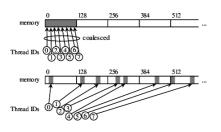


Outline

- Multi-dimensional indexing of blocks and threads
- Coalescence
- Practical: Multiplication of matrices

Coalescence

This is access the global memory of threads in a warp.

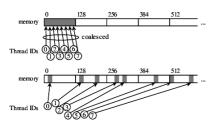


- Threads in a warp execute instructions synchronously.
- Each memory access is also processed synchronously.
- If the threads consecutive elements in the memory, this only requires the opening of one line (so 1 access).



Coalescence (cont.)

This is access the global memory of threads in a warp.



- If there are jumps, each line touched will be read.
 - imit, 32 lines read for one access. Most
 - elements in the line are unused.
- Rule: Design the kernel so that accesses are contiguous in threadIdx.x.



```
#include < cstdio>
# include" cuda . h
# define N 2048
float A[N][N]:
float c = 2.0:
__d e vice float dA [N][N]:
__globa_l_widmultiplyArray2D(intn,floatc)
  int i = blockldx.x;
  int j = blockldx.y * block Dim.x + threadIdx.x;
  if(j < n) \{ dA[i][j] * = c; \}
int main (int argc. char * * argv)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) \{ A[i][j] = i + j; \}
  // Copy the table to the GPU
  cudaMemcpyToSymbol ( dA , A, N * N * sizeof ( float ) , 0 ,
       cuda Memcov HostTo Device ) :
  int b l o c k S i z e = 1 0 2 4 :
  dim3 d i m Gr i d:
  dim Grid.x = N
  dim Grid.v = N / block Size:
  dim Grid.z = 1:
  multiply Array 2 D <<< d im Grid, block Size >>> (N, c):
  // Copy the array multiplies to the CPU
  cudaMemcpyFromSymbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
  return 0;
```

- Is it **coalescing**?
- Yes! The matrix is stored in rows, threadIdx.x aligne on lines.





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A [ N ] [ N ] :
float c = 2.0:
__d e vice float dA [N][N]:
  inti = blockldx.x * block Dim.x + threadIdx.x;
  int j = blockldx.y;
  if(i < n) {dA[i][i] * = c:}
int main (int argc. char * * argv)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) \{ A[i][j] = i + j; \}
  // Copy the table to the GPU
  cudaMemcpyToSymbol ( dA , A, N * N * sizeof ( float ) , 0 ,
       cuda Memcov HostTo Device ) :
  int b l o c k S i z e = 1 0 2 4 :
  dim3 d i m Gr i d:
  d i m Gr i d . x = N / b l o c k S i z e
  ; d i m Gr i d . y = N;
  dim Grid.z = 1:
  multiply Array 2 D <<< d im Grid, block Size >>> (N, c):
  // Copy the array multiplies to the CPU
  cudaMemcpyFromSymbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
  return 0;
```

- Is it coalescing?
- No! The matrix is stored in rows, threadIdx.x aligne on columns.
- 32 l'ectures mémoires n'ecessaires pour chaque accès mémoire d'un warp.





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A[N][N]:
float c = 2.0:
__d e vice float dA [N][N]:
__globa_l_widmultiplyArray2D(intn,floatc)
  int i = blockldx.x * block Dim.x + threadIdx
  x; int j = b l o c k l d x . y * block Dim . y + t h r e a d l d
  x.y; if (i < n & i < n & j < n) { dA[i][j] * = c; }
int main (int arg c. char * * a r g v)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) {A[i][j] = i + j; }
  // Copy the table to the GPU
  cudaMemcpvToSvmbol (dA , A, N * N * sizeof (float) , 0 ,
       cuda Memcov HostTo Device ) :
  dim3 dim Block
  dim Block . x = 3 2 :
  dim Block . y = 3 2; dim
  Block z = 1 \cdot dim3 di
  m Grid;
  d i m Gr i d . x = N / 3 2;
  d i m Gr i d . y = N / 3 2;
  dim Grid.z = 1
  multiply Array 2 D <<< d im Grid, dim Block >>> (N, c):
  // Copy the array multiplies to the CPU
  cudaMemcpyFromSymbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
```

- Is it coalescing?
 - No! The matrix is stored in rows, threadIdx.x aligne on columns.
- 32 l'ectures memoires n'ecessaires pour chaque accès memoire d'un warp.





```
#include < cstdio>
# include" cuda . h
# define N 2048
float A[N][N]:
float c = 2.0:
__d e vice float dA [N][N]:
__globa_l_widmultiplyArray2D(intn,floatc)
  int i = blockldx.x * block Dim.y + threadldx.
  y; int j = b l o c k l d x . y * block Dim . x + t h r e a d l d
 x.x; if (i < n & i = c;)
int main (int arg c. char * * a r g v)
  for (int i = 0; i < N; i + +) {
     for (int j = 0; j < N; j ++) {A[i][j] = i + j; }
  // Copy the table to the GPU
  cudaMemcpvToSymbol (dA , A, N * N * sizeof (float) , 0 ,
       cuda Memcov HostTo Device ) :
  dim3 dim Block :
  dim Block . x = 3 2 :
  dim Block . y = 3 2; dim
  Block z = 1 \cdot dim3 di
  m Grid;
  d i m Gr i d . x = N / 3 2;
  d i m Gr i d . y = N / 3 2;
  dim Grid.z = 1;
  multiply Array 2 D <<< d im Grid, dim Block >>> (N, c):
  // Copy the array multiplies to the CPU
  cudaMemcpyFromSymbol (A, dA, N * N * sizeof (float), 0,
       cuda Memcpy Device To Host );
  printf("%f\n", A[11[21):
```

- Is it coalescing?
- Yes! The matrix is stored in rows, threadIdx.x aligne on lines.



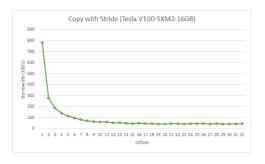


Example: Access an array with jumps

- How the performance evolve in relation to the stride?
- For **stride** = 1, the ecture of a 128 bytes line.
- For **stride** = 2, the reading of two lines of 128 bytes (half unused)
- **.** . . .
- For **stride** = 32, the reading of 32 lines of 128 bytes (31/32 unused)



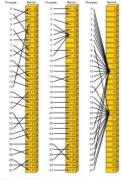
Performance of the access **a**n array with jumps



The effective bandwidth drops very quickly with jumps.



Coalescence rules



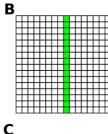
- Left
 Conflict-free access via random permutation.
- Conflict-free access since threads 3, 4, 6, 7, and 9 access the same word within bank Right
- Right
 Conflict-free breadcast access (threads access the same word within a bank).

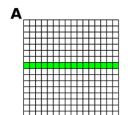
- Threads in a warp access the m^eme case m emoire = good performance (yet bande passent toujours gaspillee).
- Threads in a warp access the m^{eme line} in m emory in an aleatoire order = still good performance in new architectures.
- If coalescence is difficult to do, shared memory could ^etre useful (coming soon).

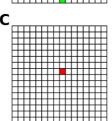


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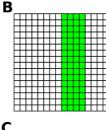


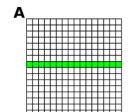


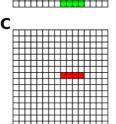


- The multiplication C = AB corresponds to the calculation $C[i][j] = \sum_{k=0}^{EN-1} A[i][k]B[k][j]$.
- First kernel: Create a block for each C[i][j].



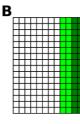


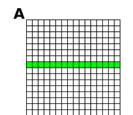


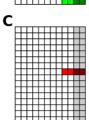


- The multiplication C = AB corresponds to the calculation $C[i][j] = \sum_{k=0}^{EN-1} A[i][k]B[k][j]$.
- Second kernel: Use P threads per block, each block computes P
 main elements of a line of C (P = 4 here).
- Assume that P divides N.



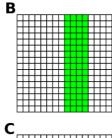


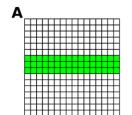


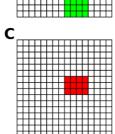


- The multiplication C = AB corresponds to the calculation $C[i][j] = \sum_{k=0}^{EN-1} A[i][k]B[k][j]$.
- Third kernel: Use P threads per block, each block computes P
 Tignain elements of a line of C (P = 4 here).
- Assume that P does not divide N.



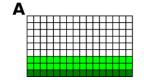






- The multiplication C = AB corresponds to the calculation $C[i][j] = \sum_{k=0}^{EN-1} A[i][k]B[k][j]$.
- Fourth kernel: Use PQ threads per block, each block computes P × Q
 The following is a list of temponents of a subblock of C (P = 4 and Q = 3 here).
- Assume that P and Q divide N.







- The multiplication C = AB corresponds to the calculation $C[i][j] = \sum_{k=0}^{n} A[i][k]B[k][j]$.
- Fifth kernel: Use PQ threads per block, each block computes P × Q tonsecutive elements of a sub-block of C (P = 4 and Q = 3 here).
- Assume that neither P nor Q divides N.

Contact

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