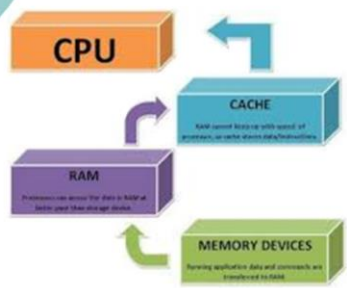
ساختار و زبان کامپیوتر

فصل ششم

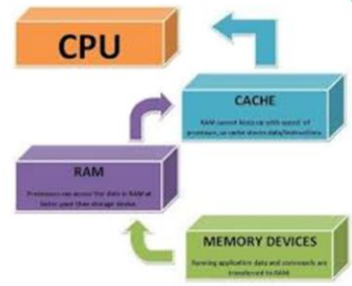
سازمان حافظه



Computer Structure and Machine Language

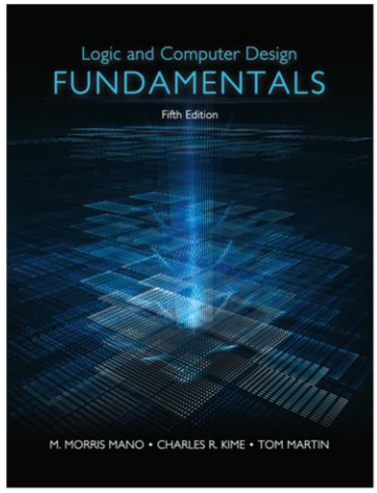
Chapter Six

Memory Organization



Logic and Computer Design Fundamentals

Fifth Edition



Chapter 7:

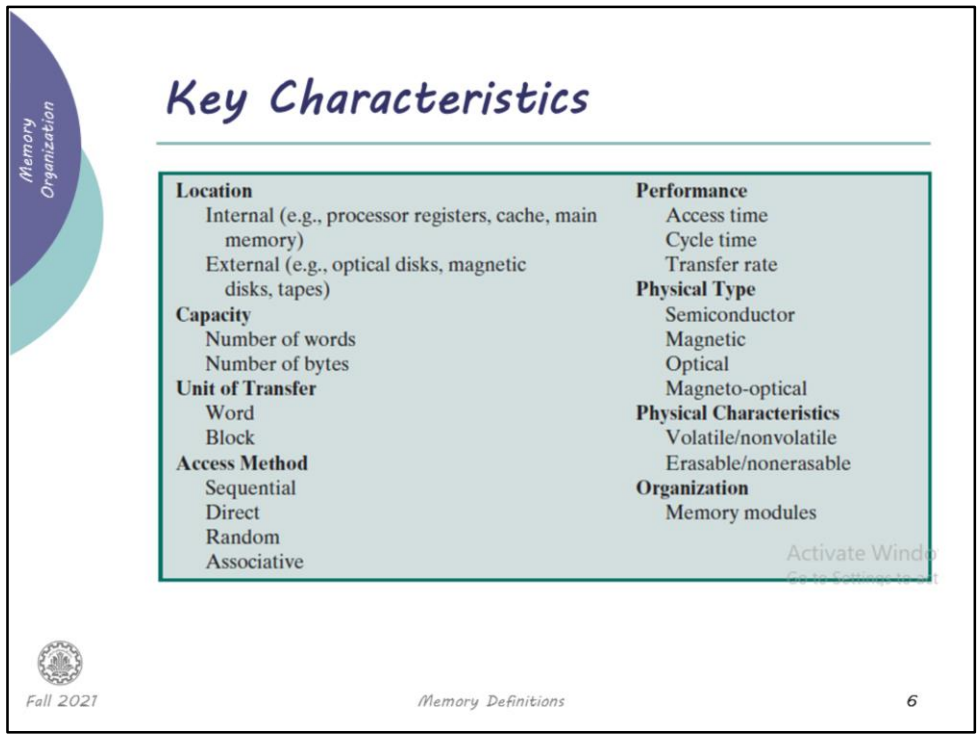
Memory Basics

Contents

- Memory Definitions
- Random Access Memory
  - SRAM Integrated Circuits
  - Array of SRAM ICs
  - DRAM Integrated Circuits
- Read Only Memory

Memory

- A collection of cells capable of storing binary information
- Contains electronic circuits for storing and retrieving the information
- Used in many different parts of a computer, providing temporary or permanent storage for substantial amounts of binary information



Two types of memories are used in various parts of a computer: *random-access memory* (RAM) and *read-only memory* (ROM).

RAM accepts new information for storage to be available later for use.

The process of storing new information in memory is referred to as a *memory write* operation.

The process of transferring the stored information out of memory is referred to as a *memory read* operation.

RAM can perform both the write and the read operations, whereas ROM performs only read operations.

Memory units that lose stored information when power is turned off are said to be *volatile*.

RAMs are volatile while ROMS are *nonvolatile.*

Direct access: As with sequential access, direct access involves a shared read–write mechanism. However, individual blocks or records have a unique address based on physical location. Access is accomplished by direct access to reach a general vicinity plus

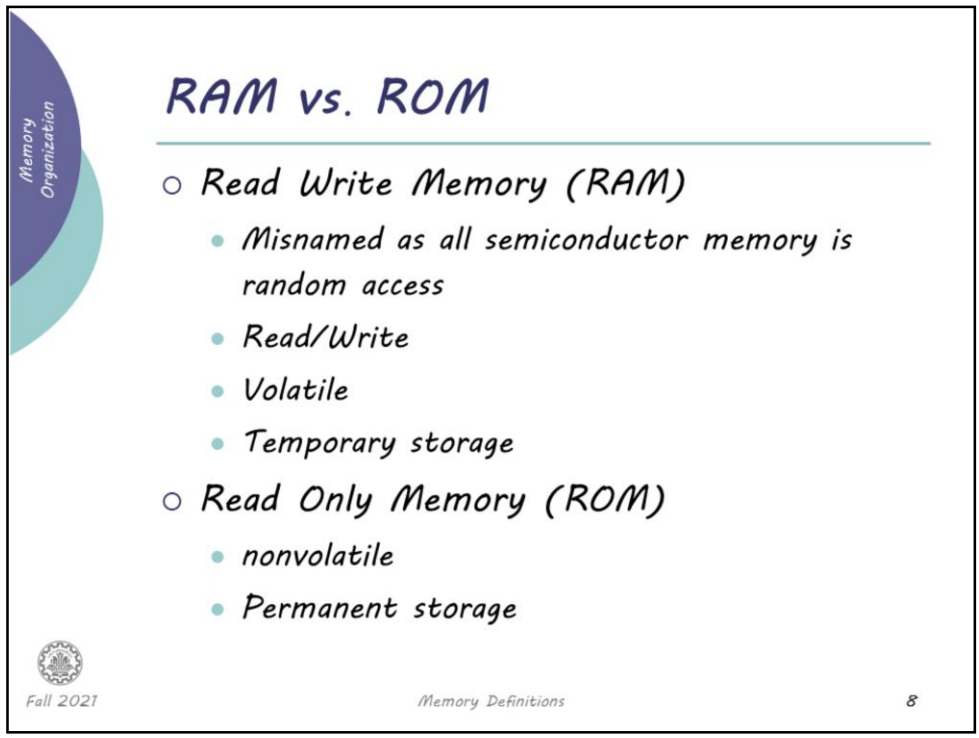
sequential searching, counting, or waiting to reach the final location. Again, access time is variable. Disk units are direct access.

Associative: This is a random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, and to do this for all words simultaneously. Thus, a word is retrieved based on a portion of its contents rather than its address. As with ordinary random-access memory, each location has its own addressing mechanism, and retrieval time is constant independent of location or prior access patterns. Cache memories may employ associative access.

Internal vs. External Memory

- Internal
  - Semiconductor memories
  - Register, Cache, Main Memory
- External
  - Magnetic/ Optical/ Semiconductor
  - Hard disks, Optical disks, SSD





The process of storing new information in memory is referred to as a *memory write* operation.

The process of transferring the stored information out of memory is referred to as a *memory read* operation.

Figure 7-2: Contents of a 1024 × 16 Memory

Memory Address		Memory Contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

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A word is an entity of bits that moves in and out of memory as a unit.

Each word in memory is assigned an identification number called an *address.*

Contents

- Memory Definitions
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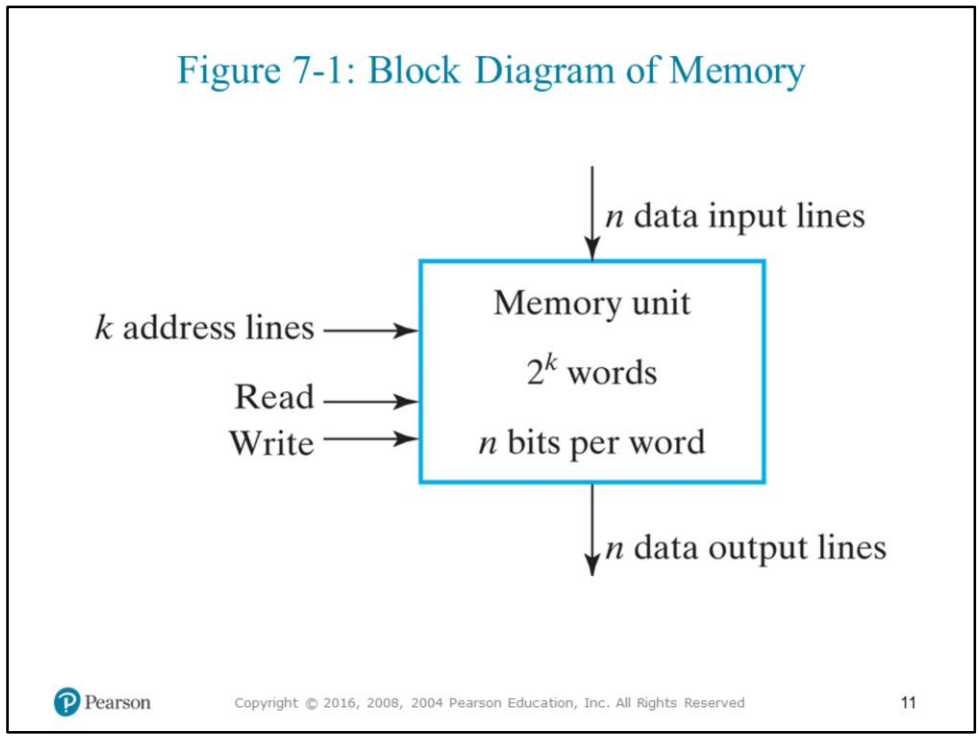
- Read Only Memory



The capacity of a memory unit is usually stated as the total number of *bytes* or *bits* that it can store.

The *n* data input/output lines provide the information to be stored in/read from memory.

The *k* address lines specify the particular word chosen among the many available.

The steps that must be taken for a *write* are as follows:

1. Apply the binary address of the desired word to the address lines.

2. Apply the data bits that must be stored in memory to the data input lines.

3. Activate the Write input.

The steps that must be taken for a *read* are as follows:

1. Apply the binary address of the desired word to the address lines.

2. Activate the Read input

Table 7.1: Control Inputs to a Memory Chip

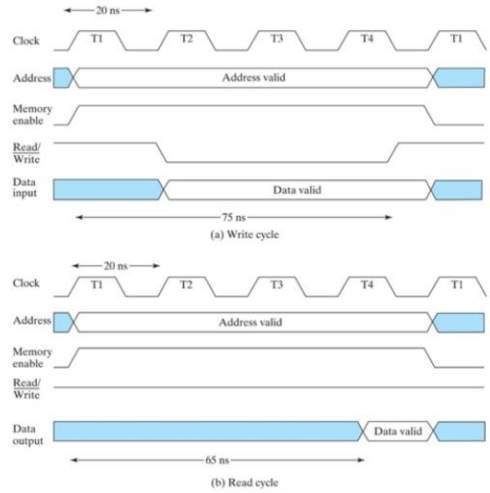
Chip Select CS	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	Memory Operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

Memory is made up of RAM integrated circuits (chips), plus additional logic circuits.

A *Chip Select* selects the chip to be read from or written to

A Read/Write that determines the particular operation

Figure 7-3: Memory Cycle Timing Waveforms



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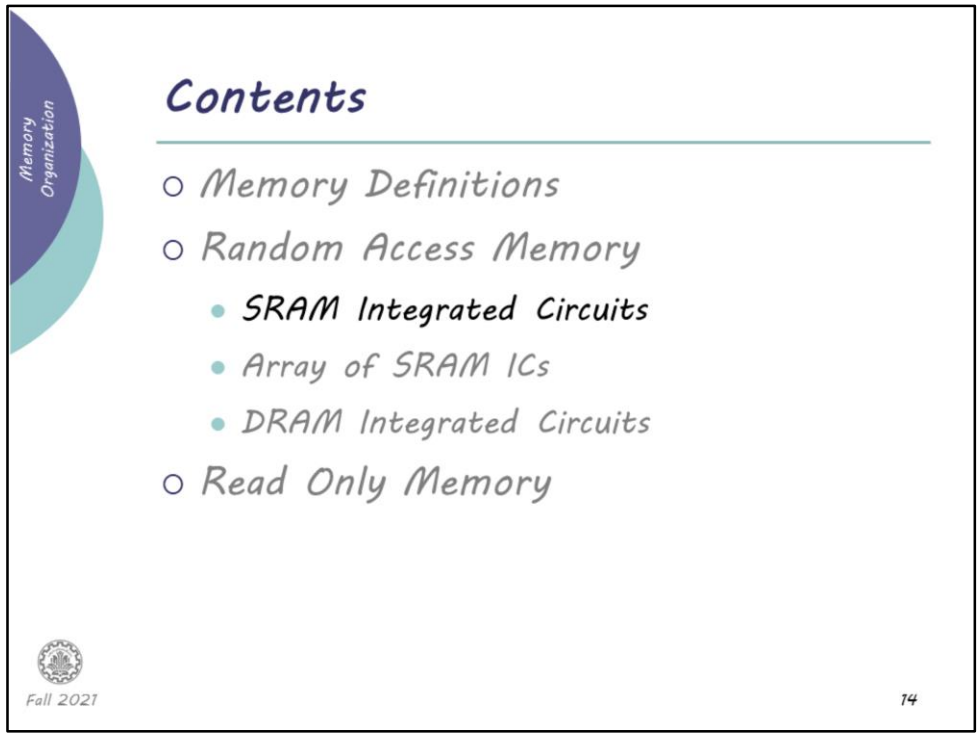
The operation of the memory unit is controlled by an external device, such as a CPU.

The *access time* of a memory read operation is the maximum time from the application of the address to the appearance of the data at

the Data Output.

The *write cycle time* is the maximum time from the application of the address to the completion of all internal memory operations required to store a word.



Static RAM (SRAM) consists of internal latches that store the binary information. The stored information remains valid as long as power is applied to the RAM.

Dynamic RAM (DRAM) stores the binary information in the form of electric charges on capacitors. The capacitors must be periodically recharged by *refreshing* the DRAM.

Figure 7-4: Static RAM Cell

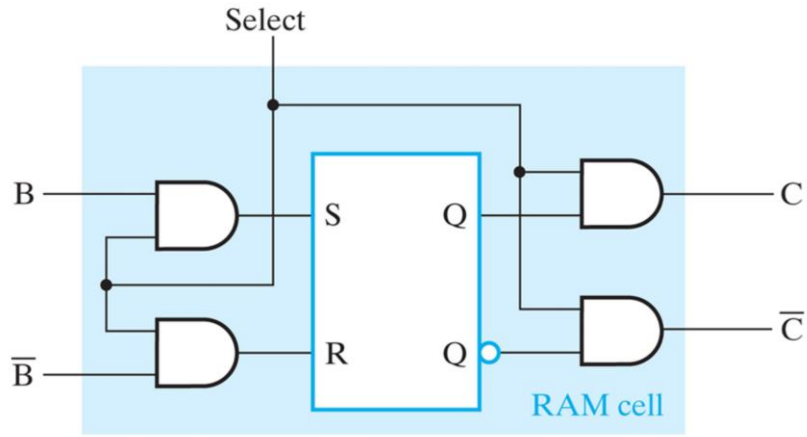
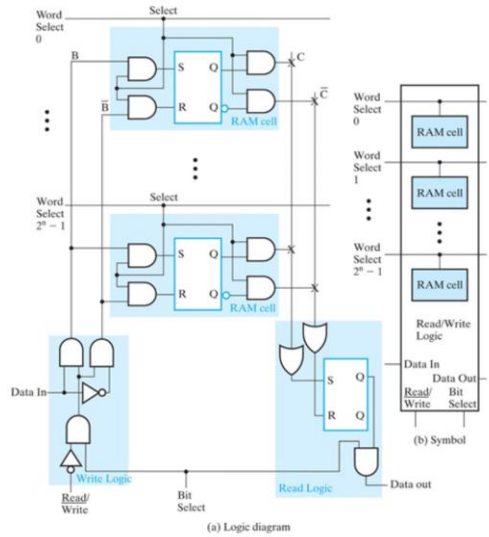


Figure 7-5: RAM Bit Slice Model



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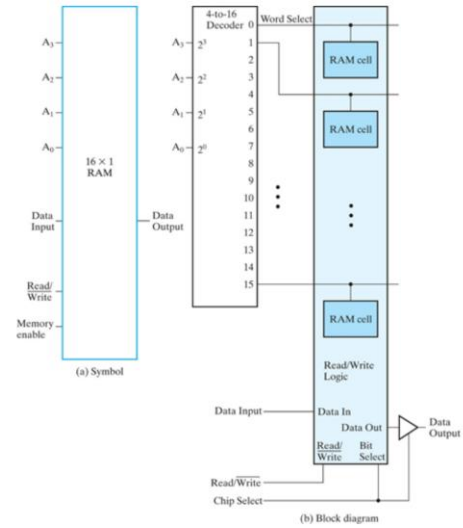
Only one word is written at a time. That is, only one Word Select line is 1, and all other Word Select lines are 0.

Each *Word Select* line extends beyond the bit slice, so that when multiple RAM bit slices are placed side by side, corresponding Word Select lines connect.

Figure 7-6: 16-Word by 1-Bit RAM Chip



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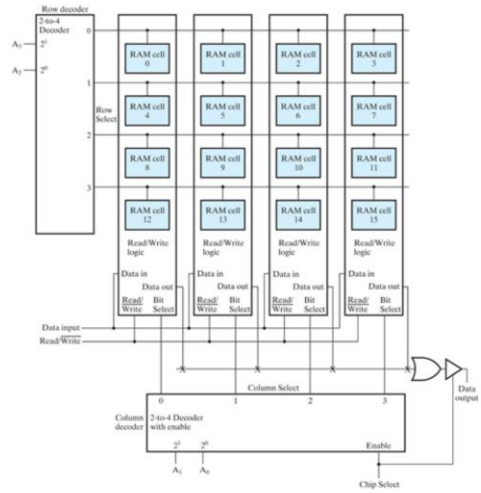
The three-state buffer allows construction of a multiplexer with an arbitrary number of inputs.

Three-state outputs are connected together and properly controlled using the Chip Select inputs.

Chip select combinations containing a single 1 can be obtained from a decoder.

Figure 7-7: Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array



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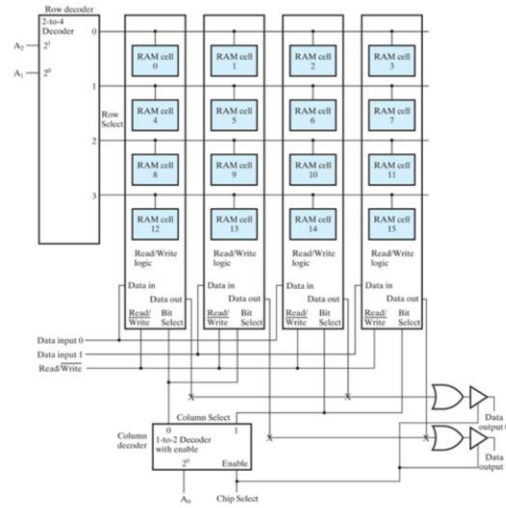
Coincident Selection

One decoder controls the word select lines (*Row Select*) and the other controls the bit select lines (*Column Select*).

The result is a two-dimensional matrix selection scheme.

The column decoder is enabled with the Chip Select input.

Figure 7-8: Block Diagram of an 8 × 2 RAM Using a 4 × 4 RAM Cell Array



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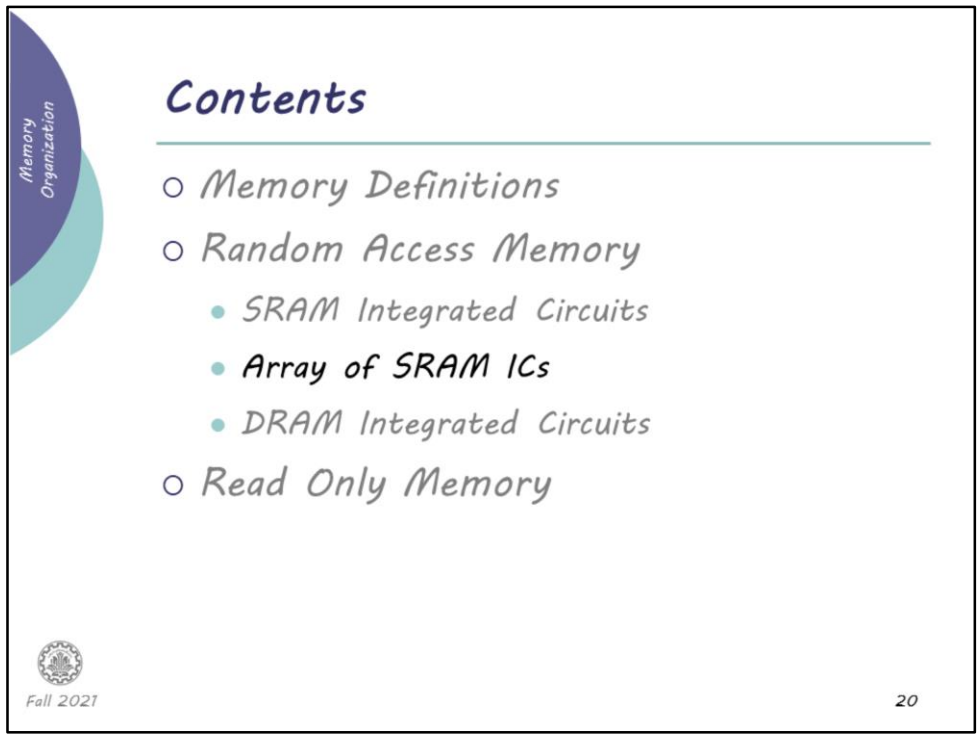
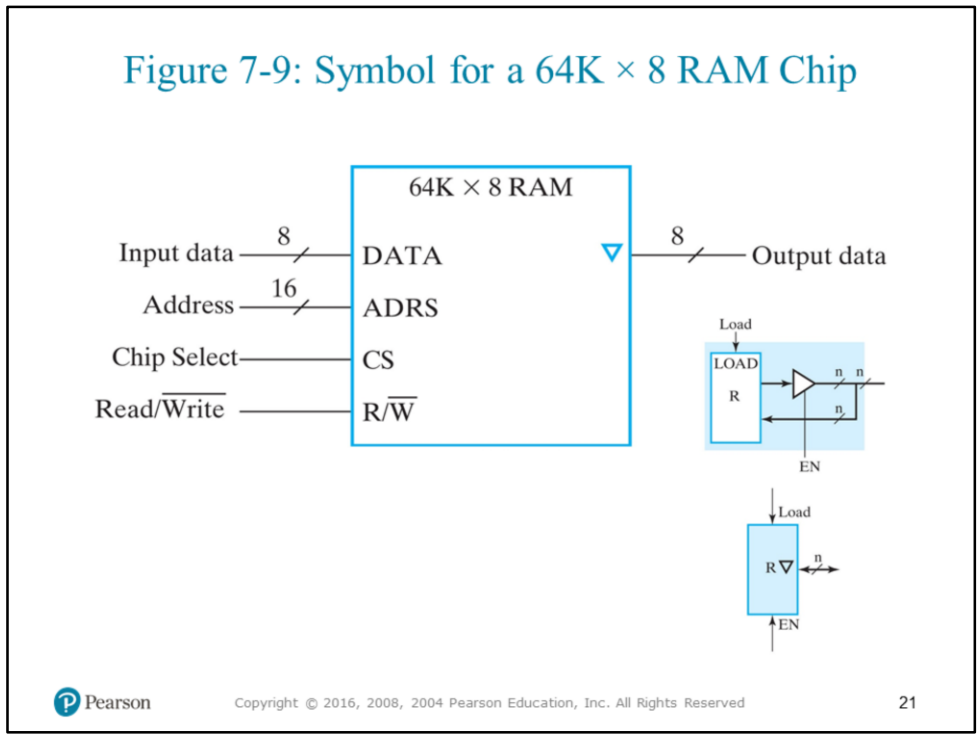
The same RAM cell array is used in Figure 7-8 to produce an 8 * 2 RAM chip (eight words of two bits each).

The only changes are in the column and output logic.



If the memory unit needed for an application is larger than the capacity of one chip, it is necessary to combine a number of chips in an array to form the required size of memory



To reduce the number of pins on the chip package, many RAM ICs provide common terminals for the data input and data output.

The common terminals are said to be *bidirectional*

Figure 7-10: Block Diagram of a 256K × 8 RAM

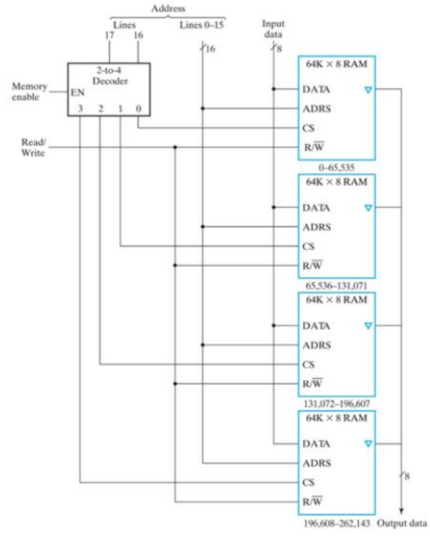
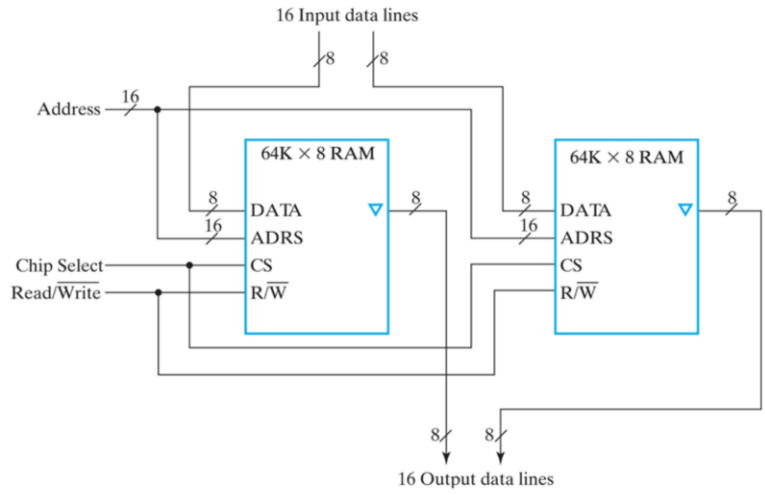
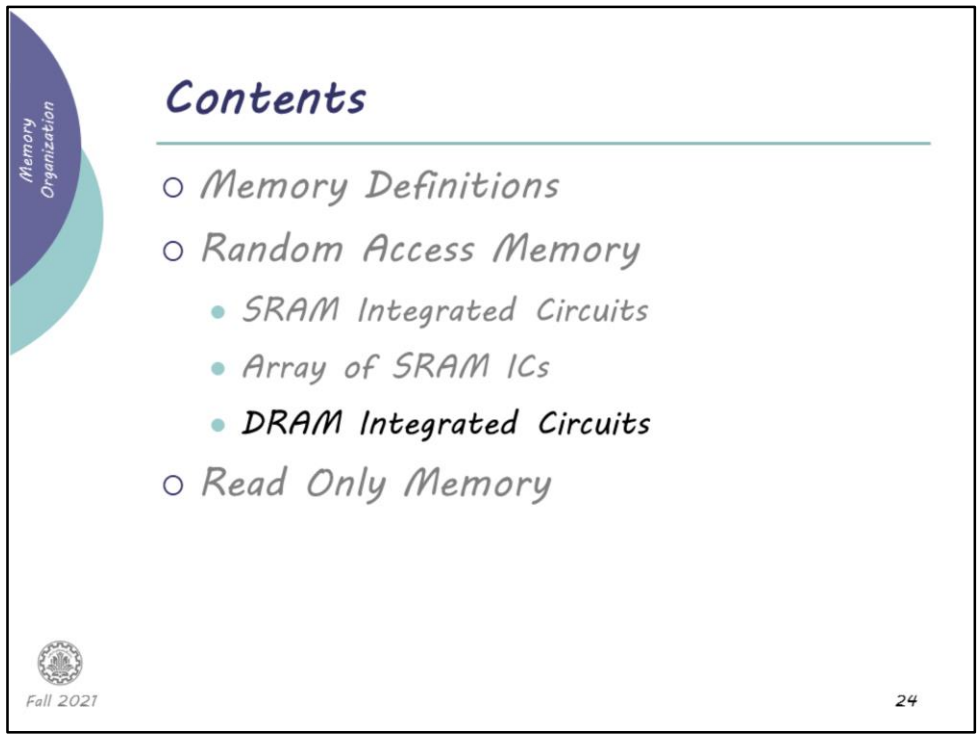


Figure 7-11: Block Diagram of a 64K × 16 RAM





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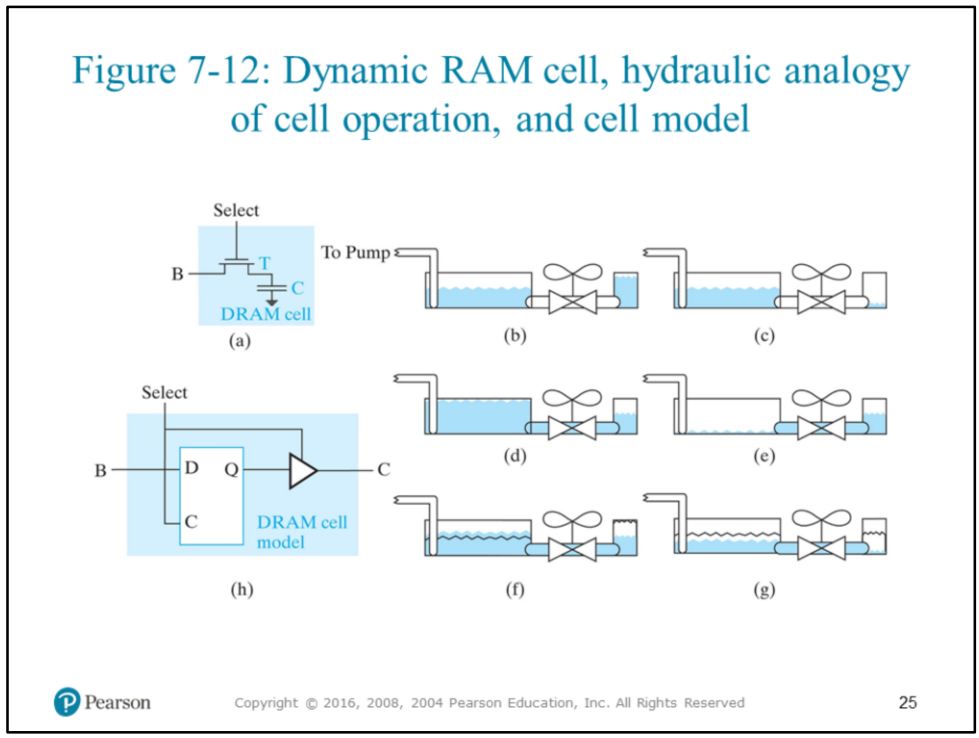


If sufficient charge is stored on the capacitor, it can be viewed as storing a logical 1.

The transistor acts much like a switch. When the switch is "open," the charge on the capacitor roughly remains fixed— is stored.

When the switch is "closed," charge can flow into and out of the capacitor from the external Bit (B) line. This charge flow allows the cell to be written with a 1 or 0 and to be read.

Destructive read: the read operation destroys the stored value

Figure 7-13: DRAM Bit-Slice Model

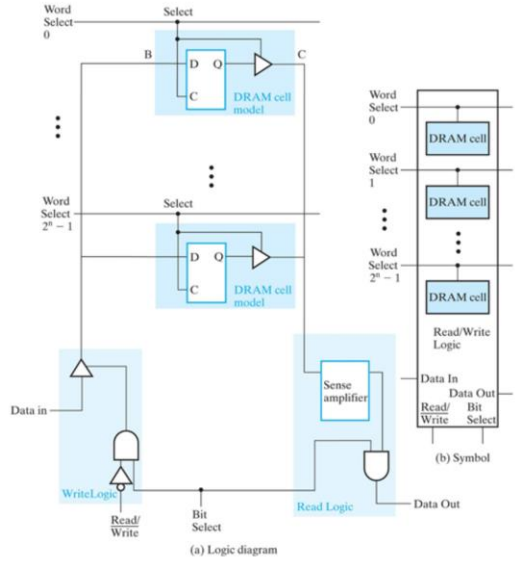
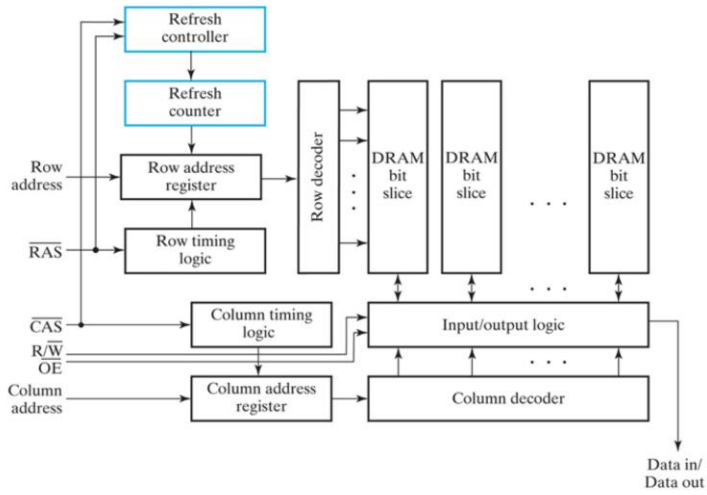


Figure 7-14: Block Diagram of a DRAM Including Refresh Logic



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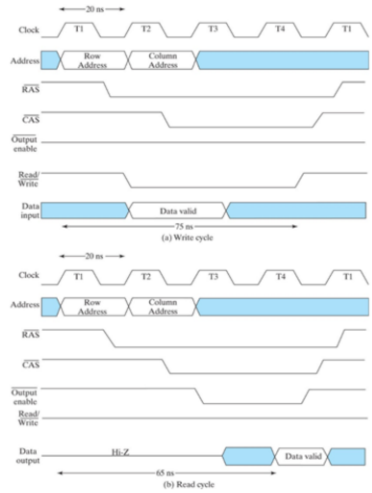
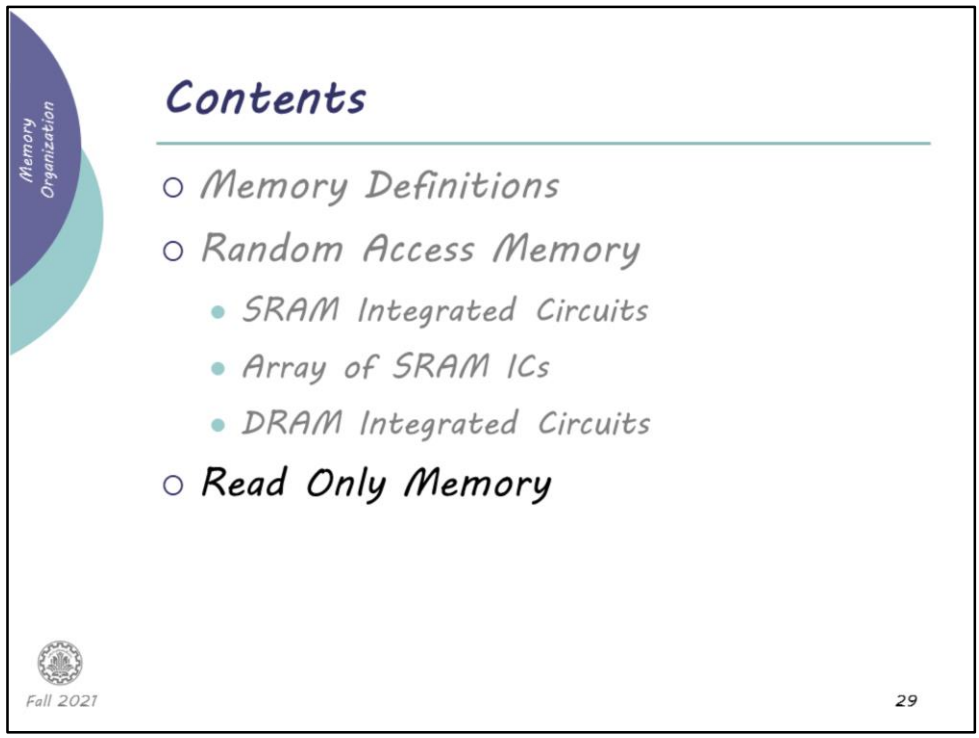
To reduce the number of pins, the DRAM address is applied serially in two parts with the row address first and the column address second.

RAS: Row address Strobe

CAS: Column Address Strobe

Figure 7-15: Timing for DRAM Write and Read Operations





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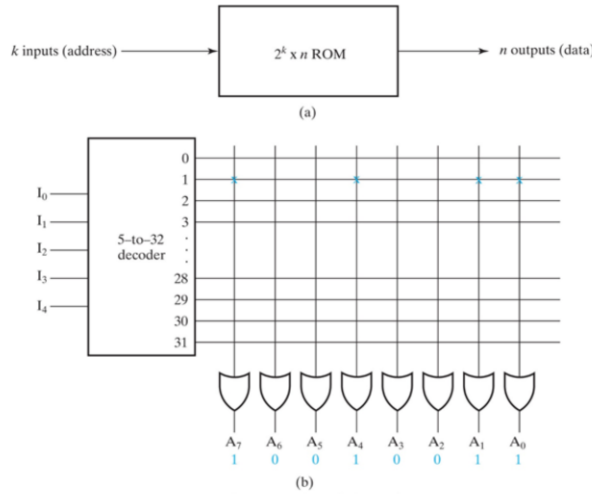
RAMs are volatile while ROMS are *nonvolatile.*

Figure 5-7 Block Diagram and Internal Logic of a ROM



Read-only memories have different names:

1. ROM: mask programmed,

2. PROM: fuse or anti-fuse programmed,

3. EPROM: erasable floating gate programmed,

4. EEPROM or E2PROM: electrically erasable floating gate programmed,

5. FLASH Memory: electrically erasable floating gate with multiple erasure and programming modes.

The choice of programming technology depends on many factors, including the number of identical ROMs to be produced, the desired permanence of the programming, the desire for reprogrammability, and the desired performance in terms of delay

Summary: Random Access Memory Types

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-Write Memory (RWM)	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-Only Memory (ROM)	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-Mostly Memory (RMM)	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level