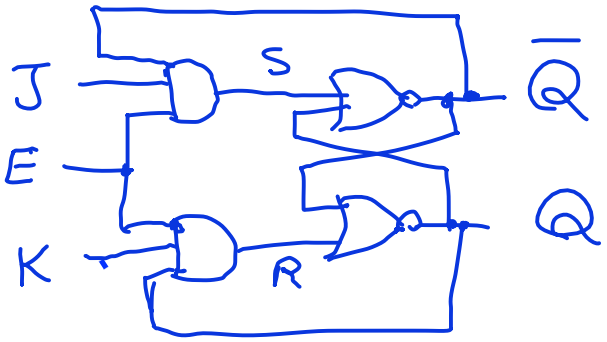
J-K Latch

J = Jump → set

K = Kill → reset

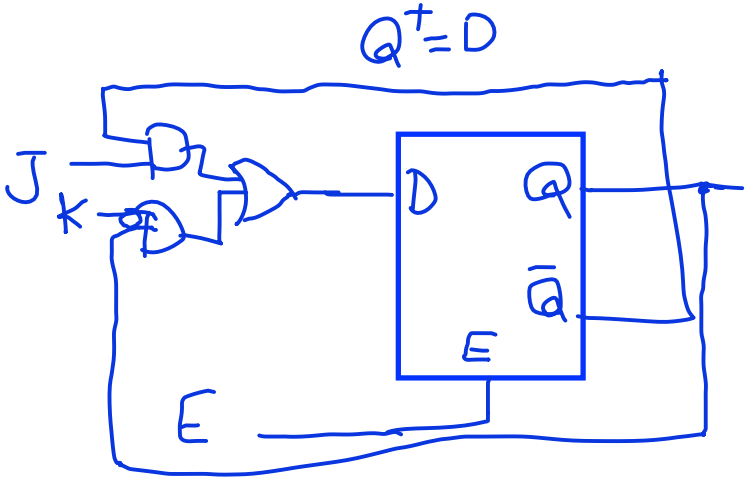


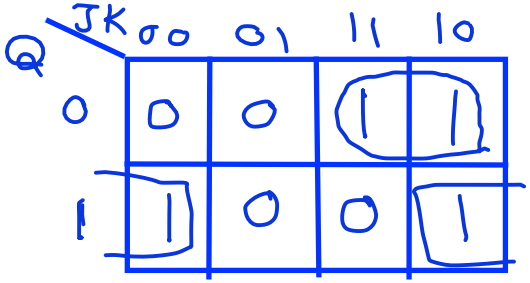
J	K	Q^n	Q^{n+1}	
0	0	0	0	} memory
0	0	1	1	
0	1	0	0	} Kill (reset)
0	1	1	0	
1	0	0	1	} Jump (set)
1	0	1	1	
1	1	0	1	} complement, toggle
1	1	1	0	

جدول حقیقت characteristic Table

$E=0 \rightarrow S=R=0 \Rightarrow Q^{n+1}=Q^n$

$E=1 \rightarrow$ حالت Jk Latch

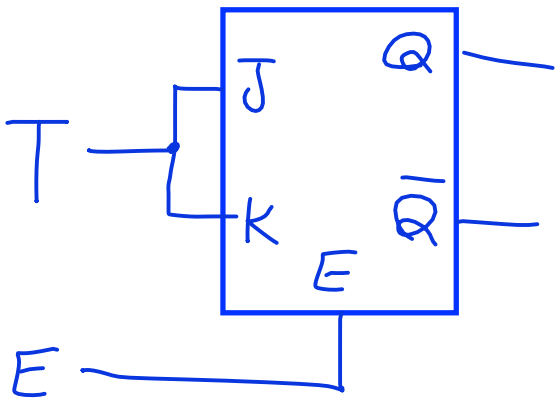




$Q^+ = Q(t+1) = J\bar{Q} + \bar{K}Q$ معادله مشخصه

J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q^n}$

T latch



J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

JK Latch

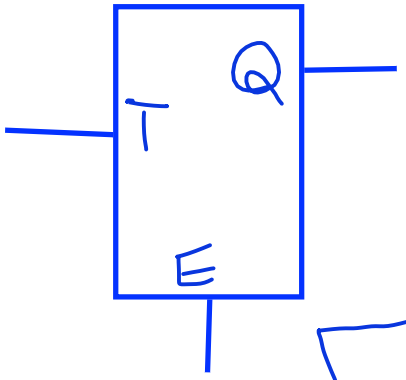
T	Q^+
0	Q
1	$\bar{Q}$

T Latch

↓

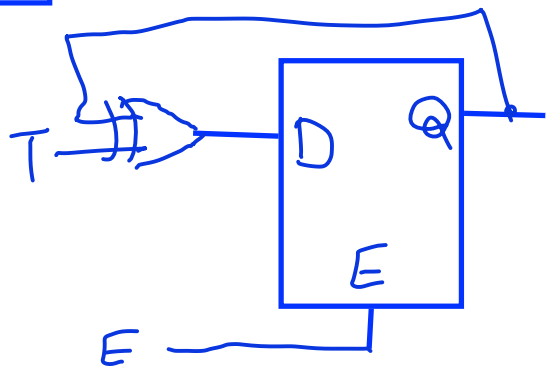
Toggle

E = 1

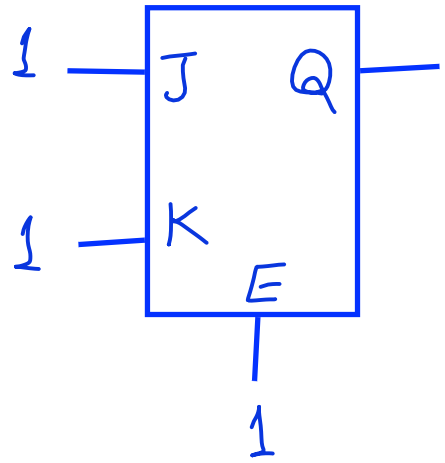


$$Q^+ = \bar{T}.Q + T.\bar{Q} = T \oplus Q$$

T / Q	0	1
0	0	(1)
1	(1)	0



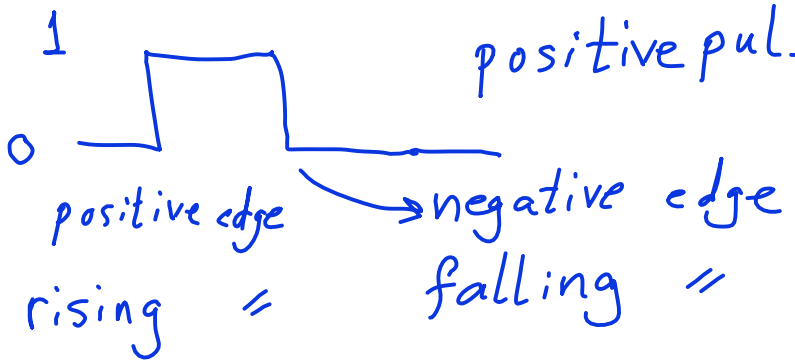
Flip-Flop



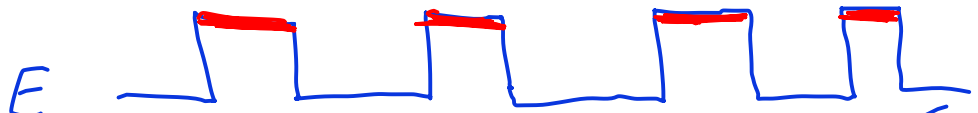
1 → 0 → 1 → 0 → ....

تغییر لحظه‌ای سیگنال کنترلی (CLK یا E) موجب تغییر حالت عنصر حافظه می‌شود. این تغییر لحظه‌ای = trigger (ماشه) (راه اندازی).

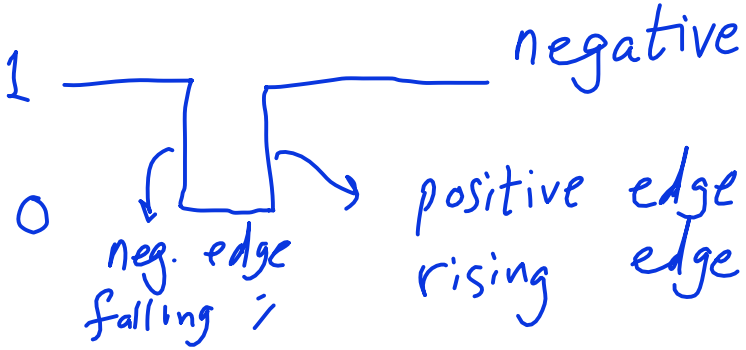
(حساس به سطح سیگنال کنترلی)



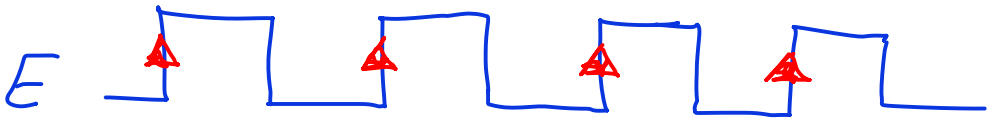
Latch response — level sensitive



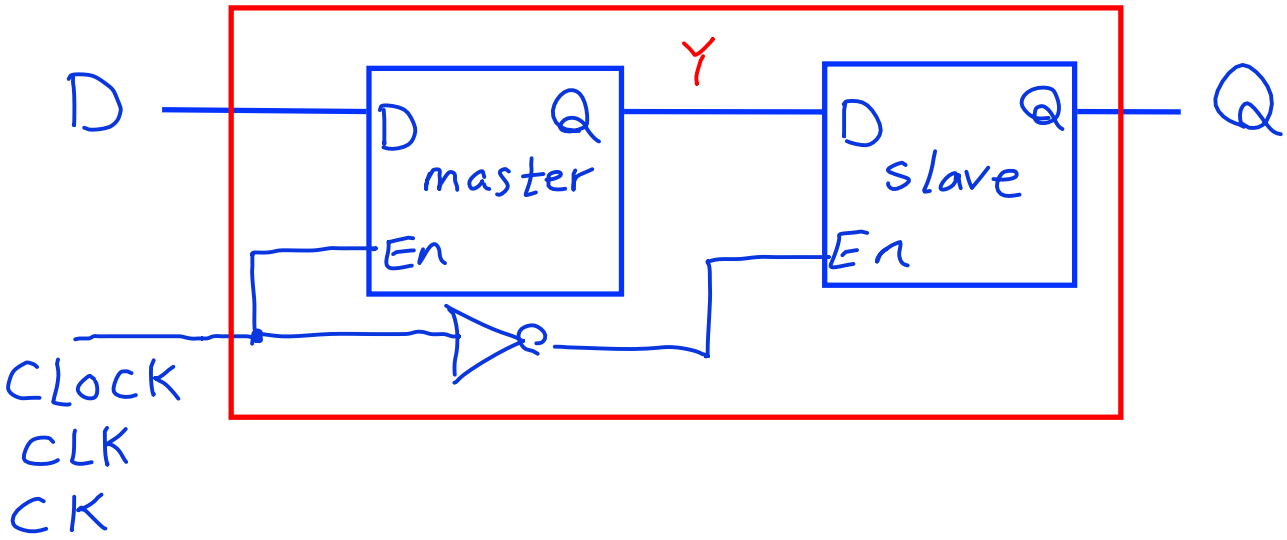
مدار آشکارساز (غیر همگام) است.

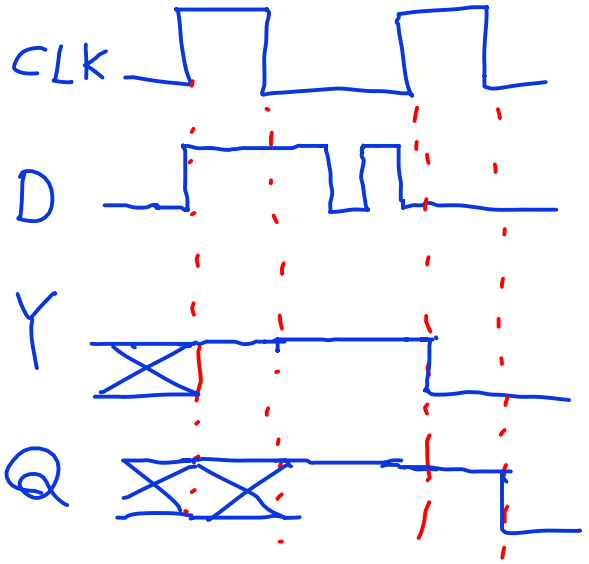


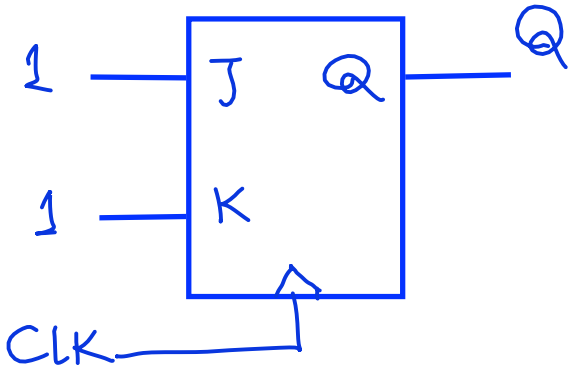
FF response — edge sensitive (حساس به لبه)

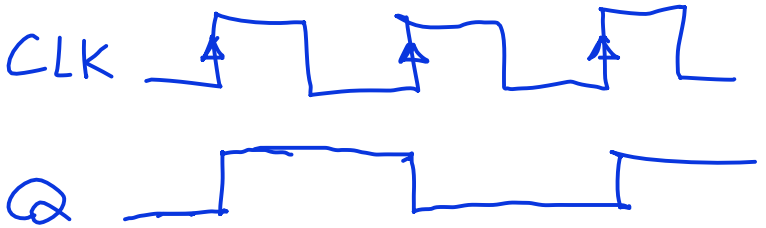


Master-slave D FF

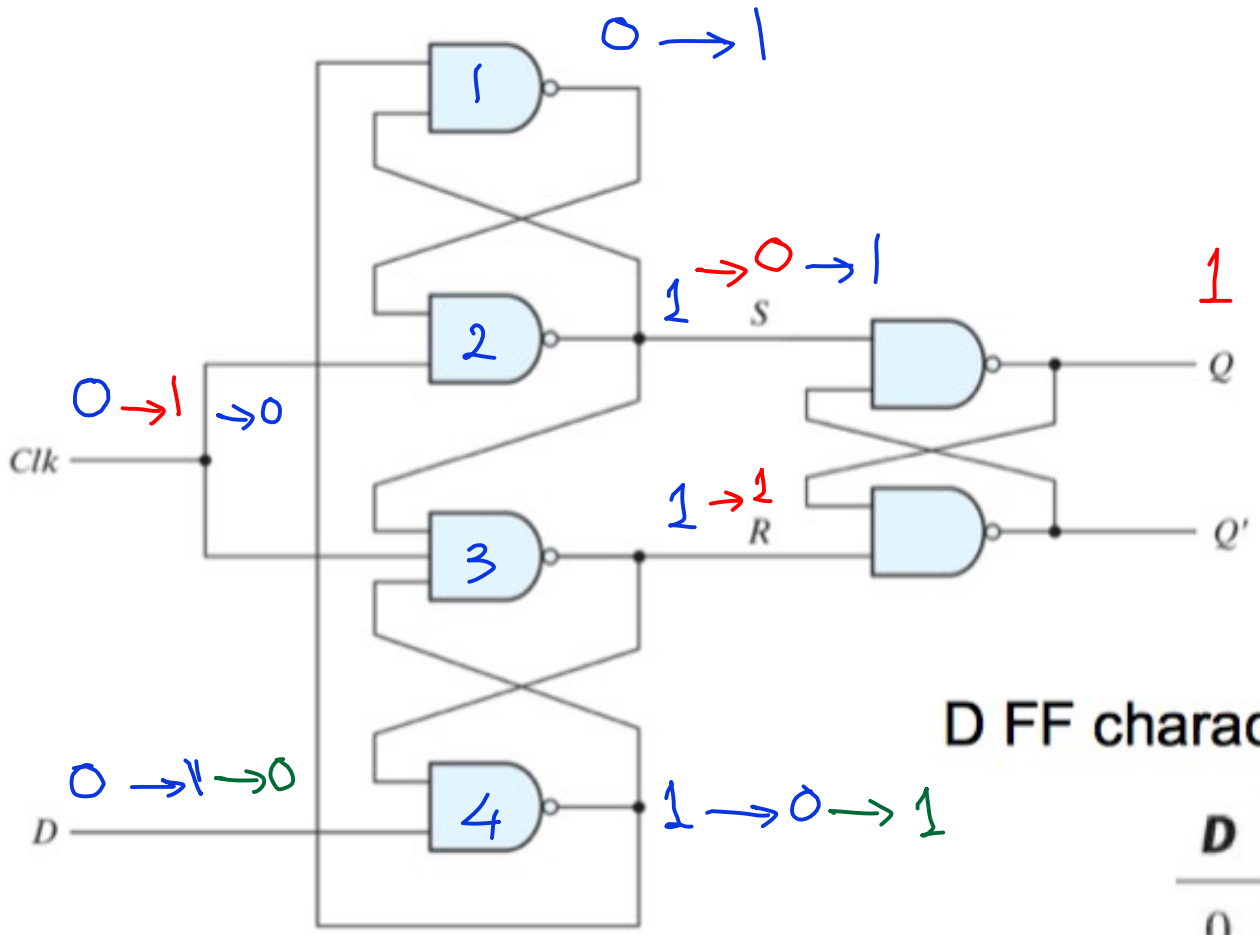








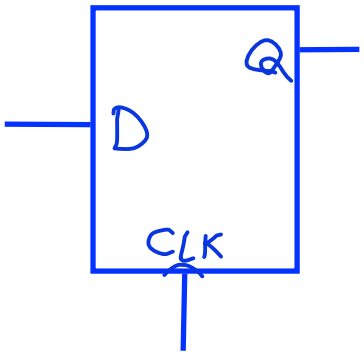
D-type positive-edge-triggered flip-flop



D FF characteristic table

D	*Q*(*t* + 1)	
0	0	Reset
1	1	Set

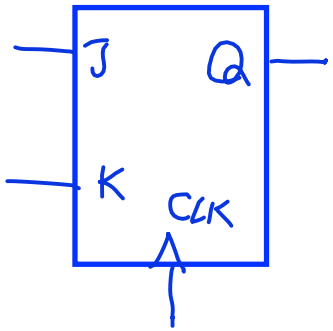
D FF



D	Q^{n+1}
0	0
1	1

$$Q^{n+1} = D$$

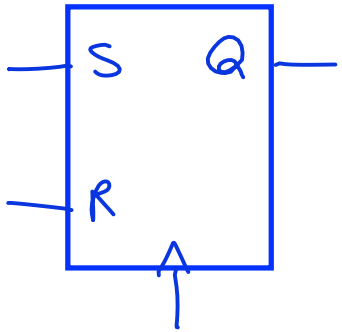
JK FF



J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q^n}$

$$Q^{n+1} = J\overline{Q^n} + \overline{K}.Q^n$$

SR FF



S	R	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	غير مسموح

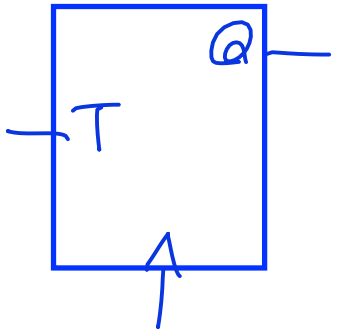
$$Q^{n+1} = S + \overline{R}Q^n$$

$$S.R = 0$$

SR / Q	00	01	11	10
0	0	0	X	1
1	1	0	X	1

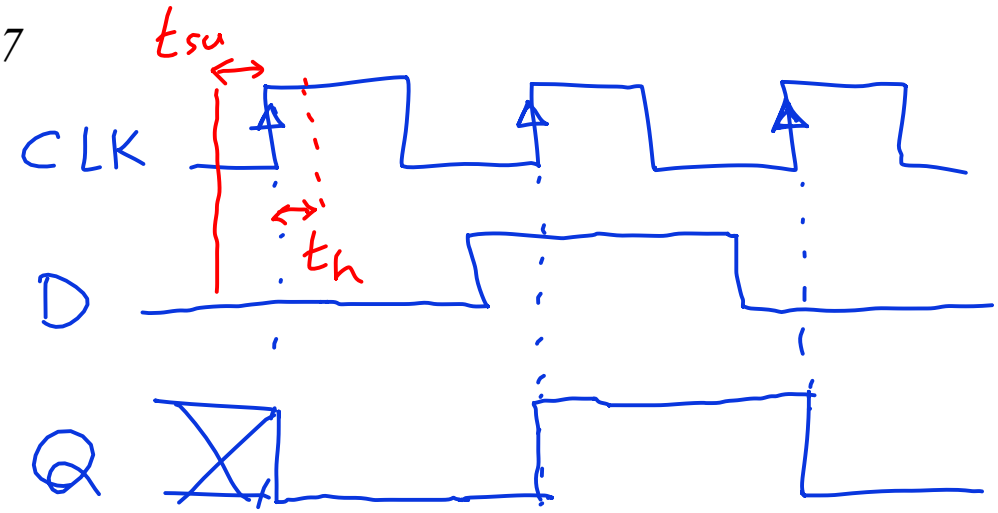
$$Q^{n+1} = S + \overline{R}Q^n \;,\; S.R = \emptyset$$

T FF



T	Q^{n+1}
0	Q^n
1	$\overline{Q^n}$

$$Q^{n+1} = T \oplus Q^n$$



t_{su} = setup time = زمان راه اندازی

زمان قبل از لبه موثر clock که باید ورودی (ها) بدون تغییر باشند.

t_h = hold time = زمان نگهداری

مدت زمانی که بعد از لبه موثر clock باید ورودی (ها) بدون تغییر باشند.