Digital System Design

Hajar Falahati

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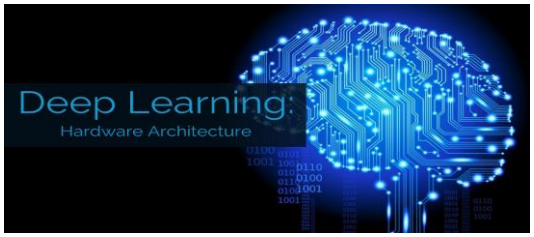
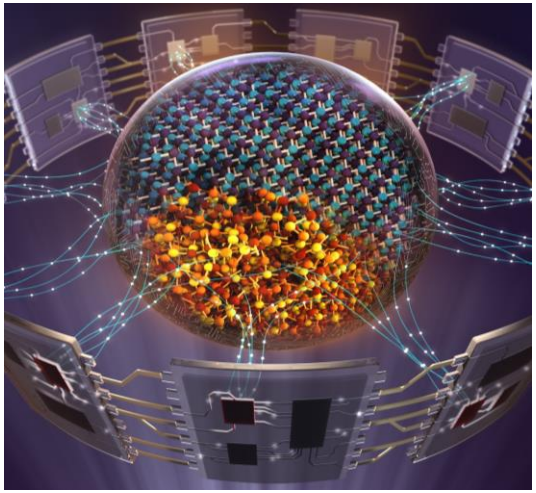
A Little About Me

- Hajar Falahati
  - **Postdoctoral Researcher** @ Institute in Fundamental Science and Technology (**IPM**), Since 2016.
    - Supervised by *Prof. Hamid Sarbazi-Azad*, Prof. *Pejman Lotfi-Kamran*
  - **Research Visitor** @ University of Southern California (**USC**), Apr 2015 – Apr 2016.
    - Supervised by *Prof. Masoud Pedram* and *Prof. Muralli Annavaram*
  - **PhD** @ Sharif University of Technology (**SUT**), Sep 20111 – Oct 2016.
    - Supervised by *Prof. Shaahin Hessabi*
  - **MSc** @ Sharif University of Technology (**SUT**), Sep 2009 – Sep 2011
    - Supervised by *Prof. Shaahin Hessabi*
  - **BSc** @ Isfahan University of Technology (**IUT**), Sep 2005 – Sep 20
    - Supervised by *Prof. Kiarash Bazargan and Mr. Nikaean*.

A Little About Me

- My Research Interest
  - Hardware Accelerators
  - Neural Networks
  - GPU Architecture
  - Processing-in-Memory
  - Bioinformatics

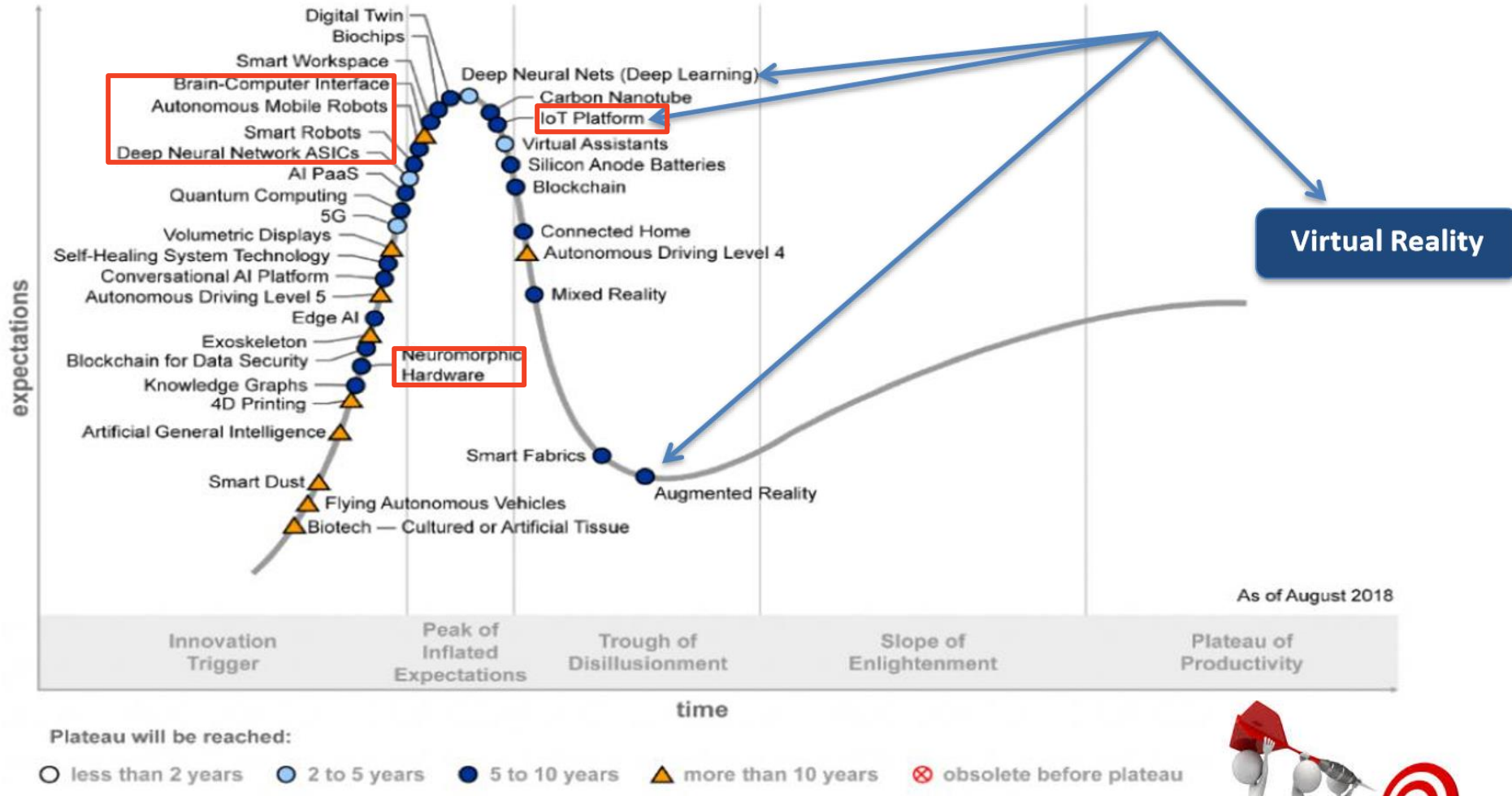




Welcome to Digital System Design (DSD)

Emerging Applications

Emerging Technologies



Market Share

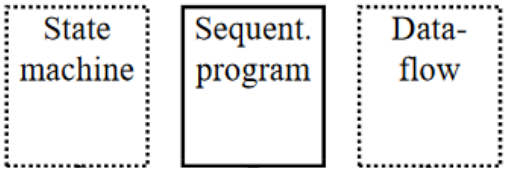
EE Times

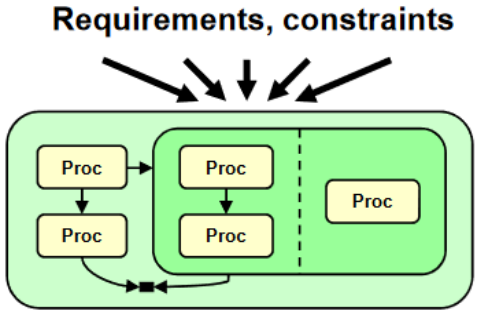
How to Get Involved?

Applications Are Getting Complex

- How to deal with the **complexity**?
- **Design approaches**
- **Abstraction levels**
- **Digital system modeling**
  - Finite State Machine (FSM)
  - Algorithm State Machine (ASM)

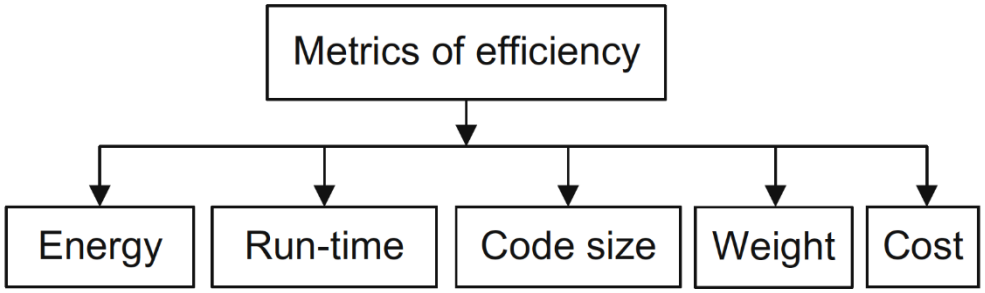
Models



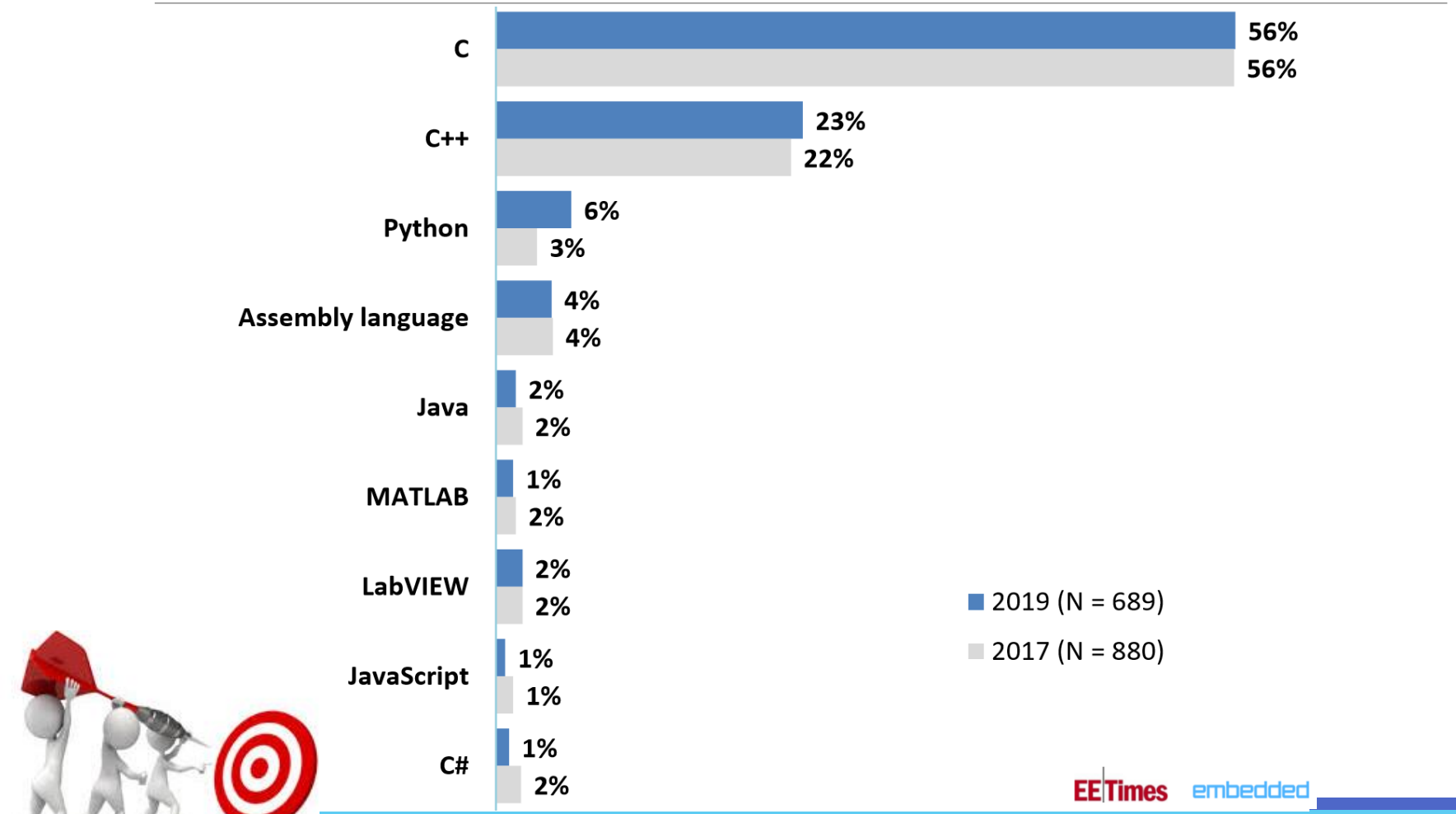


How to Process These Applications?

- How to make them **happy**?
  - Satisfy their **requirements**
    - Computational demands
    - Memory demands
- Software support
  - High level language
    - Python, C
    - ……
- Hardware supports
  - CPU, GPU, FPGA, Cloud, ASIC
  - …..

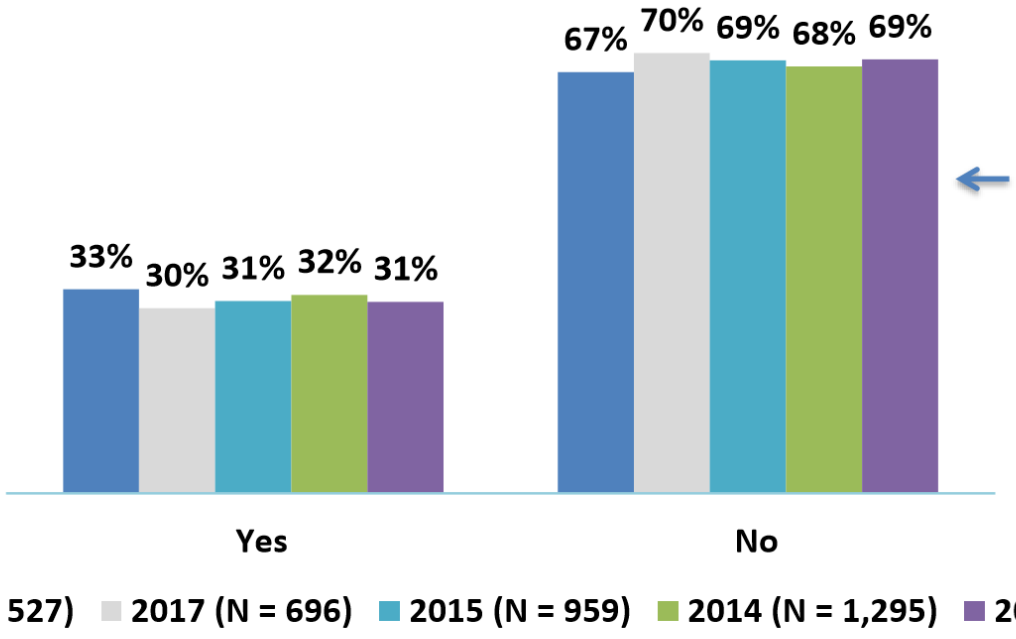


Just As A Sample: Language Programming



Just As A Sample: FPGA in Embedded Marketing

Does your current embedded project incorporate an FPGA chip?

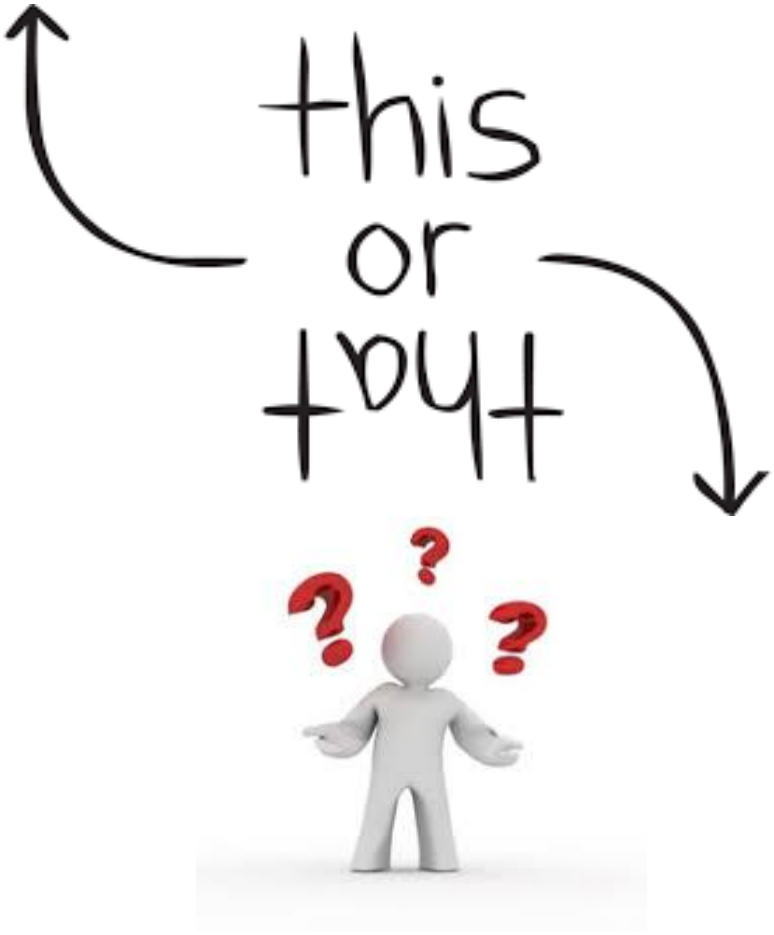


Among those not using FPGAs, only **13%** said the trend towards FPGAs with built in multicore processors would change their mind.

27% of all respondents said they would use an FPGA in their **next** project. Those **not** using FPGAs in the future say they "don't need the functionality," "FPGAs are too expensive," "consume too much power," "are too difficult to program."

EE Times embedded

Which Platforms?

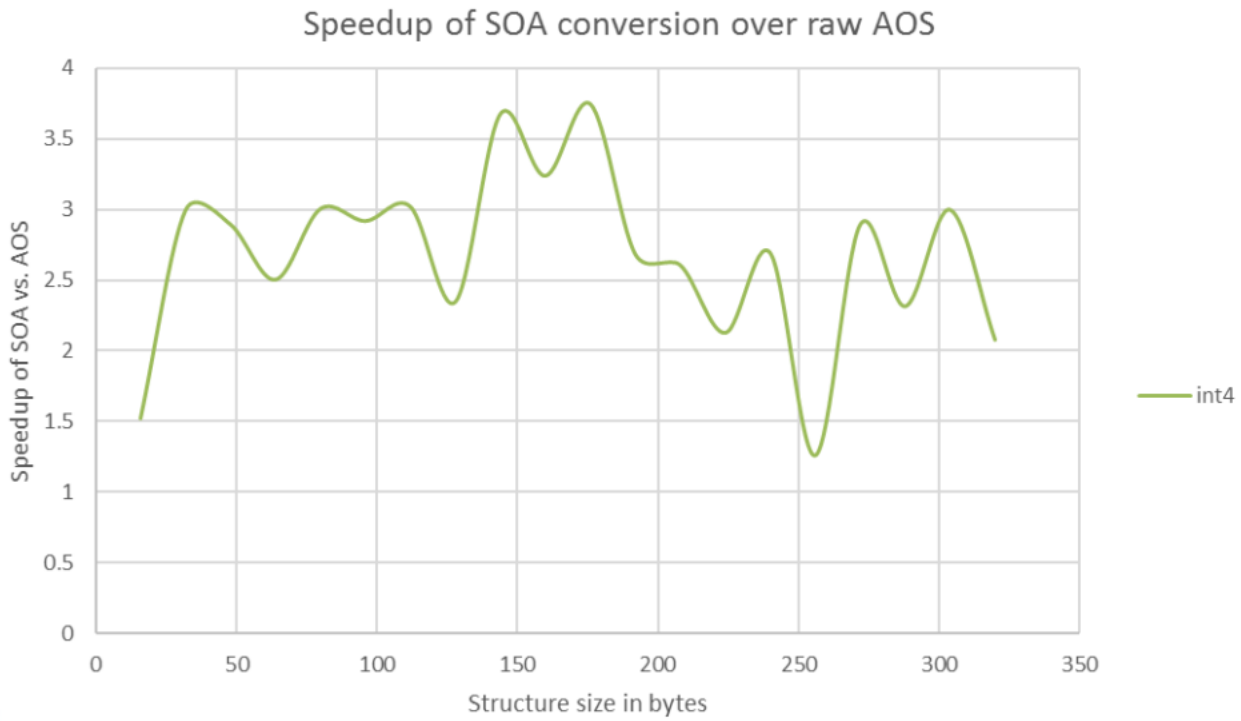


Platform Trend

- **Application Specific Integrated Circuits**

Hardware Effects on Efficiency of Programs

- More details later in the course



Array-of-Structures

```
#define NPTS 1024 * 1024

struct Coefficients_AOS {
      double u[3];
      double x[3][3];
      double p;
      double rho;
      double eta;
};

Coefficients_AOS gridData[NPTS];
```

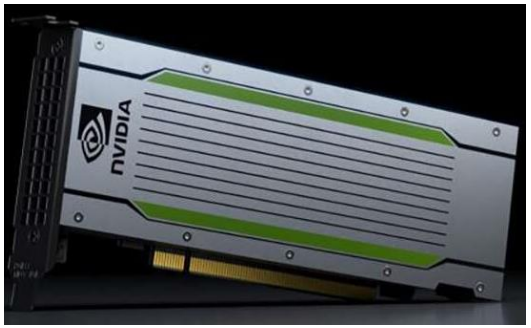
Structure-of-Arrays

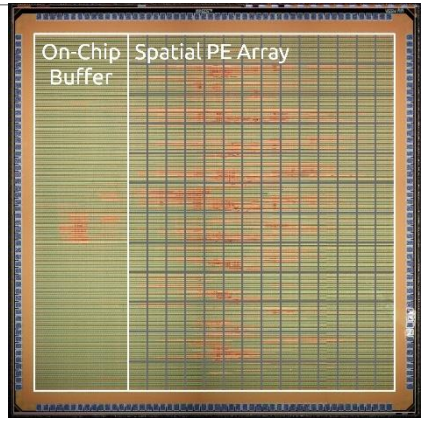
```
#define NPTS 1024 *1024

struct Coefficients_SOA {
      double u[3][NPTS];
      double x[3][3][NPTS];
      double p[NPTS];
      double rho[NPTS];
      double eta[NPTS];
};

Coefficients_SOA gridData;
```

"CUDA Optimization Tips, Tricks and Techniques," by Stephen Jones, GTC17.

How to Realize the Ideas?

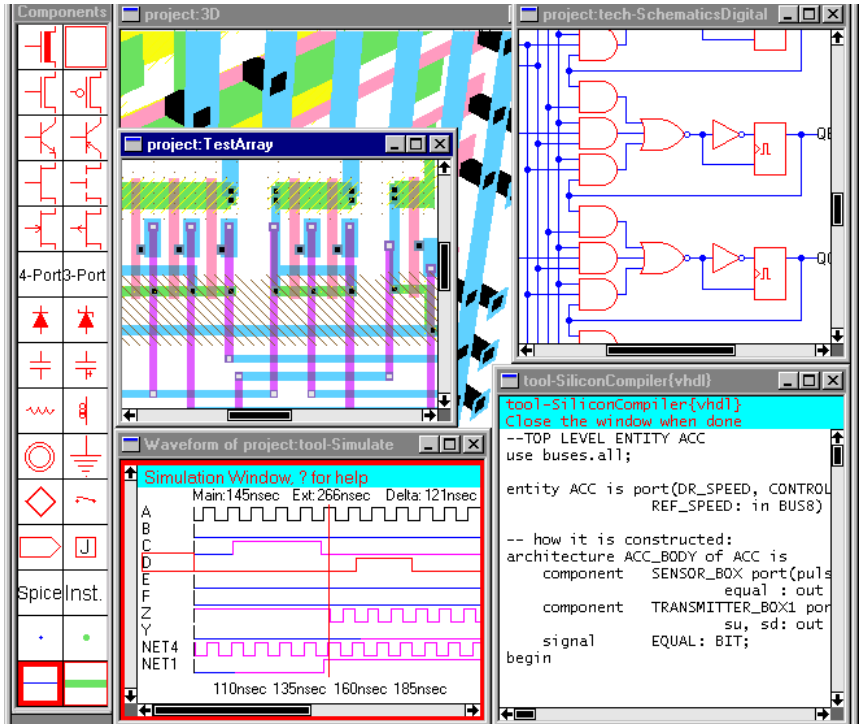
- Digital system design
  - While **satisfying** requirements
- *Technology Mapping*
  - Application Specific ICs (ASICs)
  - Programmable Logic Device (PLDs)
  - Field Programmable Gate Arrays (FPGA)
- Synthesis concepts
  - ASIC
  - FPGA





How to Accelerate Realizing Ideas?

- *Hardware description languages (HDLs)*
  - Verilog
  - VHDL
- *Simulation and verification*
  - *Testbench*
- *CAD tools*
  - *Modelsim*
  - *Design Compiler*

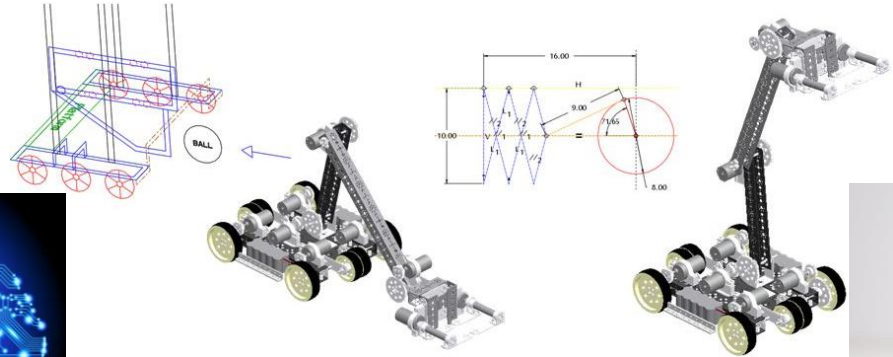


How About Job Opportunity?

- More than **80%** of job opportunities in **EDA** companies
  - Synopsys
  - Mentor
  - Cadence

Summary of DSD Goals

Computer Aided Design



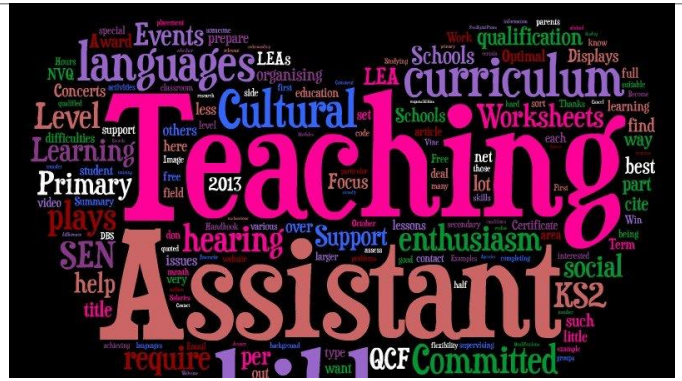
How to Achieve These Goals?

Class Information

- Class hour
  - Sun & Tue: 13:30-15:00
- Instructor
  - Hajar Falahati
- Contact info
  - hfalahati@ipm.ir

Teaching Assistant

- TA team
  - Saba Moustofi
  - Saman Mohseny
  - Majid Taherkhani
  - Fatemeh Khashei
  - Mohammadali Pashanj



- Class TA hour
  - Will be announced

References

- **Verilog® HDL: A Guide to Digital Design and Synthesis**, Second edition by *Samir Palnitkar*
- **Verilog Digital System Design , RT Level Synthesis, Testbench and Verification**, Second edition by *Zainalabedin Navabi*
- **Digital-System-Design-with-VHDL-2e**, Second edition by *Mark Zwlin'ski*
- **Digital VLSI System Design: A Design Manual for Implementation of Projects on FPGAs and ASICs using Verilog**, by *Seetharaman Ramachandran*

Class Policy

- Attend the class **on time**
  - Sun & Tue: 13:30-15:00

- Cell Phones **off** or on **silent**

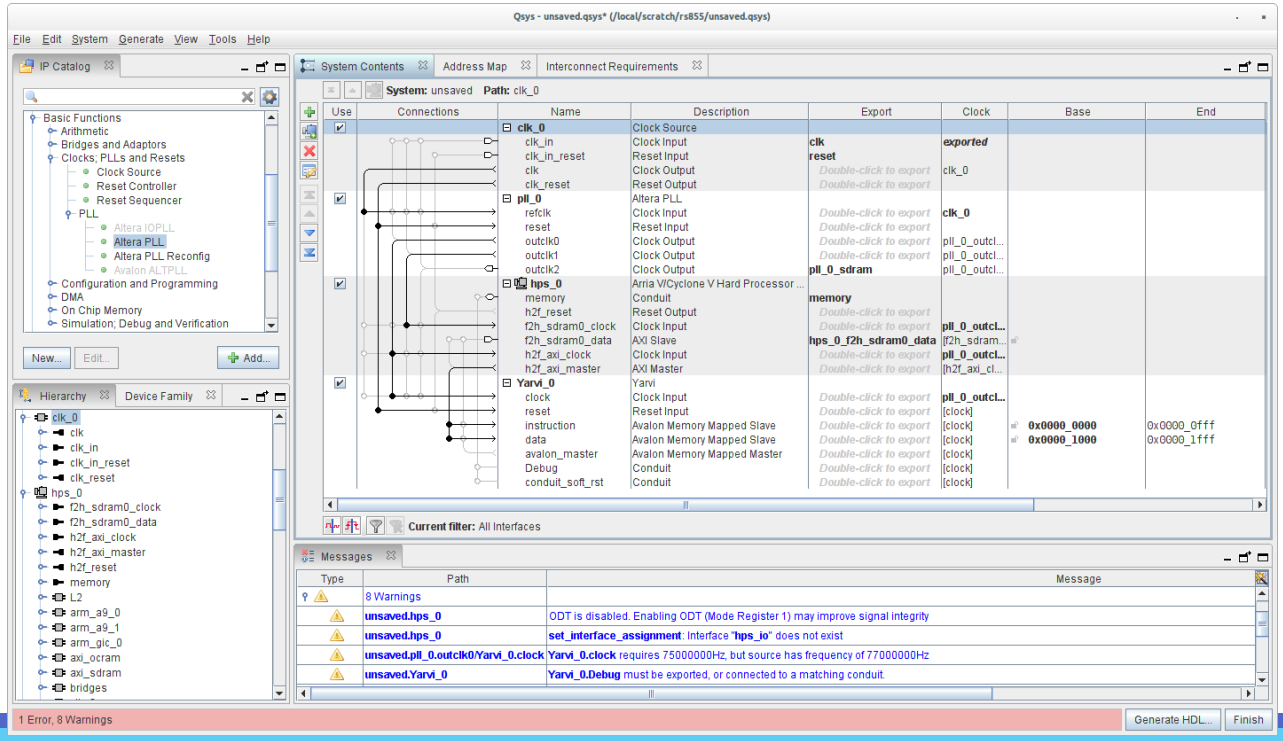
- Food **no, Water yes!**

- Ask Questions **anytime**
  - Don't hesitate to ask even stupid questions!!!

- Pass me your **feedback/thought**
  - Anything related to the course

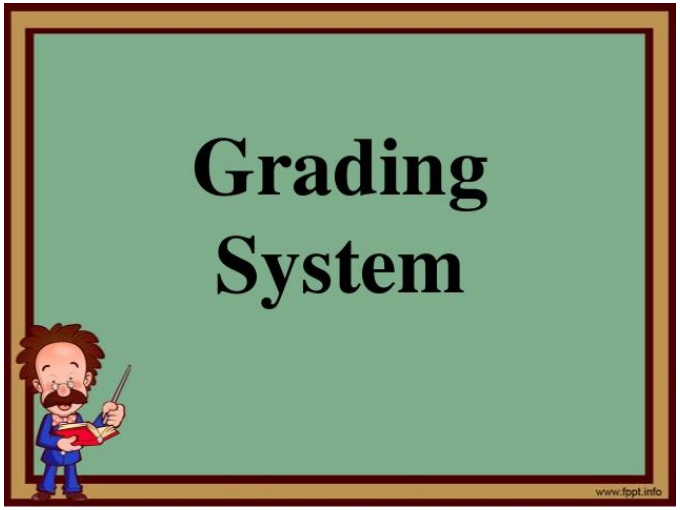
Design Sessions

- Implement what we learn in the class



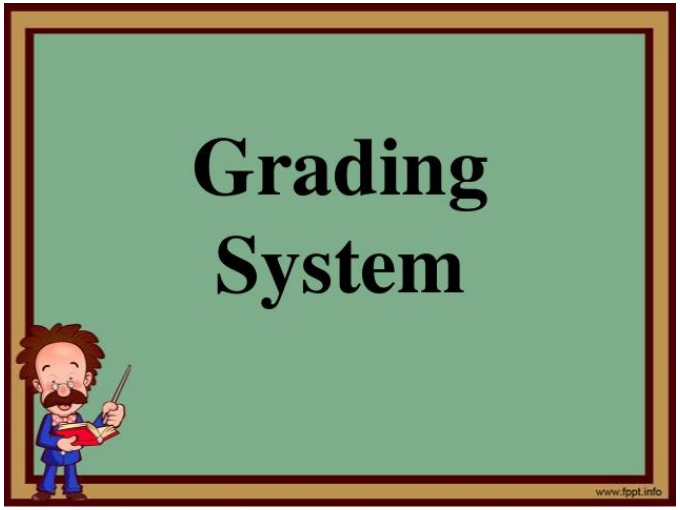
Grading (1)

- Exams: 50%
  - Midterm: 20%
  - Final: 30%
    - 1400/02/15 - 16:00 PM
- Assignments & Projects: 30 - 20%
  - Design Sessions
  - Theorical and practical assignments
  - Practical project
    - Bonus points for outstanding projects
    - Up to 25%
- Quiz and class activity: 5%



Grading (2)

- Exams: 45%
  - Midterm: 15%
  - Final: 30%
    - 1400/02/15 - 16:00 PM
- Assignments & Projects: 35 - 20%
  - Design Sessions
  - Theorical and practical assignments
  - Practical project
    - Bonus points for outstanding projects
    - Up to 25%
- Quiz and class activity: 5%



Assignments

- Deadlines
  - **Tight!**
  - 5 days late is **allowed**!

- Discussion is **allowed**

- Copied assignments and academic misconduct is **zero score**

Academic Misconduct

- Using someone else's assignments/projects/…..
- Using code from someone who took course before or has done the project
- Cheating in exams and assignments

Evaluation Policies

- Exam contents
  - Topics of this **Class** and **TA Classes**

- Grading rules for checking yourself
  - **Accepted score** in assignments, project, midterm, final Exam is **50%**.
  - **Accepted** assignment deliver rate is at least **80%.**

Projects

- Project topic:
  - Check your around
  - Modeling
  - Implementation
  - Synthesis

- Project team:
  - 1-2 students

Projects: Steps

- Topic Selection

- Specification
  - Project proposal
  - Challenges

- Modeling
  - ASM/FSM
  - Block diagram

- Design
  - HLL/HDL
  - Documentation

- Realization
  - Implementation
  - Synthesis

Projects: Phases

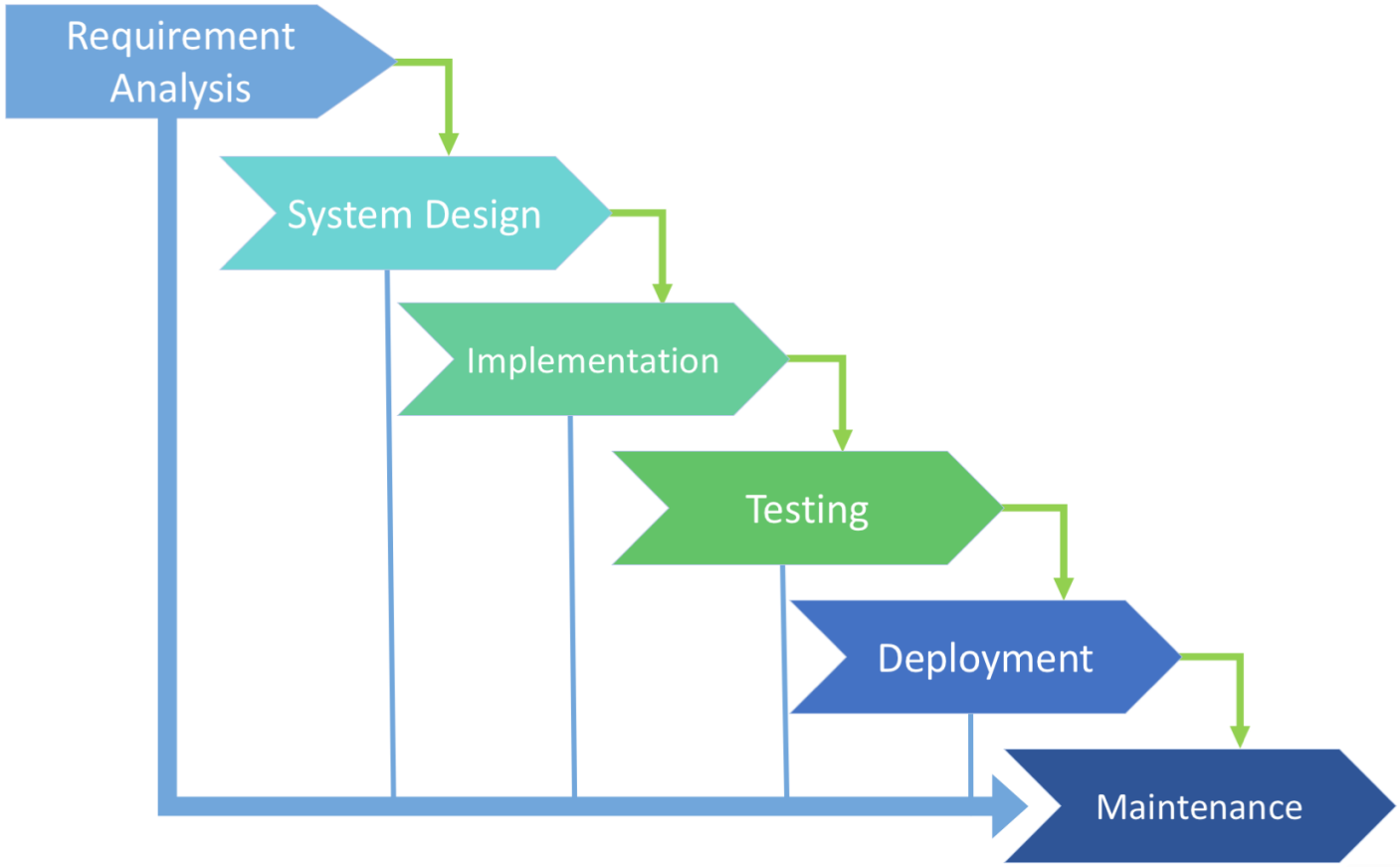
- Topic selection & proposal

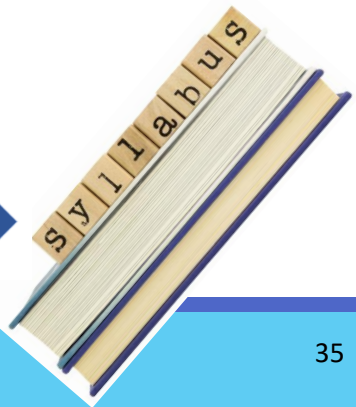
- Modeling and design: 50%
  - Modeling
  - Design (50%)
  - Mid of Ordibehest

- Realization
  - Design (100%)
  - Implementation
  - Synthesis
  - Documentation

Course Syllabus at A Glance

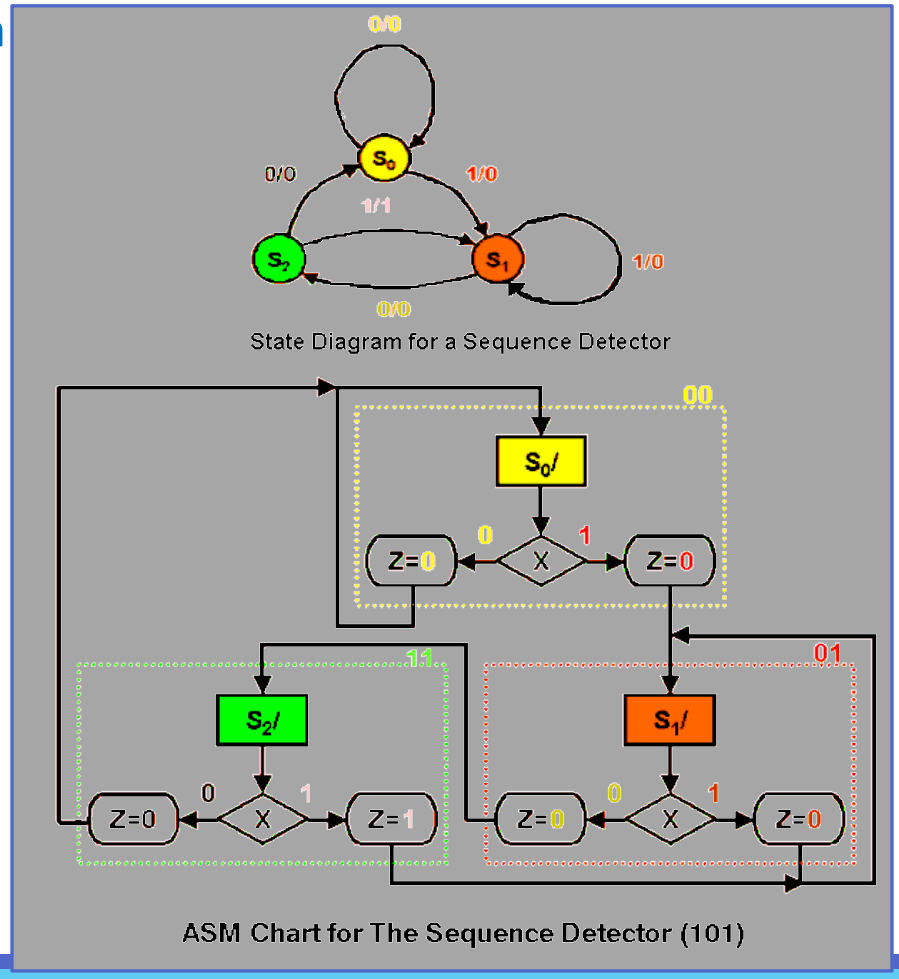
- Digital System Design (DSD)





Course Syllabus In Detail

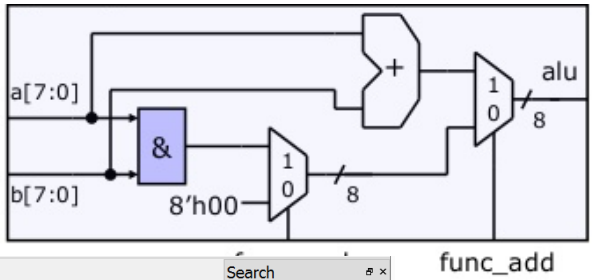
- Introduction on digital system design
  - Samples
- Hardware design
  - Approaches
  - FSM
  - ASM
  - Design Sample



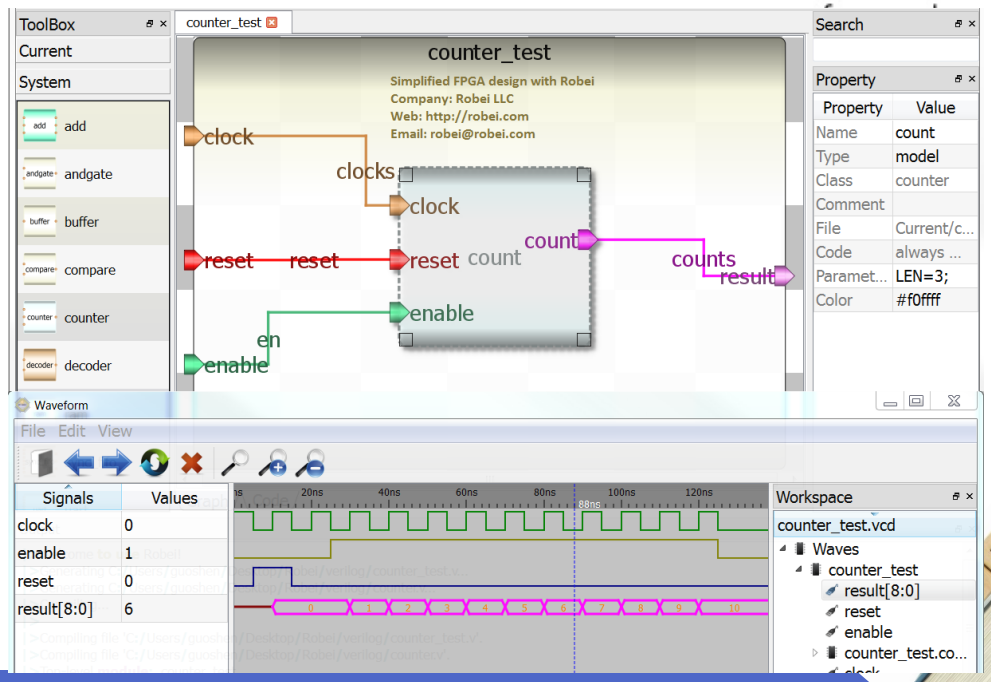
Course Syllabus in Detail (cont'd)

- Hardware Description Languages (HDLs)
  - Why HDLs?
  - Key features of HDLs
  - Verilog
  - VHDL

```
If (func_add)
   alu = a + b;
else if (func_and)
   alu = a & b;
Else
   alu = 8'h00;
```



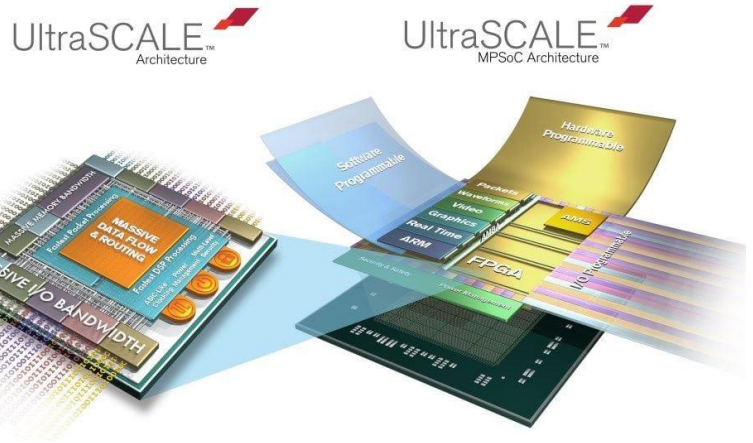
- Verilog
  - Concepts
  - Modeling levels
    - Behavioral-level
    - RTL-level
    - Gate-level
    - Switch-level
  - Testing
  - Synthesis



Course Syllabus in Detail (cont'd)

- Technology Mapping
  - Application Specific Integrated Circuits (ASIC)
  - Programmable Logic Device (PLD)

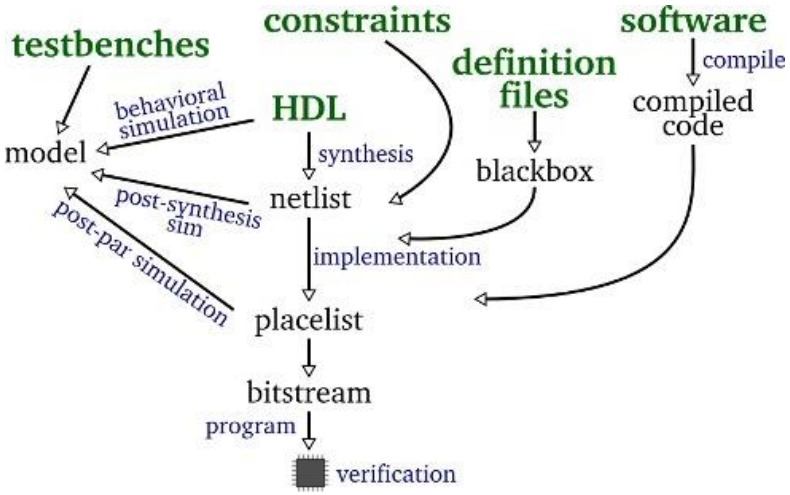
- PLDs
  - SPLDs
  - CPLDS
  - FPGAs

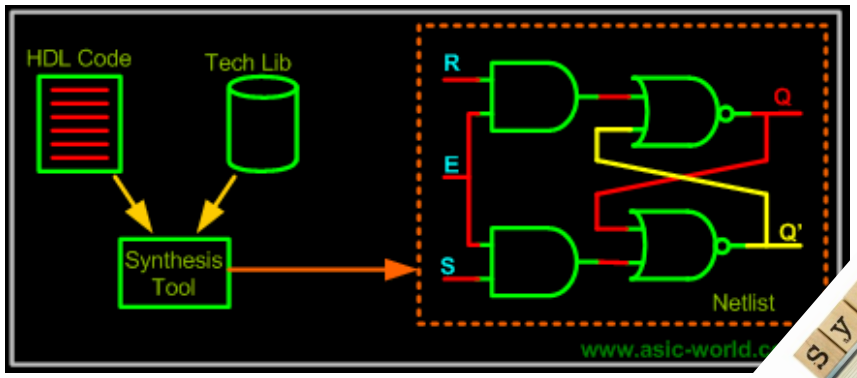


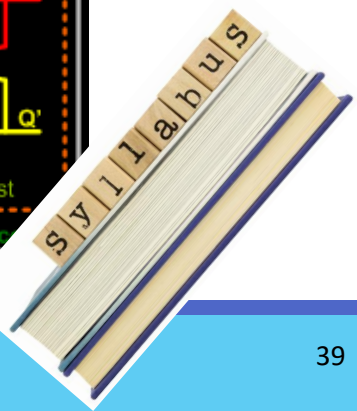
- FPGAs
  - Design

Course Syllabus in Detail (cont'd)

- Test and verifications
  - Simulation
  - Testbench design
- Synthesis
  - Techniques
  - Tools
  - Samples

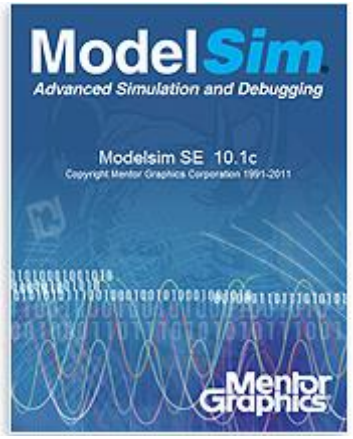




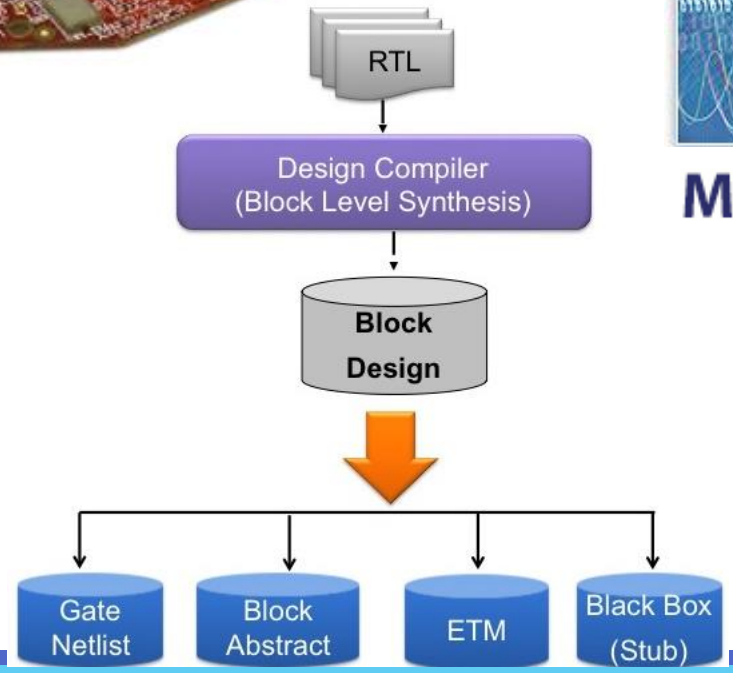


Tools

- Modelsim
  - Simulation
- Xilinx ISE tool set
  - FPGA synthesis
- Synopsys design compiler
  - ASIC synthesis



ModelSim SE



Thank You