SULLIVAN48 Reference Data

Name, Mnemonic		*Format*	Operation (in SystemVerilog)		Funct
Add	`ADD`	D	R[rd] = R[rs] + R[rt]		001000
Add immediate	`ADDI`	DI	R[rd] = R[rs] + SignExtImm	(1)	101000
Subtract	`SUB`	D	R[rd] = R[rs] - R[rt]		000100
Subtract immediate	`SUBI`	DI	R[rd] = R[rs] - SignExtImm	(1)	100100
Multiply	`MUL`	D	R[rd] = R[rs]×R[rt]		000010
Multiply immediate	`MULI`	DI	R[rd] = R[rs]×SignExtImm	(1)	100010
Compare	`CMP`	D	R[rs] - R[rt] $\stackrel{?}{=}$ 0		011111
Compare immediate	`CMPI`	DI	R[rs] - SignExtImm $\stackrel{?}{=}$ 0	(1)	111111
Vectorial sum	`VES`	D	R{rd[47:32]} = R{rs[47:32]} + R{rt[47:32]} R{rd[31:16]} = R{rs[31:16]} + R{rt[31:16]} R{rd[15:0]} = R{rs[15:0]} + R{rt[15:0]}		000000
Concatenation	`CNC`	D	R[rd] = ConcatRegister	(2)	000110
Escalated vector	`SCL`	D	R{rd[47:32]} = R{rs[47:32]}× R[rt] R{rd[31:16]} = R{rs[31:16]} × R[rt] R{rd[15:0]} = R{rs[15:0]} × R[rt]		011000
Dot Product	`DOT`	D	R[rd] = R{rs[47:32]}×R{rt[47:32]} + R{rs[31:16]} × R{rt[31:16]} + R{rs[15:0]} × R{rt[15:0]}		011010
Read value from kernel memory	`REK`	D	R[rd] = M[ConcatRegister] R{rd[47:32]} = M{ConcatRegister}[47:32]	(2)	000110
Read vector from kernel memory	`RKM`	D	R{rd[31:16]} = M{ConcatRegister}[31:16] R{rd[15:0]} = M{ConcatRegister}[15:0]	(2)	100110
Reads pixel vector from picture ROM	`REP`	D	R[rd] = M[ConcatRegister]	(2)	000110
Saves new pixel in picture RAM	`SAP`	D	M[R[rd]] = R[rs]		001000
Branch	`B`	C	PC = PC + 8 + BranchAddr	(3)	000000
Branch on equal	`BEQ`	C	PC = (Z $\stackrel{?}{=}$ 0)? PC + 8 + BranchAddr : PC	(3)	100000

(1) SignExtImm = {36{Immediate[11]},Immediate[11:0]}

(2) ConcatRegister = {16'b0,R[rs](15:0),R[rt](15:0)}

(3) BranchAddr = {22{Immediate[23]},Immediate[23:0],2'b0}

Basic Instruction Formats