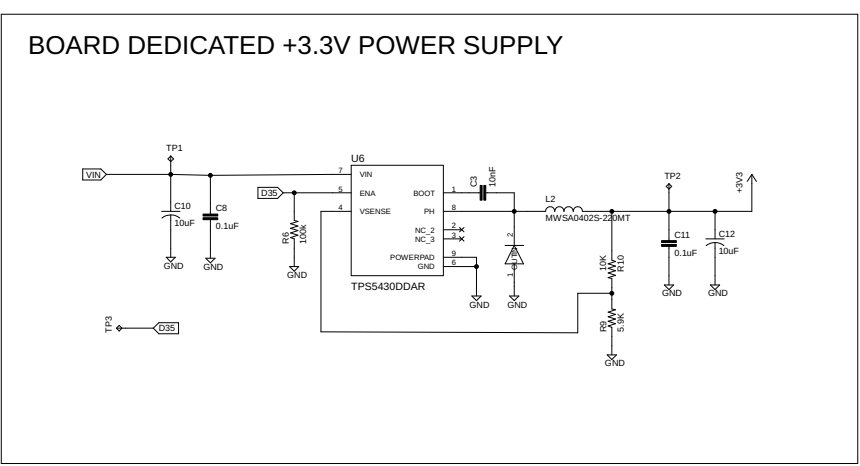
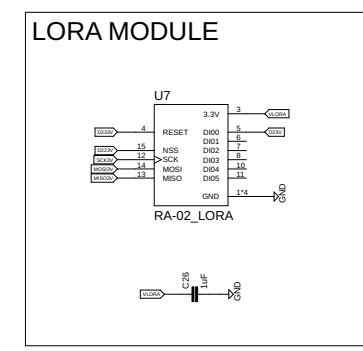
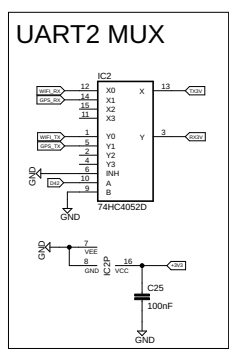


## BOARD DEDICATED +3.3V POWER SUPPLY

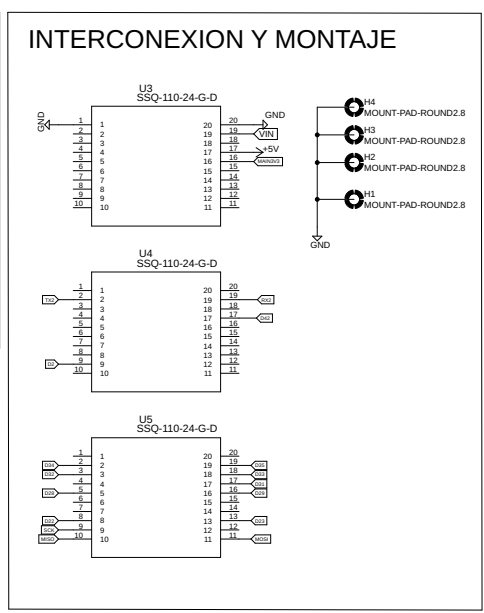
The schematic diagram illustrates a dedicated +3.3V power supply circuit. It begins with a VIN input, which is connected to a network of capacitors (C10, C8) and a diode (D35) for input filtering and protection. The circuit then passes through a resistor (R6) and a diode (D35) before entering the TPS5430DDAR DC-DC converter (U6). The converter's output is filtered by a capacitor (C1) and an inductor (L2, MWSA0402S-220MT) to produce a stable +3V3 output. The output is further filtered by capacitors C11 and C12. The circuit includes several test points (TP1, TP2, TP3) and resistors (R9, R10) for monitoring and regulation. The TPS5430DDAR is configured with its VIN, ENA, BOOT, PH, VSENSE, NC\_2, NC\_3, and POWERPAD GND pins connected to the appropriate components and ground.



# LORA MODULE

[illegible]

# INTERCONEXION Y MONTAJE



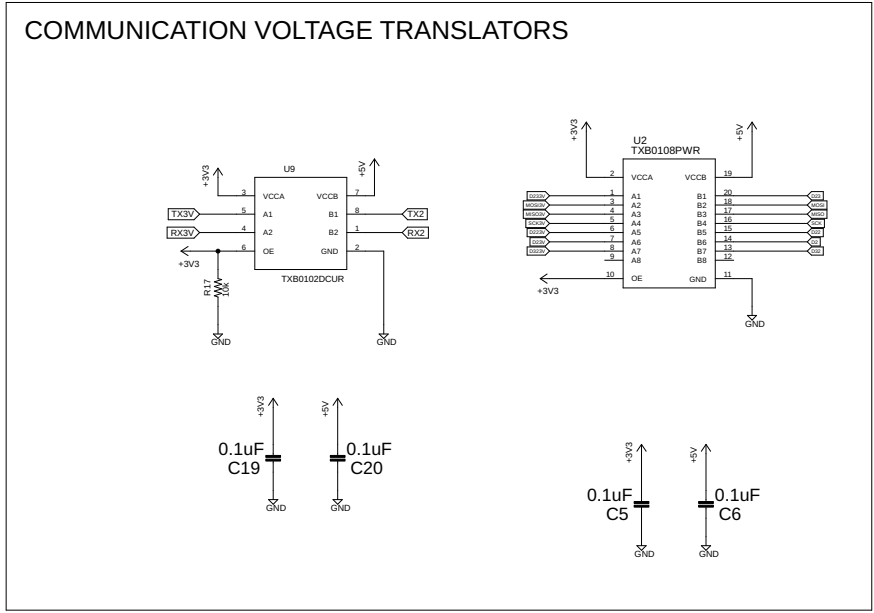
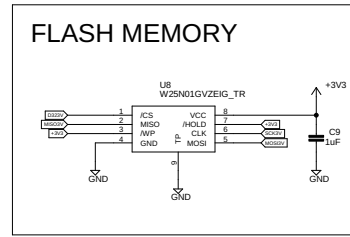
# COMMUNICATION VOLTAGE TRANSLATORS

The image displays two circuit diagrams for communication voltage translators, specifically the TXB0102DCUR and TXB0108PWR.

**TXB0102DCUR (U9):** This circuit is configured as a bidirectional level shifter between a 3V3 domain and a 5V domain. The 3V3 supply is connected to the VCCA pin (pin 3), and the 5V supply is connected to the VCCB pin (pin 7). The OE pin (pin 6) is pulled up to 3V3 by a 10k resistor (R17). The A1 pin (pin 5) is connected to TX3V, and the B1 pin (pin 8) is connected to TX2. The A2 pin (pin 4) is connected to RX3V, and the B2 pin (pin 1) is connected to RX2. The GND pin (pin 2) is connected to ground.

**TXB0108PWR (U2):** This circuit is configured as an 8-channel bidirectional level shifter between a 3V3 domain and a 5V domain. The 3V3 supply is connected to the VCCA pin (pin 2), and the 5V supply is connected to the VCCB pin (pin 19). The OE pin (pin 10) is pulled up to 3V3. The A1 through A8 pins (pins 1, 3, 4, 5, 6, 7, 8) are connected to TX0V through TX7V. The B1 through B8 pins (pins 20, 18, 17, 16, 15, 14, 13) are connected to RX0V through RX7V. The GND pin (pin 11) is connected to ground.

**Capacitors:** Two capacitors, C19 and C20, are shown with a value of 0.1uF, connected between the 3V3 and 5V supply rails to ground. Similarly, two capacitors, C5 and C6, are shown with a value of 0.1uF, connected between the 3V3 and 5V supply rails to ground.

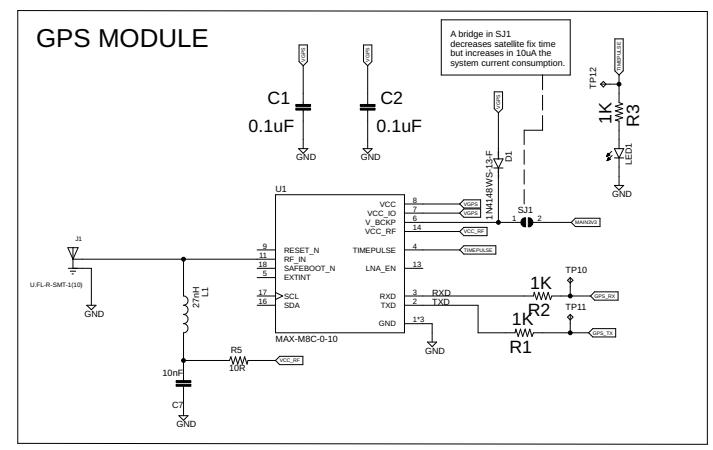
[illegible]

# TEST POINT

TP1: VIN  
TP2: Board +3.3V controlled power supply  
TP3: Power supply control pin D35  
TP4: VGPS  
TP5: VGPS control pin D34  
TP6: VLoRa  
TP7: VLoRa control pin D33  
TP10: GPS Rx  
TP11: GPS Tx  
TP12: GPS Timepulse  
TP13: WWIFI  
TP14: WWIFI control pin D31

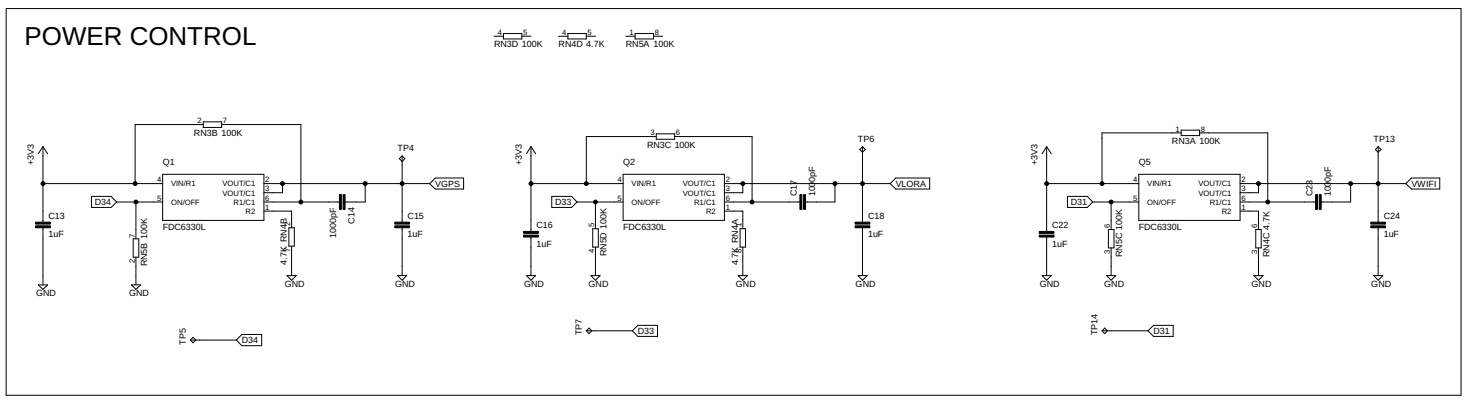
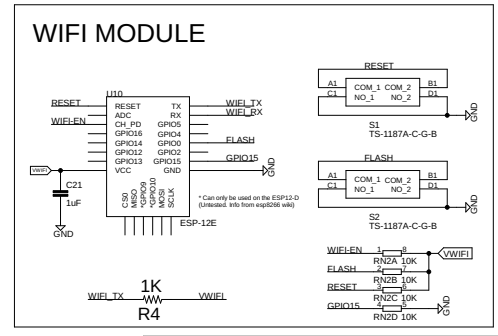
# TEST POINT

TP1: VIN  
TP2: Board +3.3V controlled power supply  
TP3: Power supply control pin D35  
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TP5: VGPS control pin D34  
TP6: VLoRa  
TP7: VLoRa control pin D33  
TP10: GPS Rx  
TP11: GPS Tx  
TP12: GPS Timepulse  
TP13: WWIFI  
TP14: WWIFI control pin D31

[illegible]

# POWER CONTROL

The diagrams show three power control circuits for different components: VGPS, VLORA, and VAWIF1. Each circuit is powered by a +3V3 supply and includes a decoupling capacitor (C13, C16, C22) and a diode (D34, D33, D31). The VGPS circuit uses MOSFET Q1 and resistor RNSB. The VLORA circuit uses MOSFET Q2 and resistor RNSC. The VAWIF1 circuit uses MOSFET Q5 and resistor RNSA. All circuits include a 4.7k resistor (RMA8, RMA4, RMA4) and a 1000pF capacitor (C14, C17, C18) for signal conditioning. The output of each circuit is connected to a test point (TP4, TP6, TP13) and a 1uF capacitor (C15, C24) for filtering.

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