COMPUTER ARCHITECTURE III: Course overview

CATALOG DESCRIPTION

Multiprocessor systems: vector processors, array processors, SIMD, MIMD systems. Interconnection networks. Multiprocessor architecture and programming. Multiprocessing control and algorithms. The PRAM model and algorithms. Message-passing models and algorithms. Scheduling and arbitration algorithms. Parallel virtual machine. Message passing interface. Performance measures for multiprocessor systems.

INSTRUCTOR AND TEACHING ASSISTANTS

Course staff	Name	E-mail address	Fall 2014 Office Hours	Location
Instructor	Miodrag Bolic	mbolic@site.uottawa.ca	Wednesdays, 12:00-13:00,	CBY A-616
Teaching assistants			By e-mail	

TIME and LOCATIONS

Section	Activity	Day	Location
CEG4136 A00 (September 06 - December 06)	LEC	Friday 11:30 - 13:00	MNO C211
CEG4136 A00 (September 06 - December 06)	LEC	Wednesday 13:00 - 14:30	STE F0126

Section	Activity	Day	Location
CEG4136 A01 (September 06 - December 06)	LAB	Monday 19:00 - 22:00	STE 2061

Section	Activity	Day	Location
CEG4136 A02 (September 06 - December 06)	TUT	Monday 13:00 - 14:30	STE F0126

TEXTS

Parallel Computer Organization and Design, by Michel Dubois, Murali Annavaram, Per Stenström, August 2012

Recommended:

*Real World Multicore Embedded Systems, 1*st Edition, edited by B. Moyer, 2013.

Computer Architecture: A Quantitative Approach, by **John L. Hennessy**, **David A. Patterson**, **David Goldberg**, Morgan Kaufmann; 3rd edition, 2002.

ADDITIONAL DOCUMENTS

Appendix E from *Computer Architecture: A Quantitative Approach* together with the **slides**.
- Material about superscalar and VLIW processors, multiprocessors on a chip will be added.

- Parallella resources such as http://adapteva.com/docs/epiphany_arch_ref.pdf

PREREQUISITES

CEG3136.

GRADES

6% Participation

24% Quizzes

32% Final

8%, 15min in-class presentation

12% Labs + 18%Project, or 30% Project

The final mark will be computed using the weighted sum of **ALL** of the above components. You need to have 50% of the exam component that includes Final and Quizzes
The quizzes will be on DGD during the weeks of September 25, October 30, November 20.

EXAMS (FINAL)

- All exams are closed book.
- Only material cover in the class and tutorials will be on the exam.

QUESTIONS ABOUT MARKS

If you have a question about a mark you have received, this is the procedure (all other questions on marks will be ignored)

- Schedule an appointment with the T.A. to see the work (if required).
- Fill out and sign form (obtained from T.A., or **download it here** – thanks to dr. Andy Adler for developing the form)
- Submit to T.A.
- You will receive a response within two weeks.

GRADING

Name	Quiz	Lab	Project or literature study	Exams
Miodrag Bolic	-	-	-	Final
TA	All	Labs	Reports	-

	quizzes			

COURSE OUTLINE

Introduction: Chapter 1

Cache memories: Chapter 4.3

Parallel-programming model abstractions and message passing MP systems: Chapter 5.2 and 5.3

Bus-based shared memory systems: Chapter 5.4

Scalable and cache only memory systems: Chapters 5.5 and 5.6

Interconnection networks: design space, switching and topologies: Chapters 6.2, 6.3 and 6.4

Routing and switching architectures: Chapters 6.5 and 6.6

Background and coherence: 7.2 and 7.3

Consistency: 7.4

Synchronization: 7.5

Multithreading: 8.2 and 8.3

Chip processor architectures and programming models: 8.4 and 8.5

Additional topics including superscalar, VLIW, DSP processors, GPUs and so on

LABS AND THE PROJECT

All the material about the Labs and the project is available on Virtual Campus.