8.2.7.3 Wallace Tree Multiplication

TABLE 8.4 An Adder as a 1's Counter

ABC	CS	Number of 1's
000	00	0
001	10	1
010	10	1
011	01	2
100	01	1
101	10	2
110	10	2
111	11	3

- In effect, a "one's counter": *A, B*, and *C* inputs and encodes them on *SUM* and *CARRY* outputs.
- A 1-bit full adder (FA) provides a ***3:2*** compression in the number of bits.

Ex: 6×6 Multiplier(table)

TABLE 8.5 A 6 × 6 Multiplier

					X5	X4	X3	X2	X1	X0	Multiplicand
					Y5	Y4	Y3	Y2	Y1	Y0	Multiplier
					X5Y0	X4Y0	X3Y0	X2Y0	X1Y0	X0Y0	
				X5Y1	X4Y1	X3Y1	X2Y1	X1Y1	X0Y1		
			X5Y2	X4Y2	X3Y2	X2Y2	X1Y2	X0Y2			
		X5Y3	X4Y3	X3Y3	X2Y3	X1Y3	X0Y3				
	X5Y4	X4Y4	X3Y4	X2Y4	X1Y4	X0Y4					
X5Y5	X4Y5	X3Y5	X2Y5	X1Y5	X0Y5						
P11 P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	Product

Seven bits Wallace tree addition

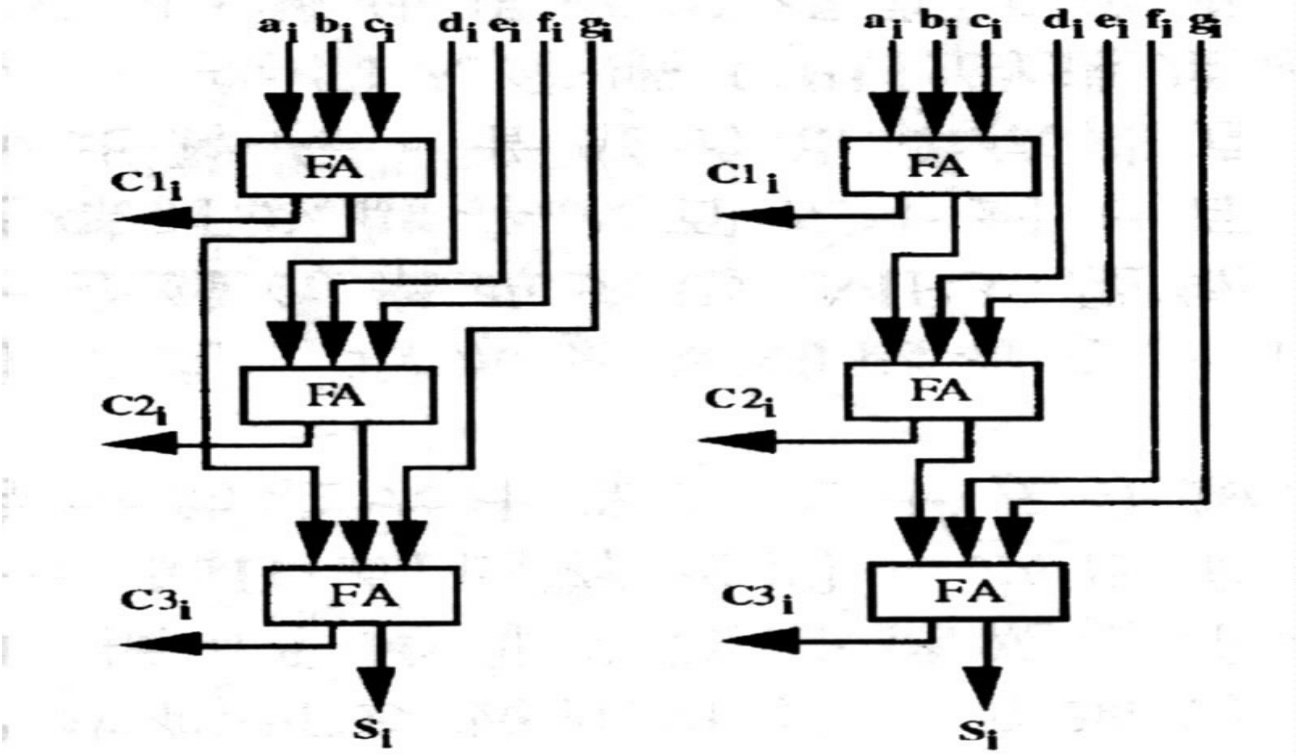
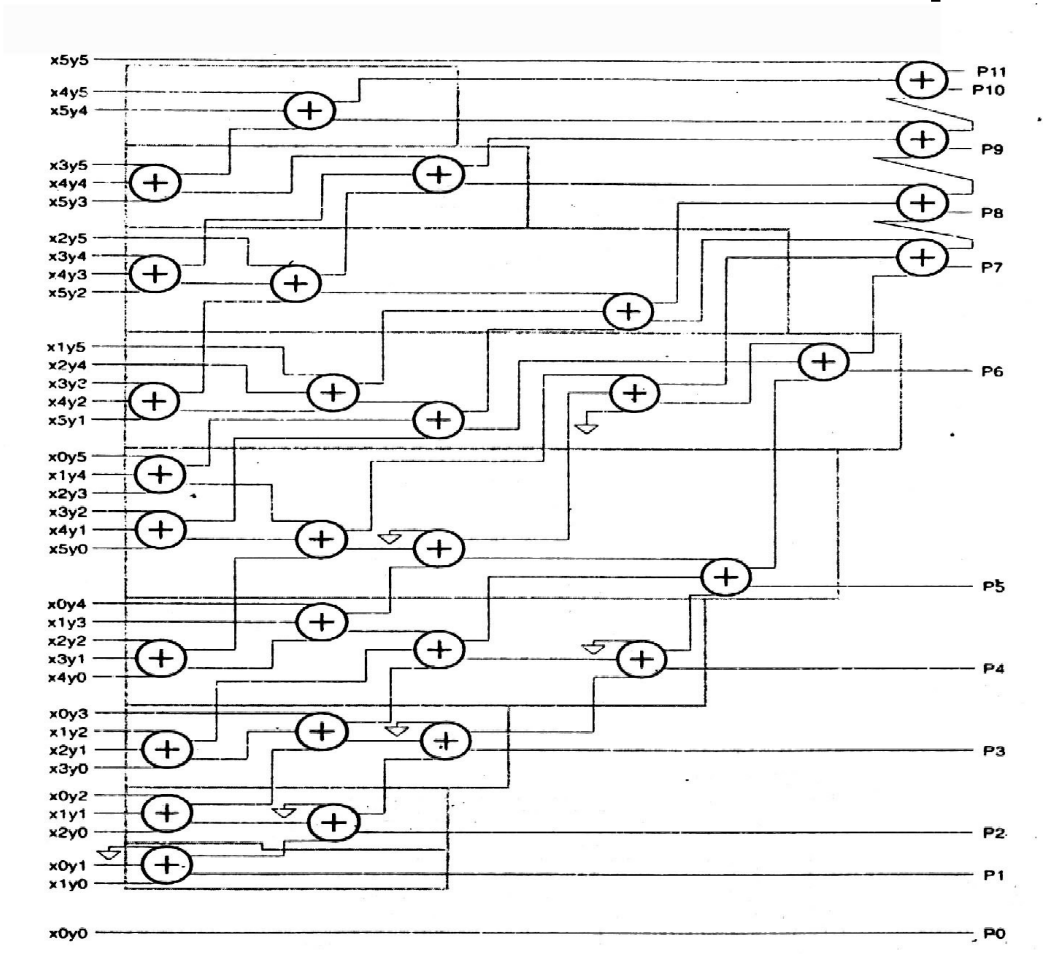


Fig. 2. Two examples of Wallace tree addition of seven bits

Ex: 6×6 Wallace Multiplier



Example

- In a 32-bit multiplier, the maximum number of partial products is 32 and the compressions are：

  32 → 22 → 16 → 12 → 8 → 6 → 4 → 3 → 2

  => There are 9 adder delays in the array

1. *c.f.* Array multiplier (Booth-recoded) =16
2. Can be used together with Booth-encoding scheme

Wallace Tree Multiplier

- *MxN* Booth-encoded multiplier (IEEE JSSC, vol.1,no.2, June 1993)

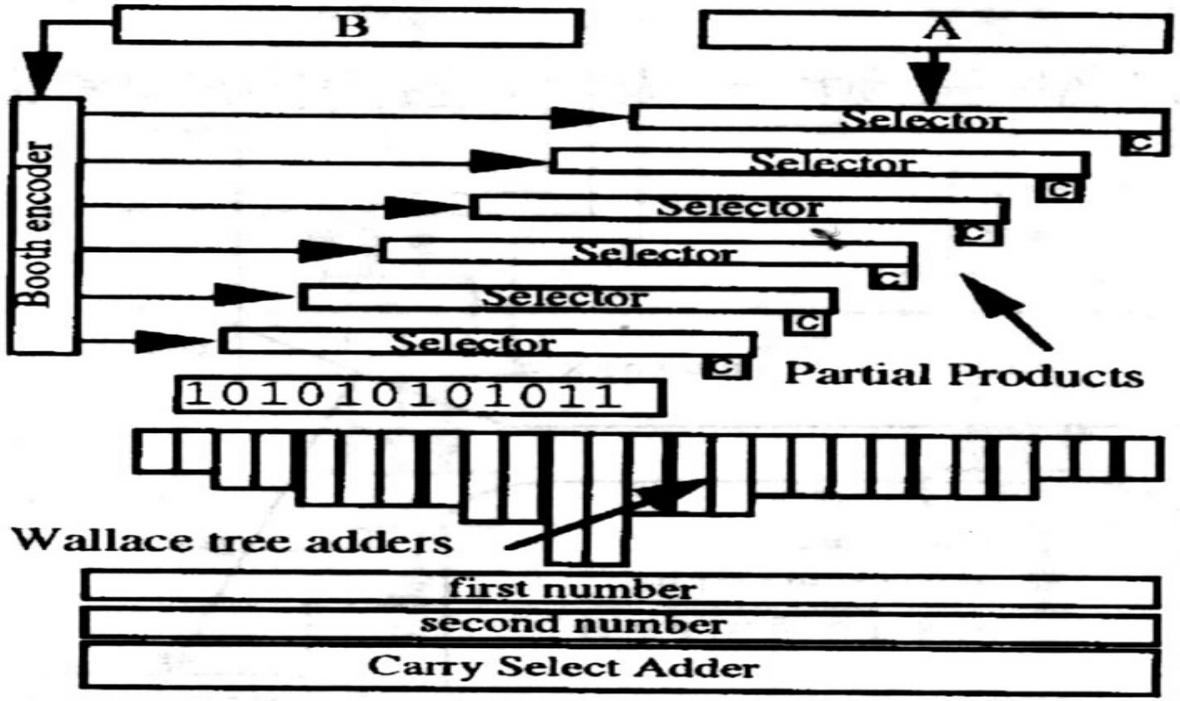
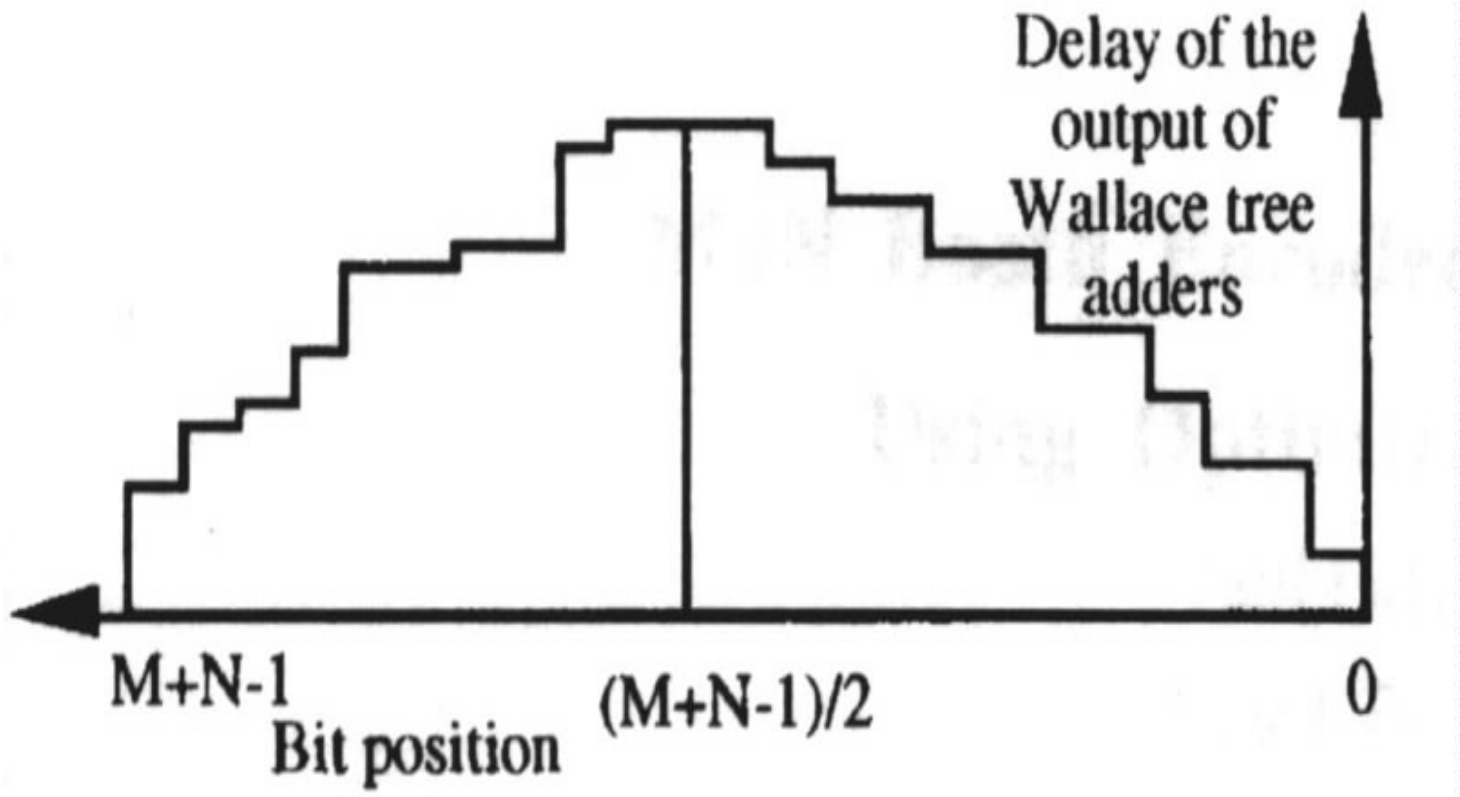


Fig.1. Block diagram of the parallel multiplier.

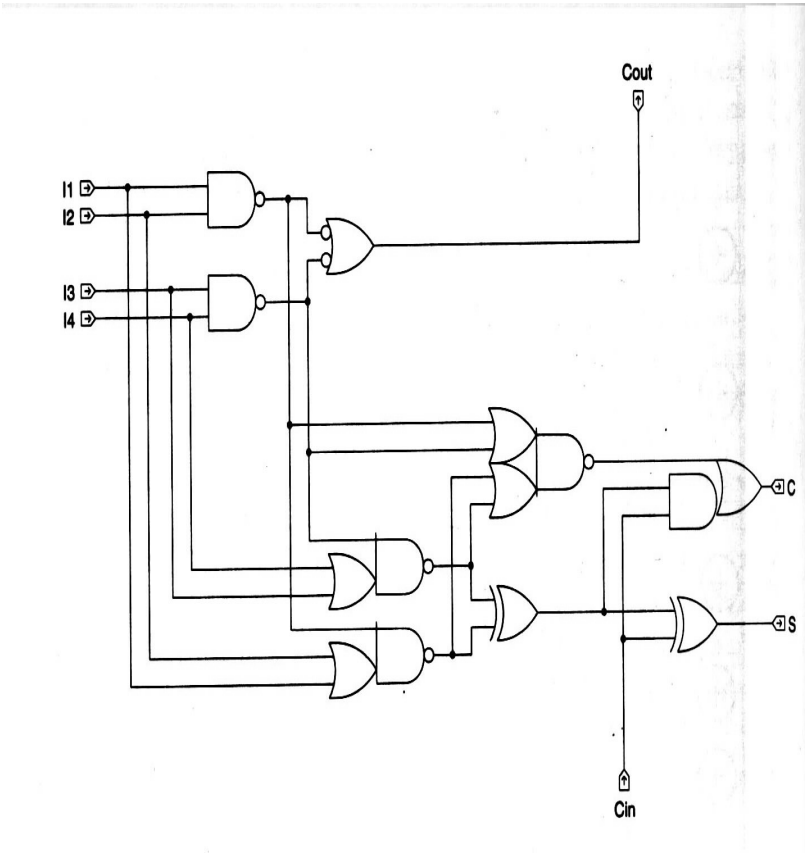
A typical delay distribution of the output of Wallace tree section



Extension

- 32-bits Wallace-tree multiplier has 9 adder delays in the array
- Questions:
  1. For a 64-bit multiplier, what is the minimum adder delay?
  2. Is there any way to reduce the delay by other compression scheme?

Approach:
Using 4：2 compression adder



- The 4:2 compression (really ***5:3***) has three XOR delays in the sum path.
- *c.f.*: Four XOR delays will be present if two adders are used

Reference

- A 54x54 regularly structured tree multiplier ,IEEE Journal of Solid-State Circuits (vol27 no.9, 1992)

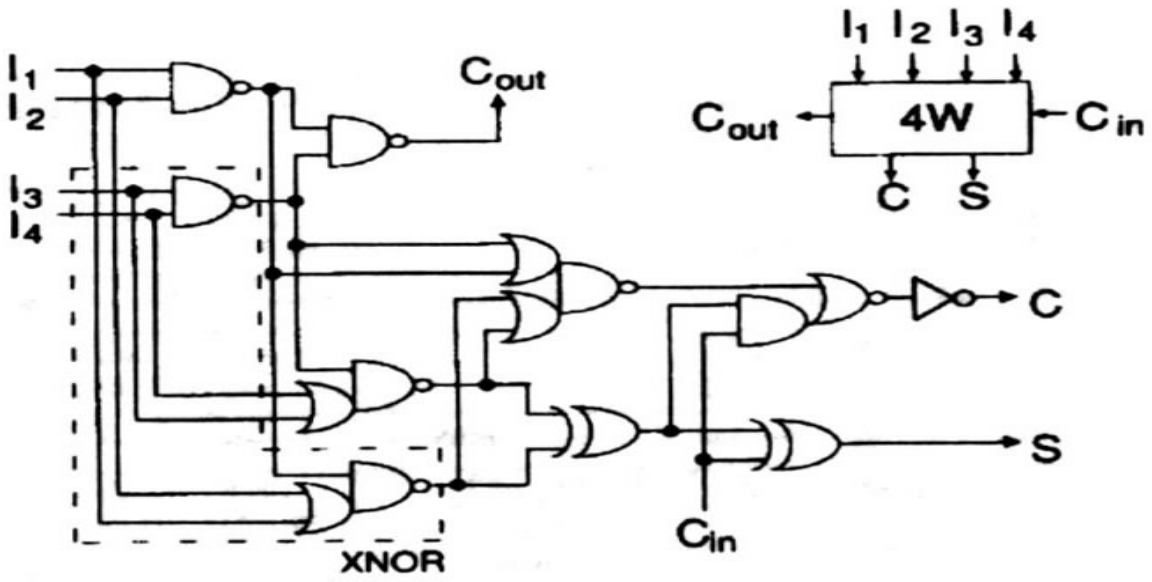


Fig. 4. Logic diagram of the 4W unit.