

Multipliers - Carry Save and Wallace Tree

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- 1 Carry Save Structures
- 2 Wallace Tree
- 3 Delay Trees
- 4 Fused Structures/MAC

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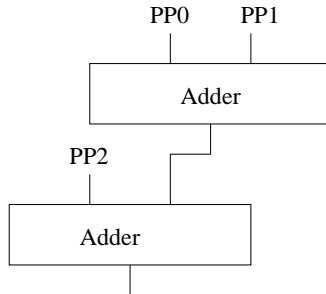
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- Remember that underlying technologies are always changing, the best way to build a circuit changes!

Carry Save Structures

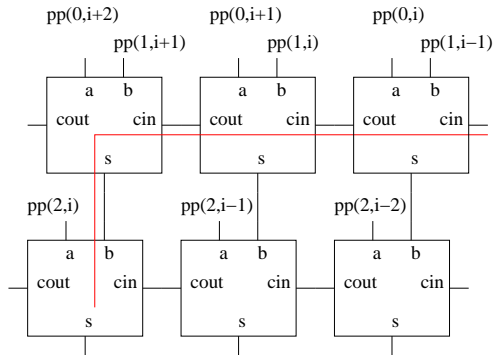
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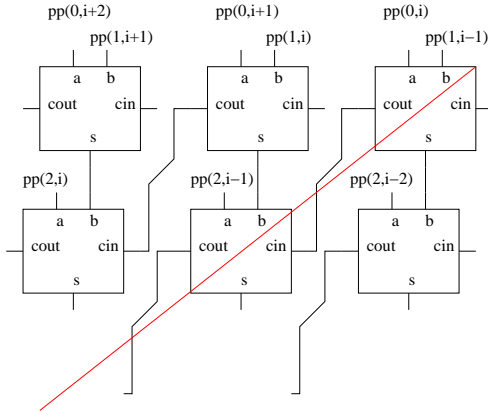
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- Note that for an array multiplier, the computation of the sum bit from an adder cell may also be on the critical path.
- This leads us to the carry save architecture.



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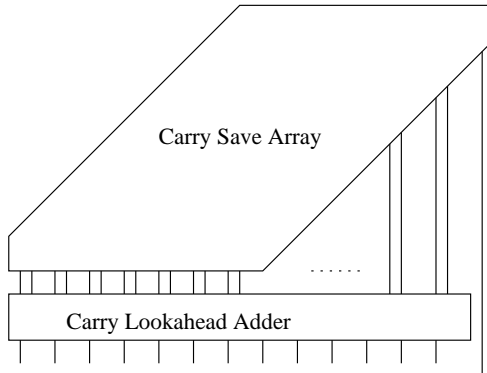
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- Since signal arrival times are not uniform, a variation on CLA may be used - the synthesis tool may be used for this.

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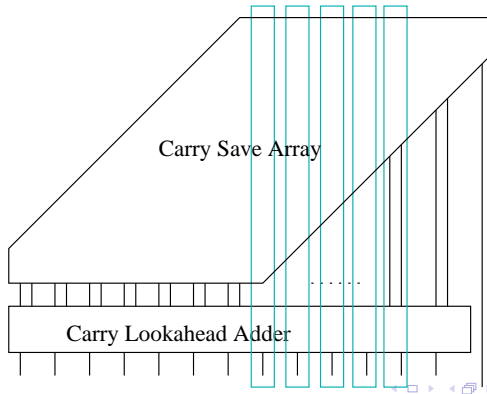


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- the last two sum bits in that column that are passed to the CLA.

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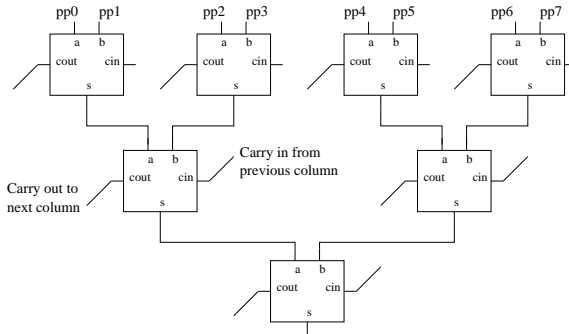
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- So in the Wallace tree multiplier we use a *tree* of adder cells.
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- In comparison to the basic array multiplier, the delay from partial products to final sum bits in a column is $O(\ln(n))$ rather than $O(n)$.

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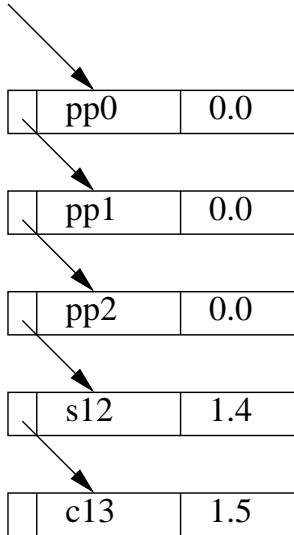
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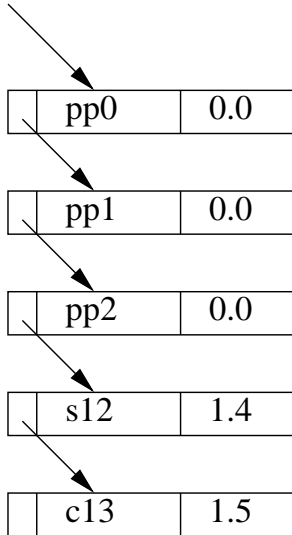
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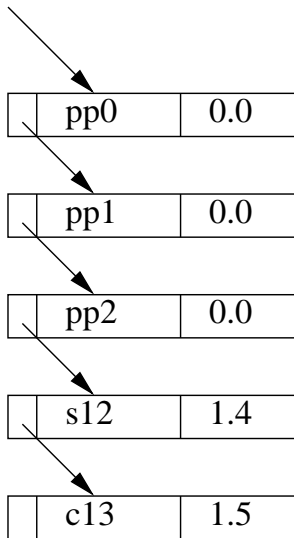
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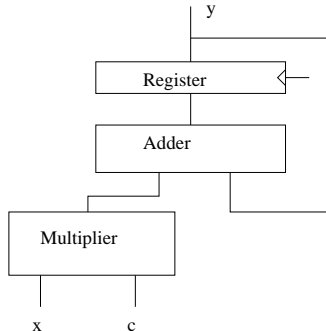
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- When two pass to CLA, when three use half adder and pass to CLA.

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- But we can still do better.

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- The same idea can be extended to equations such as $y = a * x + b * z$ and so on.
- These are referred to as *fused* multipliers.