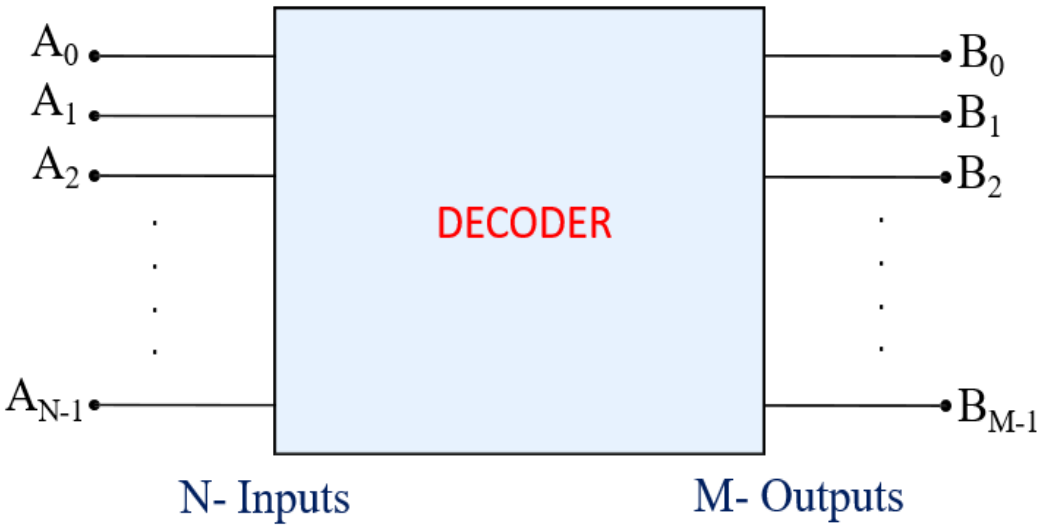
DECODER

Presented by Nabanita Das

DECODER

- Decoder is a combinational circuit.
- A decoder accepts a set of inputs that represents a binary number and activates only that output corresponding to the input number. All other outputs remain inactive.
- This is the block diagram of decoder with 'N' inputs and 'M' outputs.
- There are 2^N possible input combinations, for each of these input combination only one output will be HIGH (active) all other outputs are LOW
- Some decoder have one or more ENABLE (E) inputs that are used to control the operation of decoder.



Only one output is High for each input

2 TO 4 LINE DECODER

- Block diagram of 2 to 4 decoder is shown in fig. 2
- A and B are the inputs. (No. of inputs =2)
- No. of possible input combinations: $2^2=4$
- No. of Outputs : $2^2=4$, they are indicated by D_0, D_1, D_2 and D_3
- From the Truth Table it is clear that each output is "1" for only specific combination of inputs.

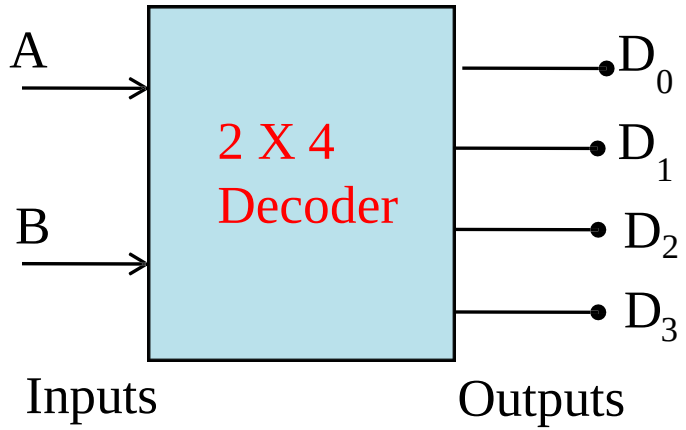


Fig. 2

TRUTH TABLE

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

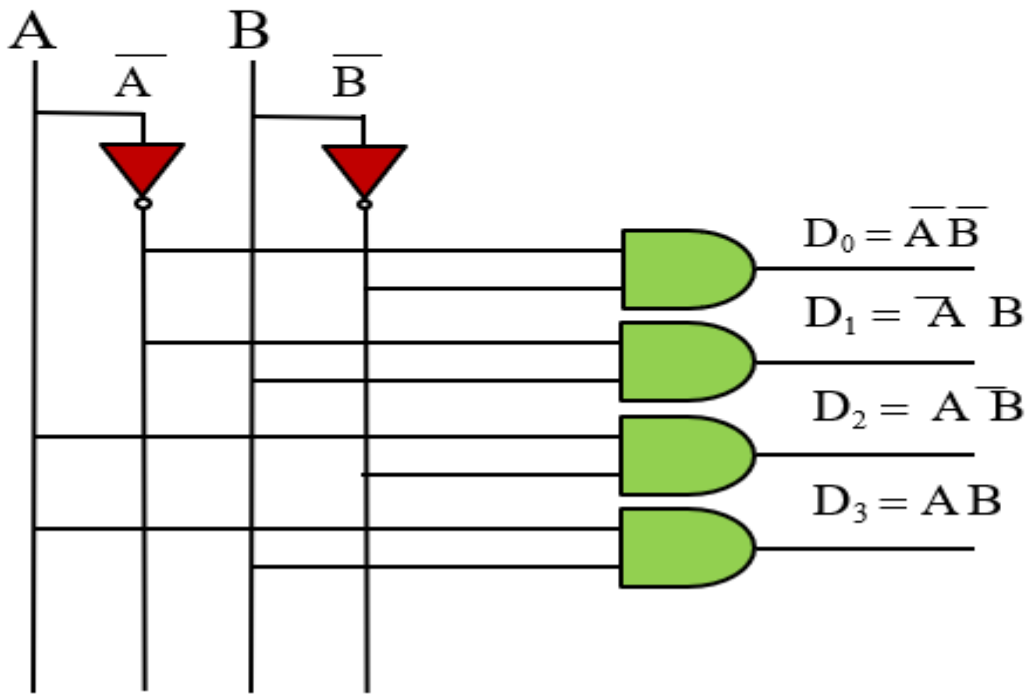
BOOLEAN EXPRESSION

From Truth Table

$$D_0 = \overline{A}\,\overline{B} \qquad D_1 = \overline{A}B$$

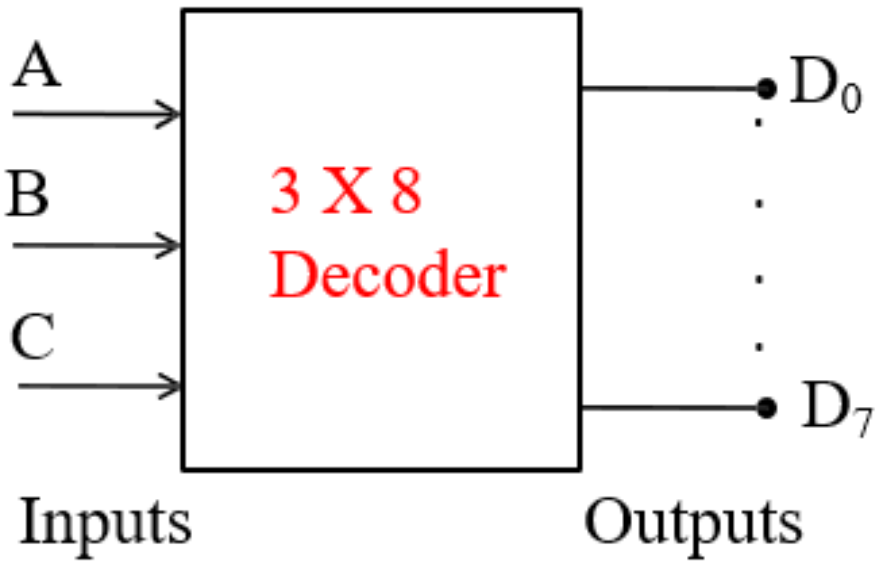
$$D_2 = A\,\overline{B} \qquad D_3 = AB$$

LOGIC DIAGRAM:



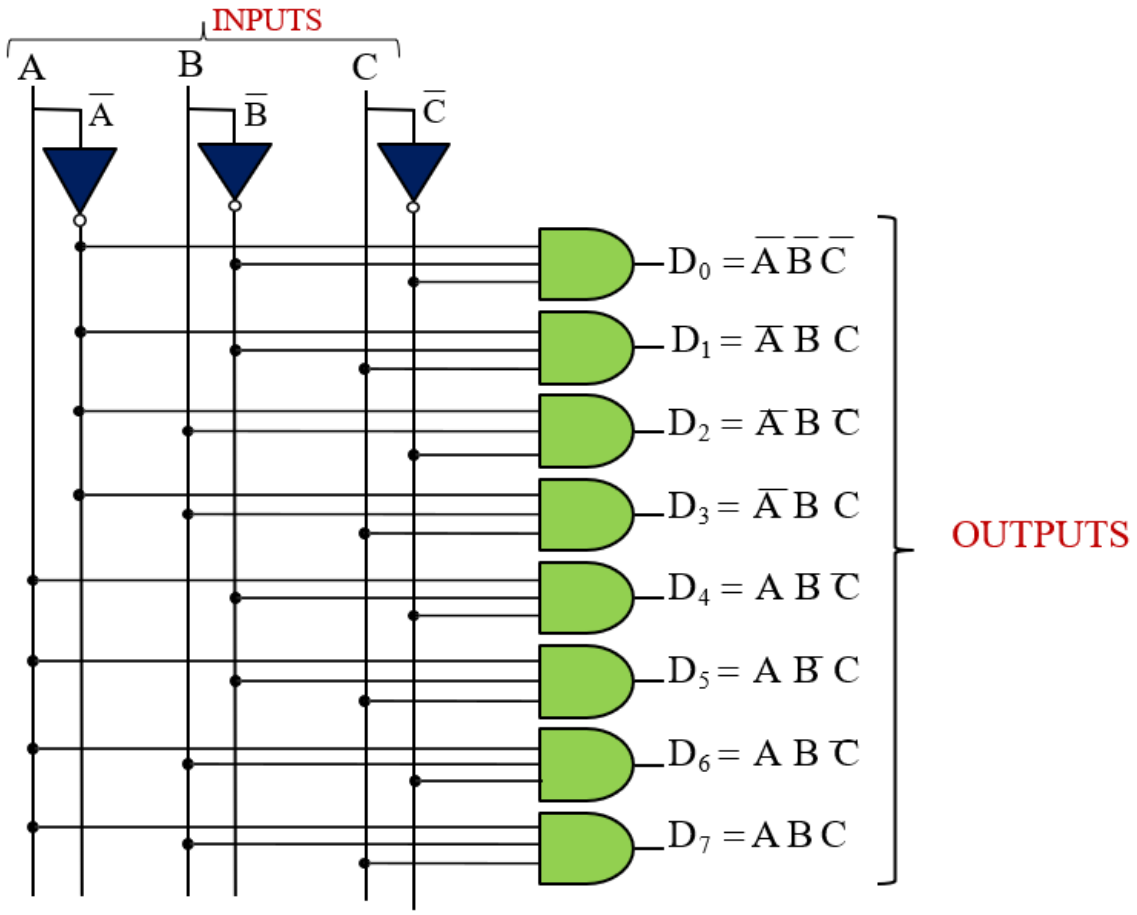
3 TO 8 LINE DECODER

- 3-to-8 line decoder has 3 inputs & 8 outputs.
- It uses all AND gates, and therefore the outputs are active-HIGH. It is also called a *binary-to-octal decoder* because it takes a 3-bit binary input code and activates one of the eight (octal) outputs corresponding to that code.
- It is also referred to as *1-of-8 decoder* because only one of the eight outputs is activated at one time.

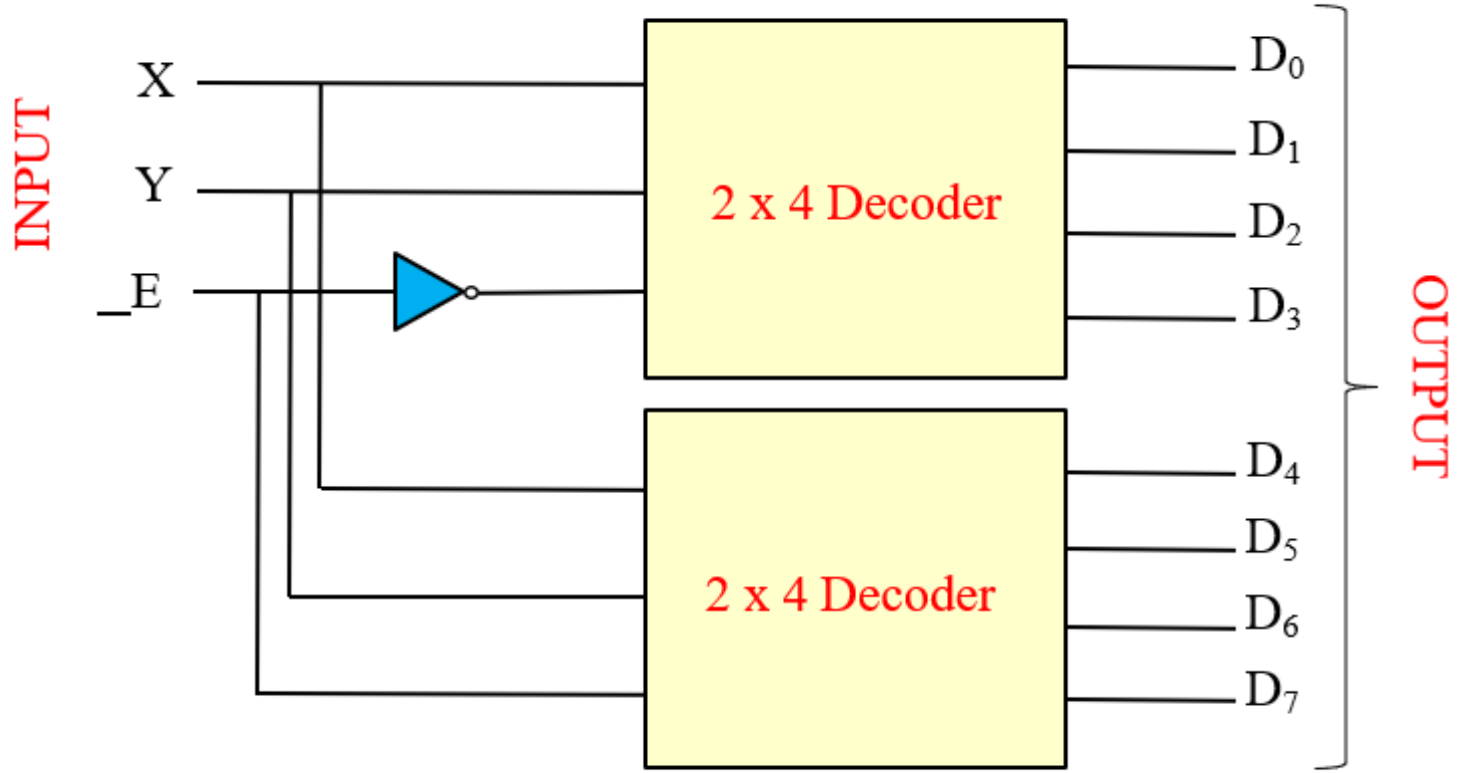


TRUTH TABLE & CIRCUIT OF 3 TO 8 DECODER

INPUTS			OUTPUTS								
A	B	C	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	1	0	0	0	0	0	0	0	$D_0 = \overline{A}\,\overline{B}\,\overline{C}$
0	0	1	0	1	0	0	0	0	0	0	$D_1 = \overline{A}\,\overline{B}\,C$
0	1	0	0	0	1	0	0	0	0	0	$D_2 = \overline{A}\,B\,\overline{C}$
0	1	1	0	0	0	1	0	0	0	0	$D_3 = \overline{A}\,B\,C$
1	0	0	0	0	0	0	1	0	0	0	$D_4 = A\,\overline{B}\,\overline{C}$
1	0	1	0	0	0	0	0	1	0	0	$D_5 = A\,\overline{B}\,C$
1	1	0	0	0	0	0	0	0	1	0	$D_6 = A\,B\,\overline{C}$
1	1	1	0	0	0	0	0	0	0	1	$D_7 = A\,B\,C$



IMPLEMENTATION OF HIGHER-ORDER DECODER (3:8 DECODER BY USING 2:4DECODER)



BOOLEAN FUNCTION USING DECODER

Example: Implement the following multiple output function using a suitable Decoder.

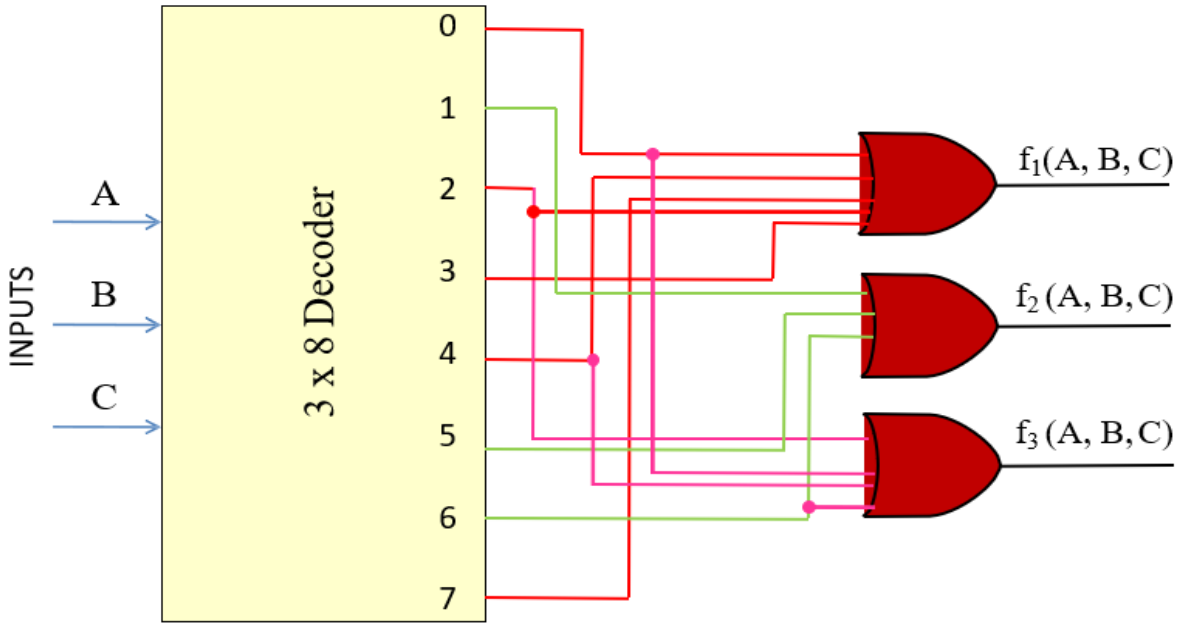
$$f_1(A, B, C) = \sum m(0,4,7) + d(2,3)$$

$$f_2(A, B, C) = \sum m(1,5,6)$$

$$f_3(A, B, C) = \sum m(0,2,4,6)$$

Solution: f1 consists of don't care conditions.

So we consider them to be logic 1.



BOOLEAN FUNCTION USING DECODER

EXAMPLE: A combinational circuit is defined by the following Boolean function. Design circuit with a Decoder and external gate.

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + x\,z$$

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,z$$

SOLUTION: STEP 1: Write the given function F_1 in SOPform

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + (y + \bar{y})\,x\,z$$

$$F_1(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + x\,y\,z + x\,\bar{y}\,z$$

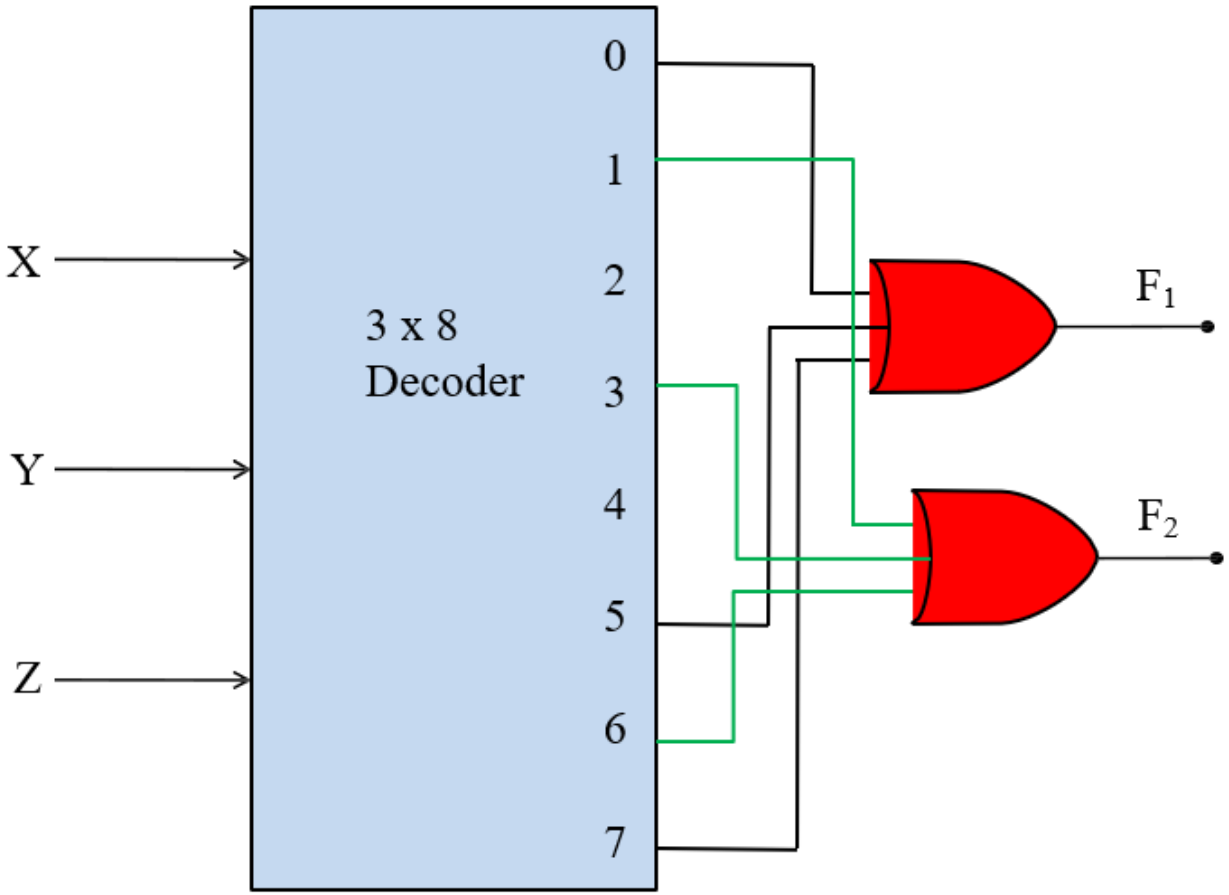
$$F_1(x, y, z) = \Sigma m\,(0,5,7)$$

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,z$$

$$F_2(x, y, z) = x\,y\,\bar{z} + (y + \bar{y})\,\bar{x}\,z$$

$$F_2(x, y, z) = x\,y\,\bar{z} + \bar{x}\,y\,z + \bar{x}\,\bar{y}\,z$$

$$F_2(x, y, z) = \Sigma m\,(1,3,6)$$



DECODER APPLICATIONS

- Decoders are used whenever an output or group of outputs is to be activated only on the occurrence of a specific combination of input levels.
- Decoders can be used as timing or sequencing signals to turn devices on or off at specific times, because when the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially.
- Decoders are widely used in memory systems of computers where they respond to the address code from the central processor to activate the memory storage location specified by the address code.
- Decoder is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times.