Sequential Circuit Latch & Introduction of SR Flip-flop

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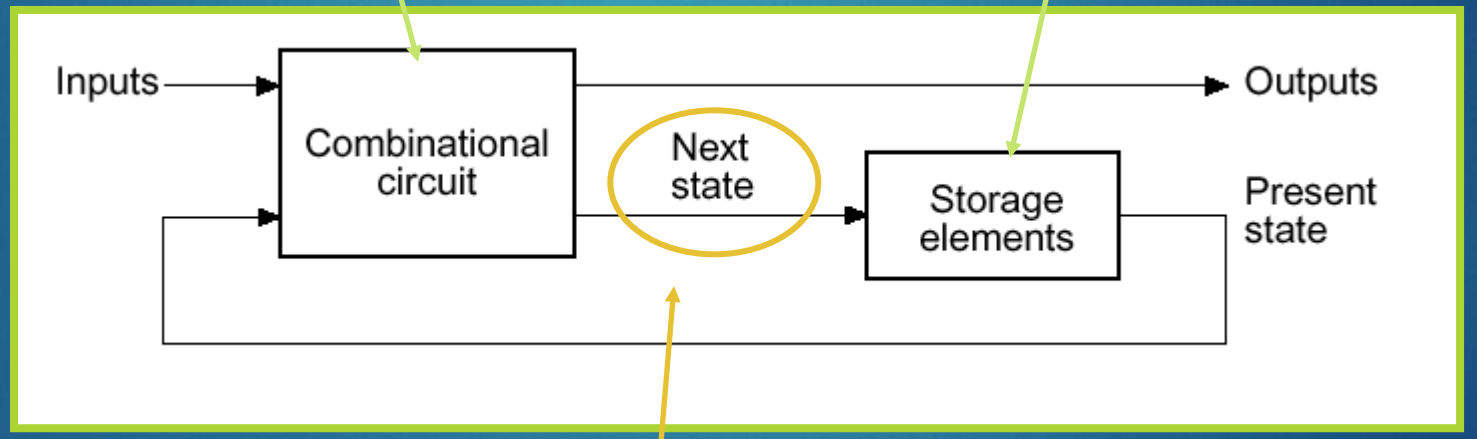
Digital Circuits

- Combinational Circuits
  - The outputs depend only on the current input values
  - It uses only logic gates
- Sequential Circuits
  - The outputs depend on the current and past input values.
  - It uses logic gates and storage elements.
  - Sequential Logic circuits remember past inputs and past circuit state.
  - Outputs from the system are “fed back” as new inputs with gate delay and wire delay.
  - The storage elements are circuits that are capable of storing binary information: memory.

Sequential Circuits

Circuits that we have learned so far

Information Storing Circuits



Timed "States"

Synchronous vs. Asynchronous

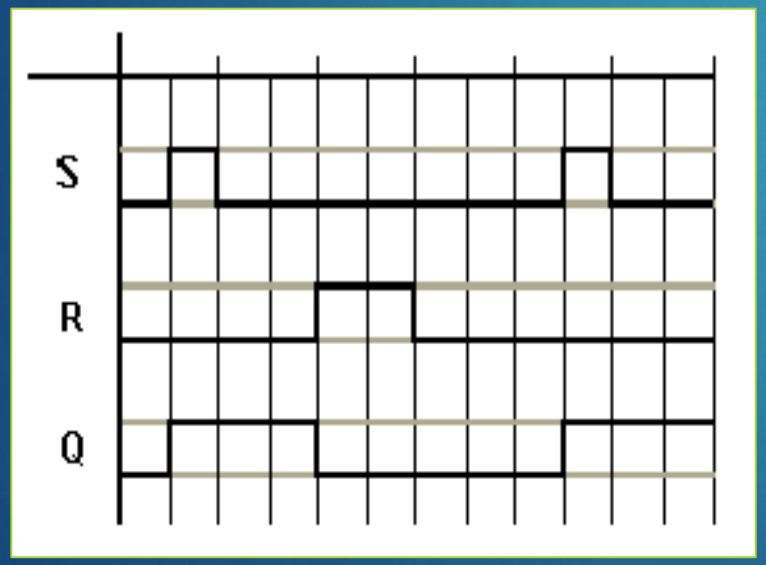
There are two types of sequential circuits:

- **Synchronous** sequential circuit: circuit output changes only at some discrete instants of time. This type of circuits achieves synchronization by using a timing signal called the *clock*.
  - Example: Flip-Flop are useful for synchronous sequential circuits.
- **Asynchronous** sequential circuit: circuit output can change at **any** time (clockless).
  - Example: Latches are useful for asynchronous sequential circuits.

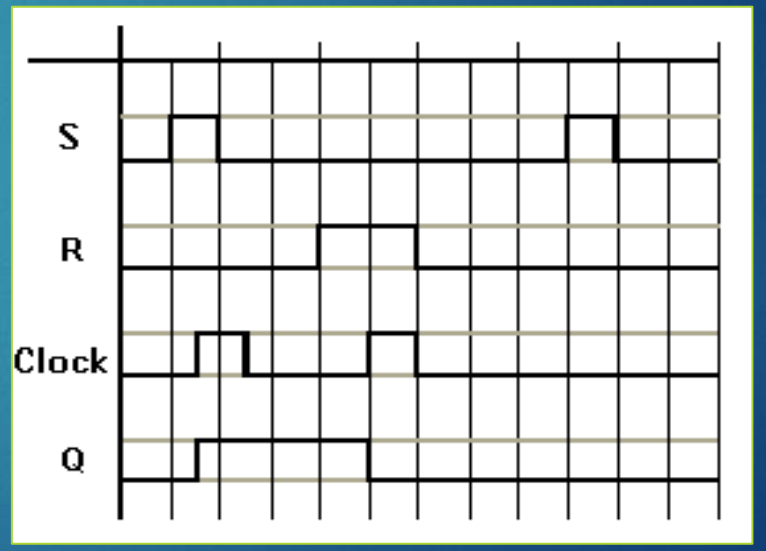
Memory Devices

Latches A *latch* is a memory element whose excitation signals control the state of the device. A latch has two stages *set* and *reset*. *Set* stage sets the output to 1. *Reset* stage set the output to 0.

Flip-flops A *flip-flop* is a memory device that has clock signals control the state of the device.



Latch



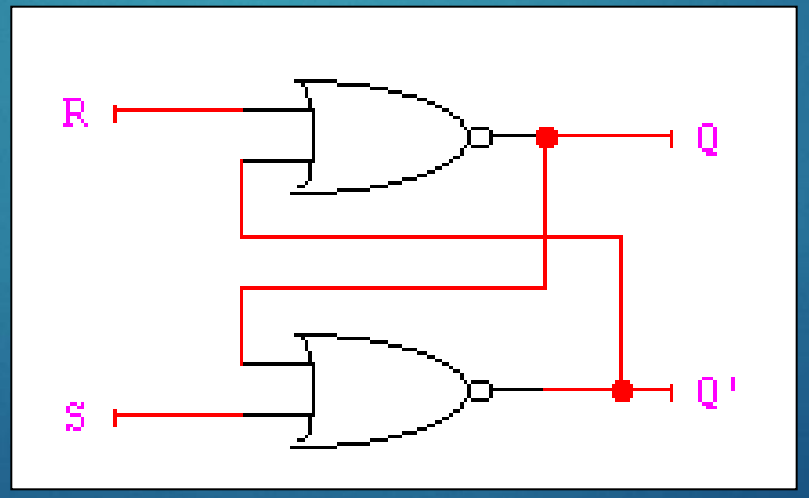
Flip-flop

SR Latch

SR Latch

The SR latch is the basic memory element consists of two cross-coupled NOR gates. It has two input signals, ***S*** set signal and ***R*** reset signal. It also has two outputs Q and Q'; and two states, a set state when Q = 1 and a reset state when Q = 0 (Q' = 1)

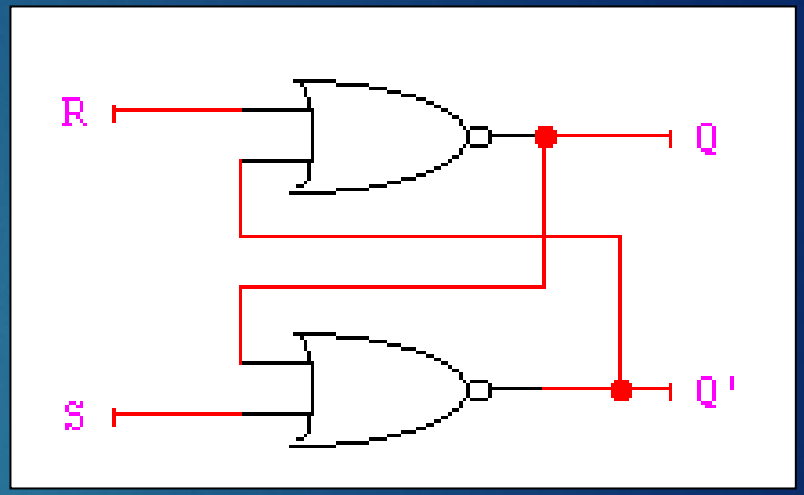
S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0



S	R	Q
0	0	no change
0	1	0 reset
1	0	1 set
1	1	unstable

The SR Latch (NOR version)

- The SR (Set-Reset) Latch

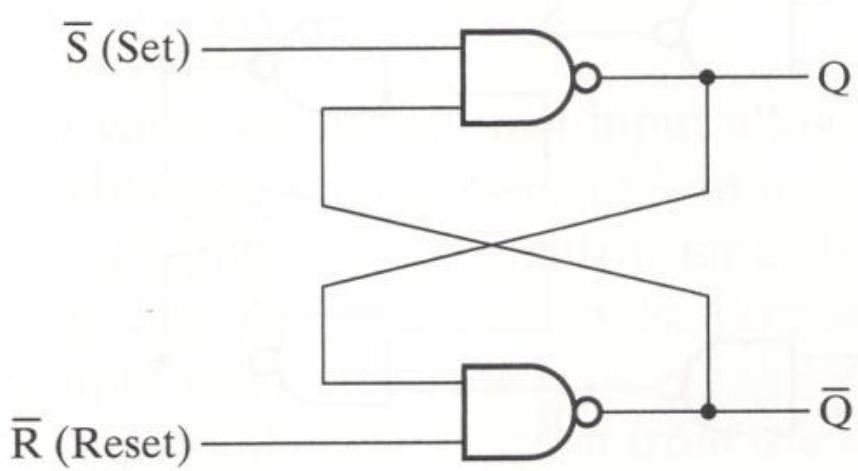


- And its operation

S	R	Q	Q′	
1	0	1	0	Set Q
0	0	1	0	Hold
0	1	0	1	Clear
0	0	0	1	Hold
1	1	0	0	Undefined

S	R	Q
0	0	hold
0	1	0 reset
1	0	1 set
1	1	unstable

The SR Latch (NAND version)

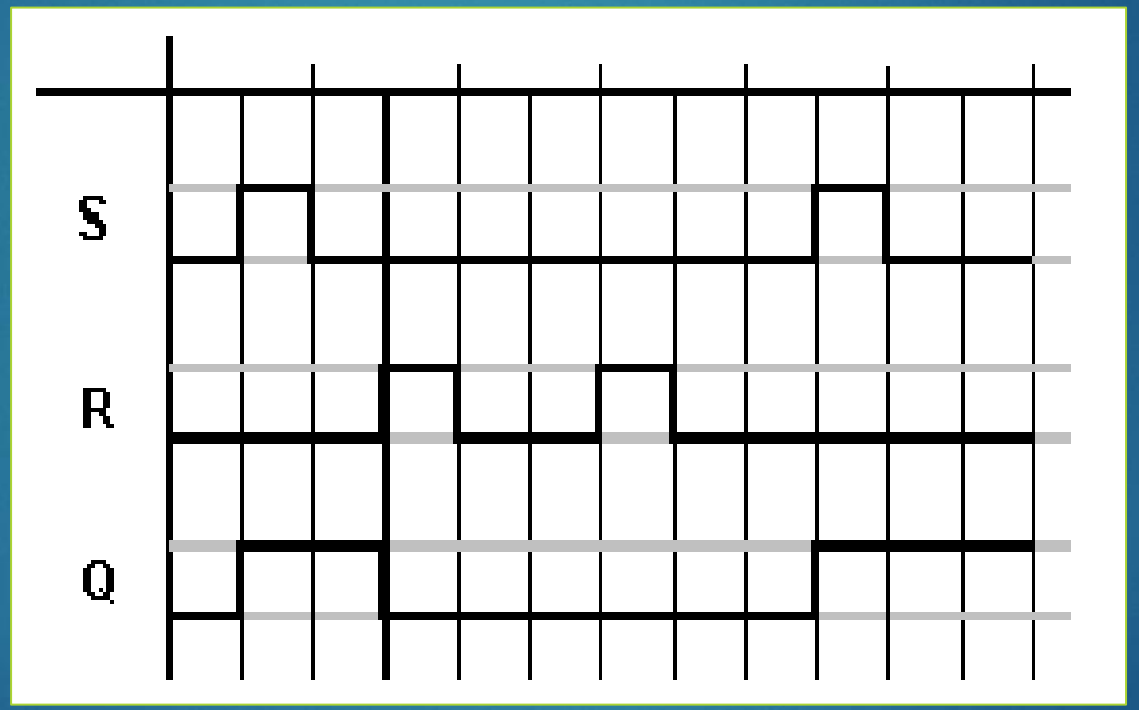


(a) Logic diagram

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	Undefined

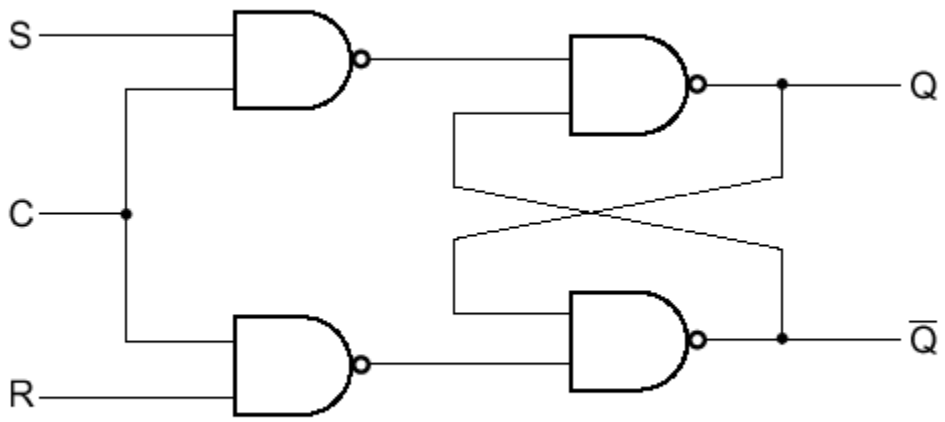
(b) Function table

Timing Diagram of SR-Latch



SR Flip-Flop

- Flip-flop is a memory element which change its condition based on clock signal
- The flip-flops are constructed from latches.
- They are useful for synchronous sequential circuits.

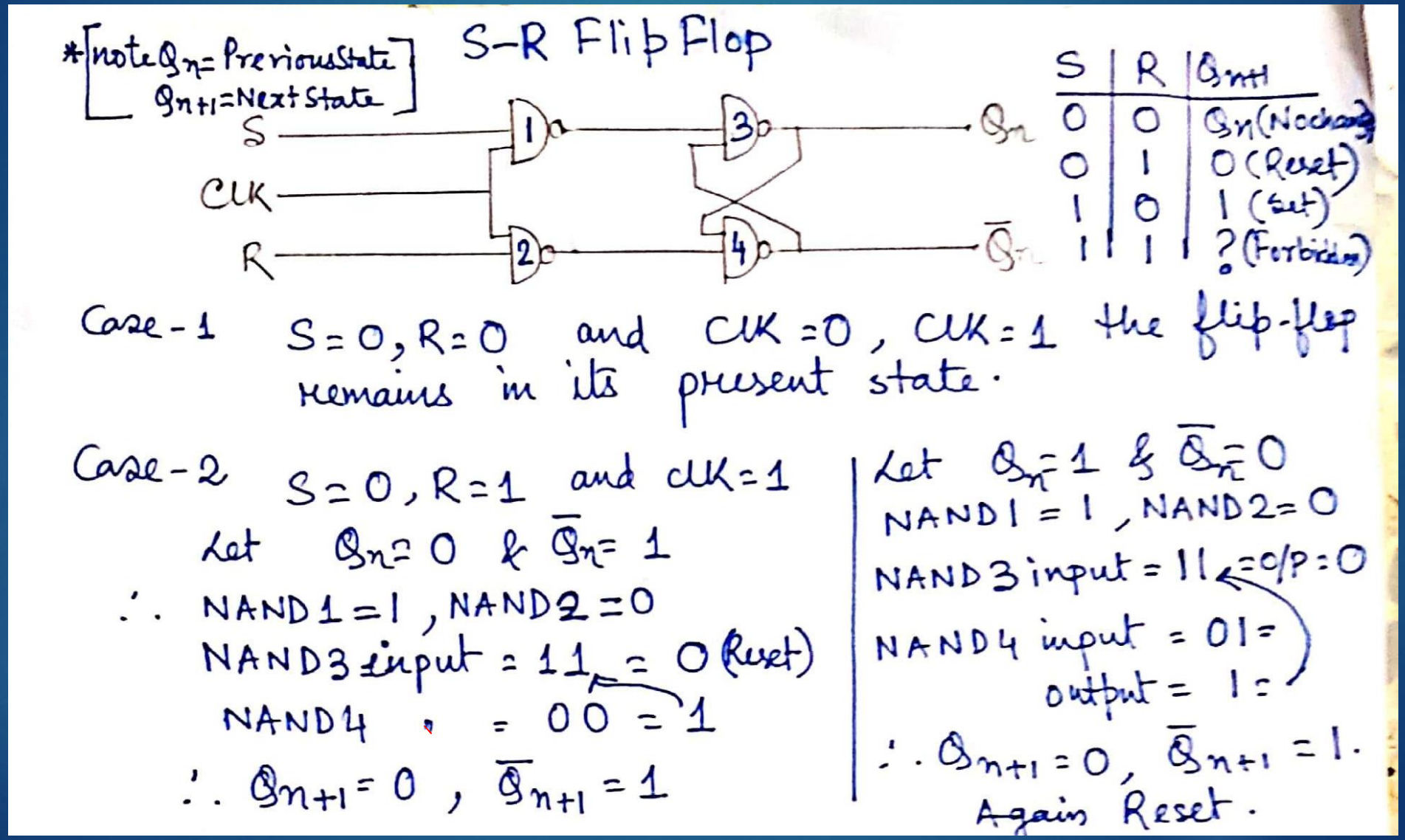


(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

SR Flip-Flop


*[note Qn = Previous State
Qn+1 = Next State]
S-R Flip Flop
S
CLK
R
1
2
3
4
Qn
$\overline{Q}_n$
S | R | Qn+1
0 | 0 | Qn (No change)
0 | 1 | 0 (Reset)
1 | 0 | 1 (Set)
1 | 1 | ? (Forbidden)
Case-1 S=0, R=0 and CLK=0, CLK=1 the flip-flop remains in its present state.
Case-2 S=0, R=1 and CLK=1
Let Qn=0 & $\overline{Q}_n$=1
∴ NAND1=1, NAND2=0
NAND3 input = 11 = 0 (Reset)
NAND4 = 00 = 1
∴ Qn+1 = 0, $\overline{Q}_{n+1}$ = 1
Let Qn=1 & $\overline{Q}_n$=0
NAND1 = 1, NAND2=0
NAND3 input = 11 = o/p = 0
NAND4 input = 01 = output = 1
∴ Qn+1 = 0, $\overline{Q}_{n+1}$ = 1.
Again Reset.

Case-3 $S=1, R=0$ & $CLK=1$

Let $Q_n=0$, $\bar{Q}_n=1$

∴ NAND1 = 0, NAND2 = 1

NAND3 input = 01 ← output = 1

NAND4 input = 10, output = 1

∴ $Q_{n+1}=1$, $\bar{Q}_{n+1}=0$

Set state

Let $Q_n=1$, $\bar{Q}_n=0$.

∴ NAND1 = 0, NAND2 = 1

NAND3 input = 00

NAND3 output = 1 = Set State

NAND4 input = 11 = 0

NAND4 output = 11 = 0

$Q_{n+1}=1$, $\bar{Q}_{n+1}=0$.

Case-4 $S=1, R=1$ & $CLK=1$

Let $Q_n=0$, $\bar{Q}_n=1$

∴ NAND1 = 0, NAND2 = 0

NAND3 input = 01, output = 1

NAND4 input = 00 = 1, output = 1

both Q_{n+1} & $\bar{Q}_{n+1}$ in same state which is not possible.

$S=1, R=1$

Let $Q_n=1$, $\bar{Q}_n=0$

∴ NAND1 = 0, NAND2 = 0

NAND3 input = 01

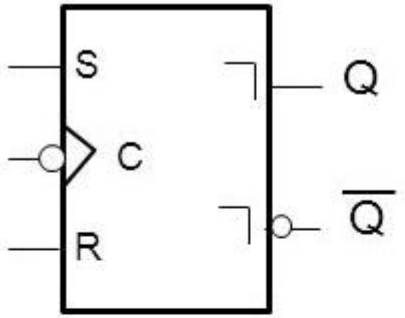
NAND3 output = 1

NAND4 input = 01 = 1

NAND4 output = 01 = 1

Again Q_{n+1} & $\bar{Q}_{n+1}$ are same.

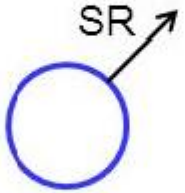
State Transition Diagram of SR Flip Flop

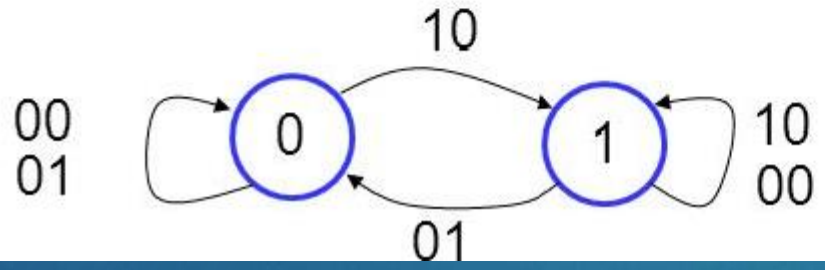


Function table

S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	-

State Diagram:



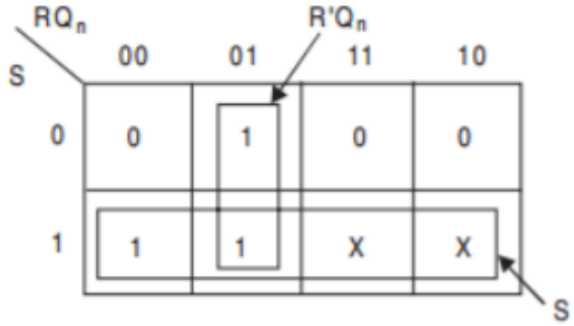


SR Flip-Flop

- Characteristic Table of an S-R Flip Flop.

Flip-flop inputs		*Present output*	*Next output*
S	*R*	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Now we will find out the characteristic equation of the S-R flip-flop from the characteristic table with the help of the Karnaugh map:-



From the Karnaugh map above we find the expression for Q_{n+1} as

$$Q_{n+1} = S + R'Q_n$$