Registers

Presented by Nabanita Das

Registers

Flip-flop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a Register. The n-bit register will consist of n number of flip-flop and it is capable of storing an n-bit word.

The binary data in a register can be moved within the register from one flip-flop to another. The registers that allow such data transfers are called as shift registers. There are four mode of operations of a shift register.

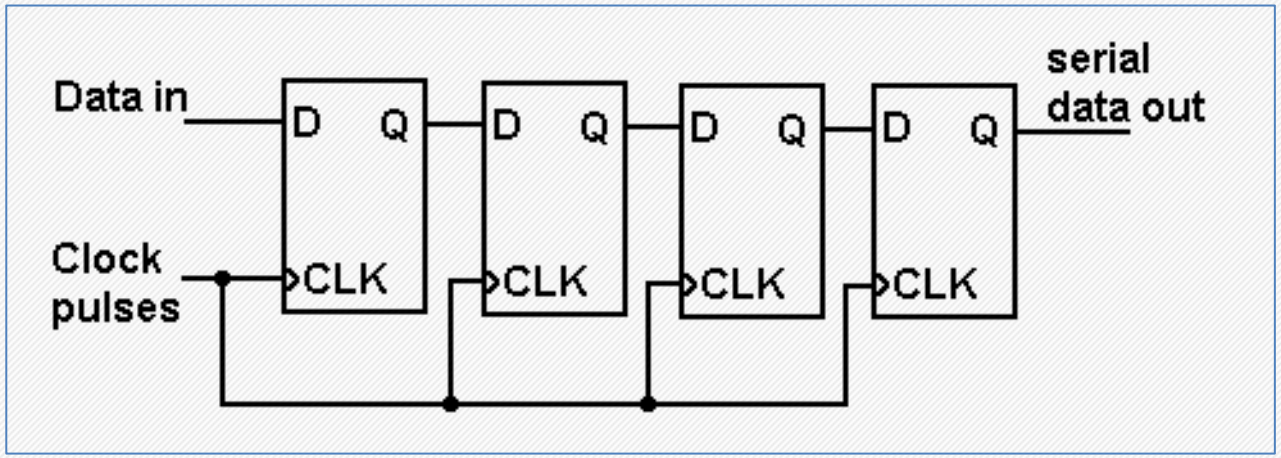
- Serial Input Serial Output
- Serial Input Parallel Output
- Parallel Input Serial Output
- Parallel Input Parallel Output

Registers are useful for storing and manipulating information

- Internal registers in microprocessors to manipulate data

Serial Input Serial Output (SISO)

- Let all the flip-flop be initially in the reset condition i.e. Q3 = Q2 = Q1 = Q0 = 0. If an entry of a four bit binary number 1 1 1 1 is made into the register, this number should be applied to Din bit with the LSB bit applied first. The D input of FF-3 i.e. D3 is connected to serial data input Din. Output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2 and so on.



Truth Table of SISO

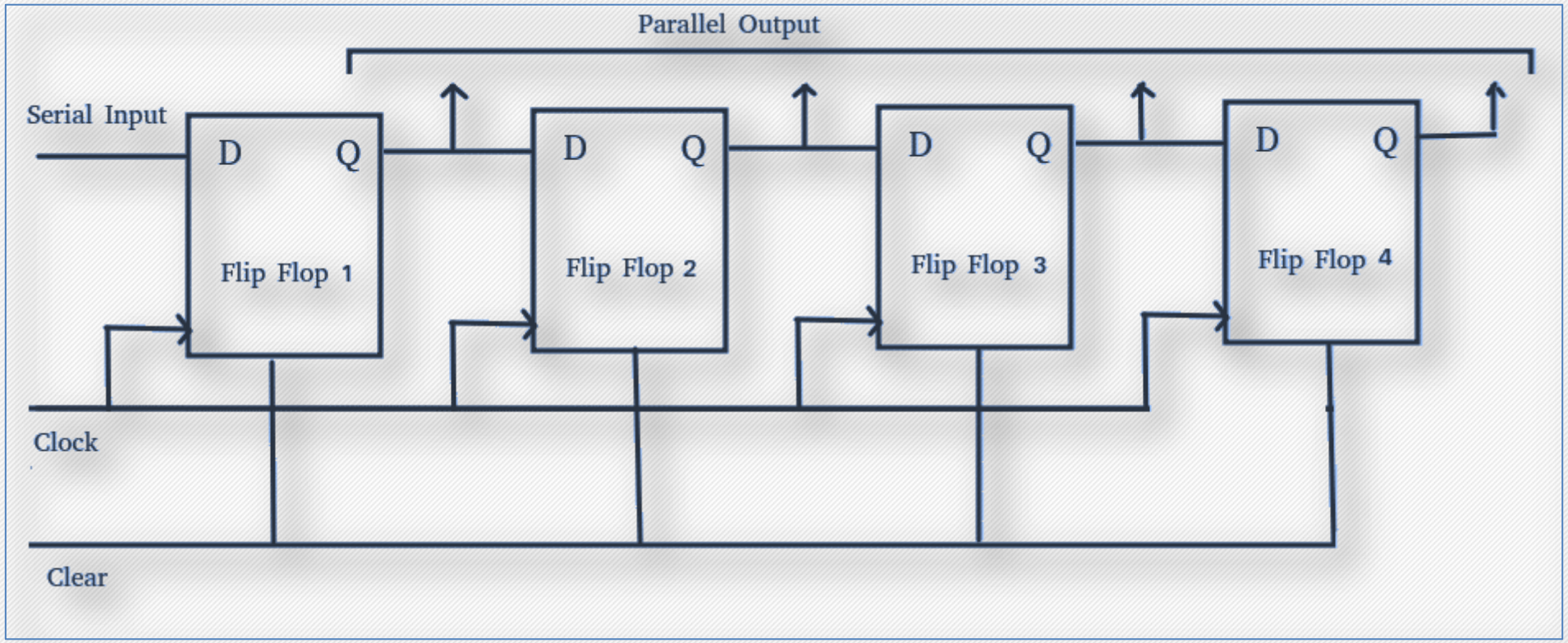
	Clk	$D_n=Q_3$	$Q_3=D_2$	$Q_2=D_1$	$Q_1=D_0$	Q_0
Initially			0	0	0	0
(1)	↓	1	1	0	0	0
(2)	↓	1	1	1	0	0
(3)	↓	1	1	1	1	0
(4)	↓	1	1	1	1	1

→ Direction of data travel

Serial Input Parallel Output (SIPO)

- In such types of operations, the data is entered serially and taken out in parallel fashion.
- Data is loaded bit by bit. The outputs are disabled as long as the data is loading.
- As soon as the data loading gets completed, all the flip-flops contain their required data, the outputs are enabled so that all the loaded data is made available over all the output lines at the same time.
- 4 clock cycles are required to load a four bit word. Hence the speed of operation of SIPO mode is same as that of SISO mode.

Serial Input Parallel Output (SIPO)



Parallel Input Serial Output (PISO)

- Data bits are entered in parallel fashion.
- The circuit shown below is a four bit parallel input serial output register.
- Output of previous Flip Flop is connected to the input of the next one via a combinational circuit.
- The binary input word B0, B1, B2, B3 is applied though the same combinational circuit.
- There are two modes in which this circuit can work namely - shift mode or load mode.

Parallel Input Serial Output (PISO) contd.

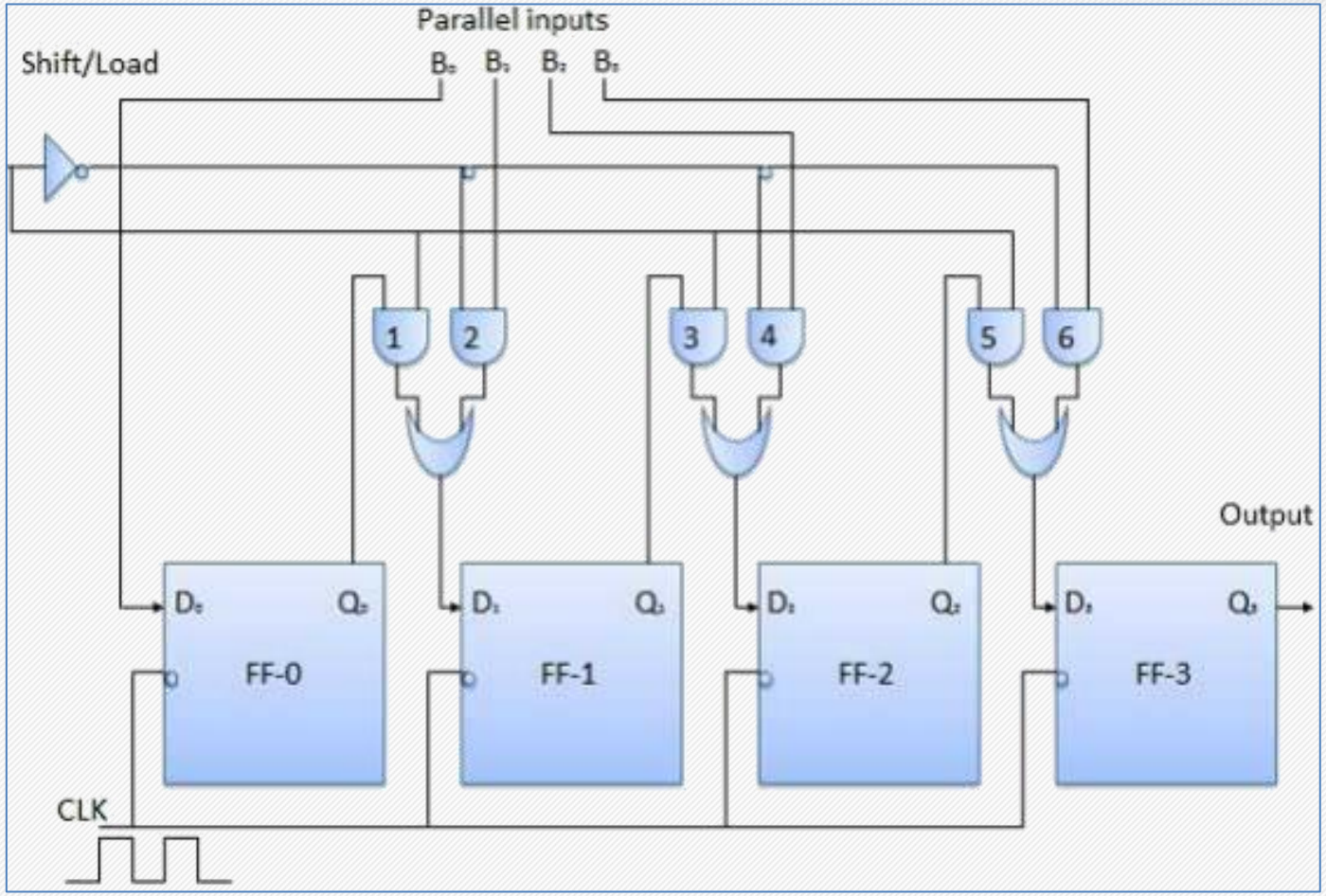
- Load mode

When the shift/load bar line is low 0, the AND gate 2, 4 and 6 become active they will pass B1, B2, B3 bits to the corresponding flip-flops. On the low going edge of clock, the binary input B0, B1, B2, B3 will get loaded into the corresponding flip-flops. Thus parallel loading takes place.

- Shift mode

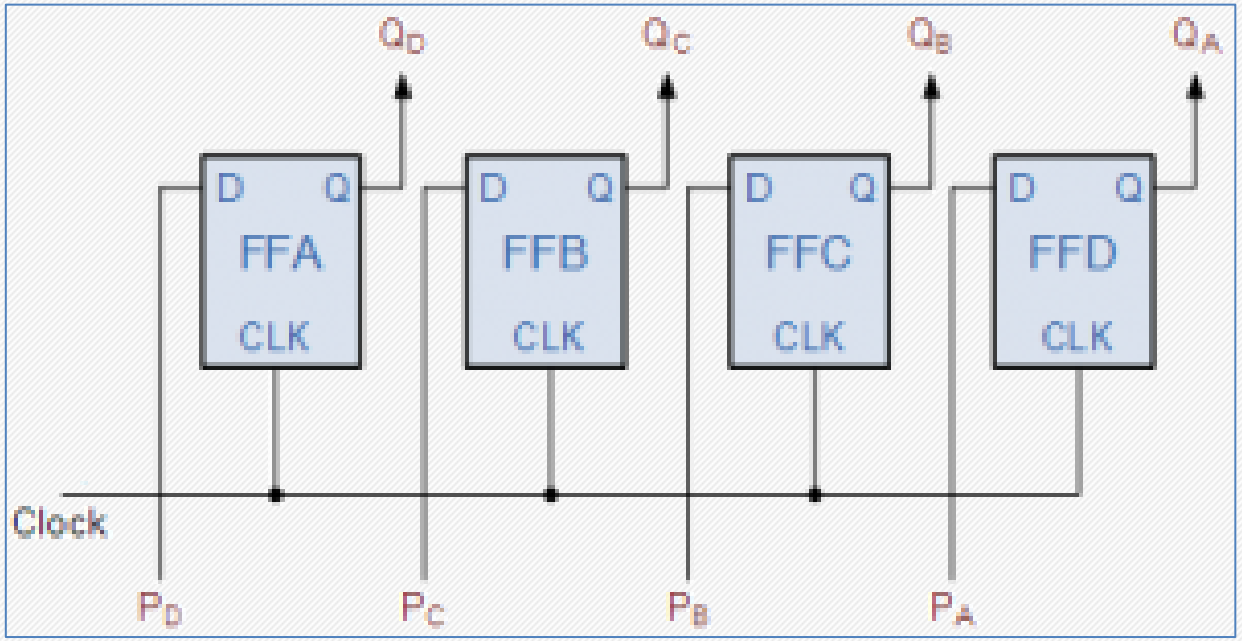
When the shift/load bar line is low 1, the AND gate 2, 4 and 6 become inactive. Hence the parallel loading of the data becomes impossible. But the AND gate 1,3 and 5 become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses. Thus the parallel in serial out operation takes place.

Block Diagram of Parallel Input Serial Output (PISO)



Parallel Input Parallel Output (PIPO)

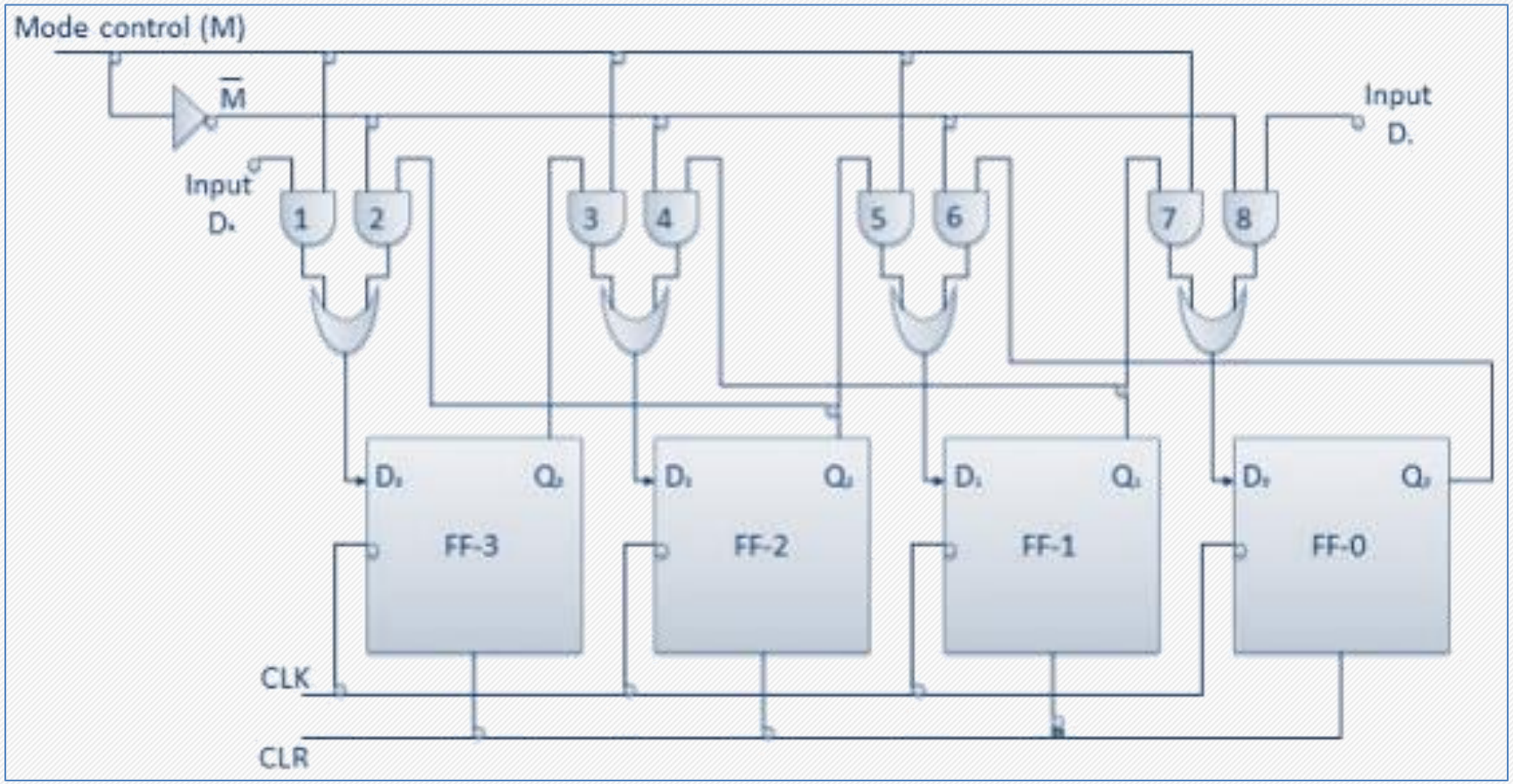
- In this mode, the 4 bit binary input P_A, P_B, P_C, P_D is applied to the four flip-flops respectively. As soon as the clock is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side. Only clock pulse is essential to load all the bits.



Bidirectional Shift Register

- If a binary number is shifted left by one position then it is equivalent to multiplying the original number by 2. Similarly if a binary number is shifted right by one position then it is equivalent to dividing the original number by 2. Hence if we want to use the shift register to multiply and divide the given binary number, then we should be able to move the data in either left or right direction. Such a register is called bi-directional register. A four bit bi-directional shift register is shown in fig. There are two serial inputs namely the serial right shift data input DR, and the serial left shift data input DL along with a mode select input M.

Block Diagram of Bidirectional Shift Register



Operations of Bidirectional Shift Register

Operation

S.N.	Condition	Operation
1	**With M = 1 − Shift right operation**	If M = 1, then the AND gates 1, 3, 5 and 7 are enabled whereas the remaining AND gates 2, 4, 6 and 8 will be disabled. The data at DR is shifted to right bit by bit from FF-3 to FF-0 on the application of clock pulses. Thus with M = 1 we get the serial right shift operation.
2	**With M = 0 − Shift left operation**	When the mode control M is connected to 0 then the AND gates 2, 4, 6 and 8 are enabled while 1, 3, 5 and 7 are disabled. The data at DL is shifted left bit by bit from FF-0 to FF-3 on the application of clock pulses. Thus with M = 0 we get the serial right shift operation.

Universal Shift Register

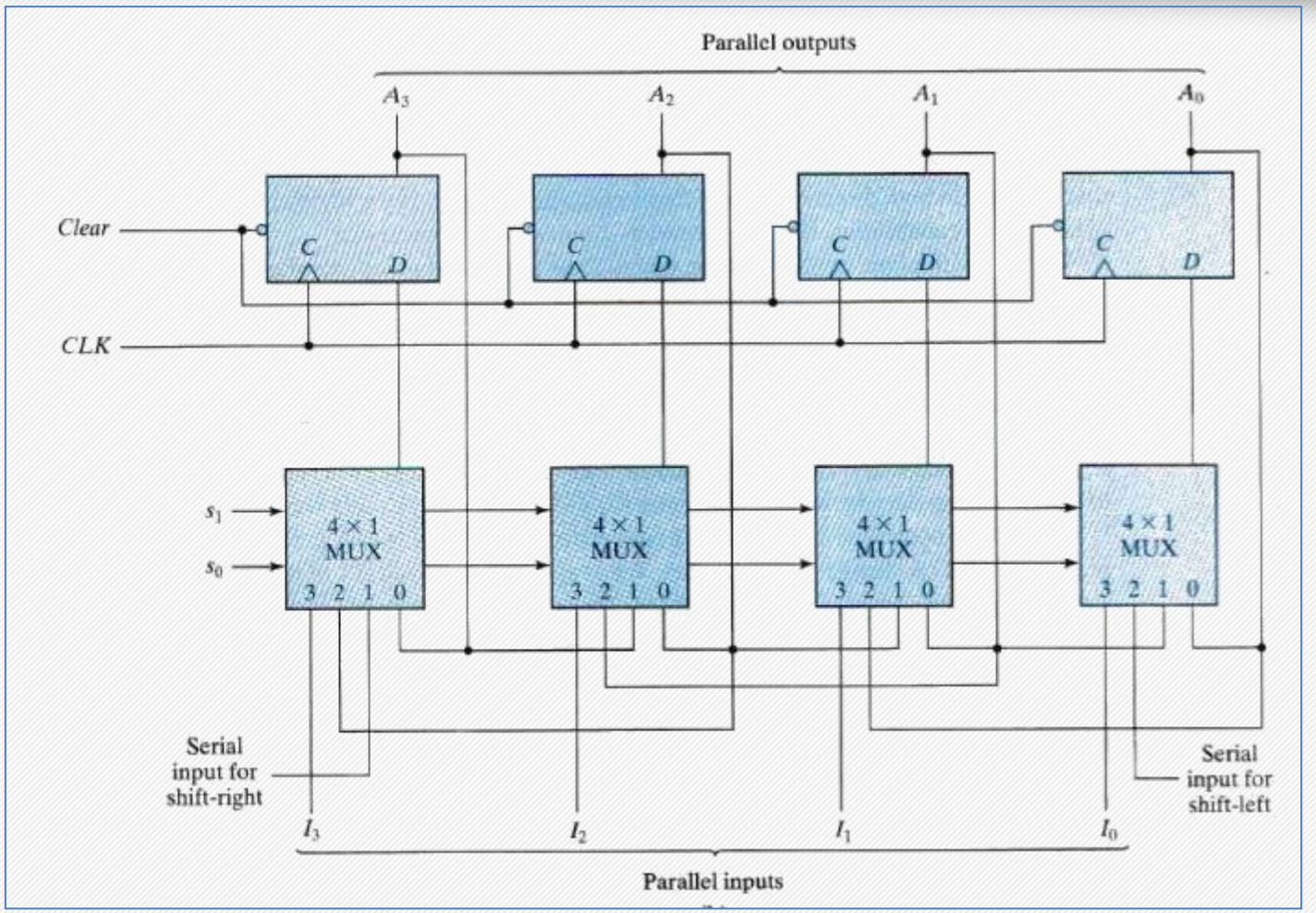
- A shift register which can shift the data in only one direction is called a uni-directional shift register.
- A shift register which can shift the data in both directions is called a bi-directional shift register.
- Applying the same logic, a shift register which can shift the data in both directions as well as load it parallelly, is known as a universal shift register.
- The shift register is capable of performing the following operation
  - ✓ Parallel loading
  - ✓ Lift shifting
  - ✓ Right shifting

1. The first input is connected to the output pin of the corresponding flip-flop.
2. The second input is connected to the output of the very-previous flip flop which facilitates the right shift.
3. The third input is connected to the output of the very-next flip-flop which facilitates the left shift.
4. The fourth input is connected to the individual bits of the input data which facilitates parallel loading.

Operations of Universal Shift Register

- The s1 and s0 inputs control the mode of operation of the register as specified in the function entries.
- When s1s0 =00 the present values of the register is applied to the D inputs of the flip-flops. This condition forms a path from the output of each flip-flop into the input of the same flip-flop.
- The next clock pulse transfers into each flip-flop the binary value it held previously, and no change of state occurs.
- When s1s0 =01, terminals 1 of the multiplexer inputs have the path to the D inputs of the flip-flops. This causes the shift-right operation, with the serial input transfer into the flip-flop A4.
- When s1s0 =10, a shift-left operations results, with the other serial input going into flip-flop A1.
- Finally, when s1s0 =11, the binary information on the parallel input lines are transferred into the register simultaneously during the next clock pulse.

Universal Shift Register contd.



S1	S0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load