Master Slave JK Flip Flop

by

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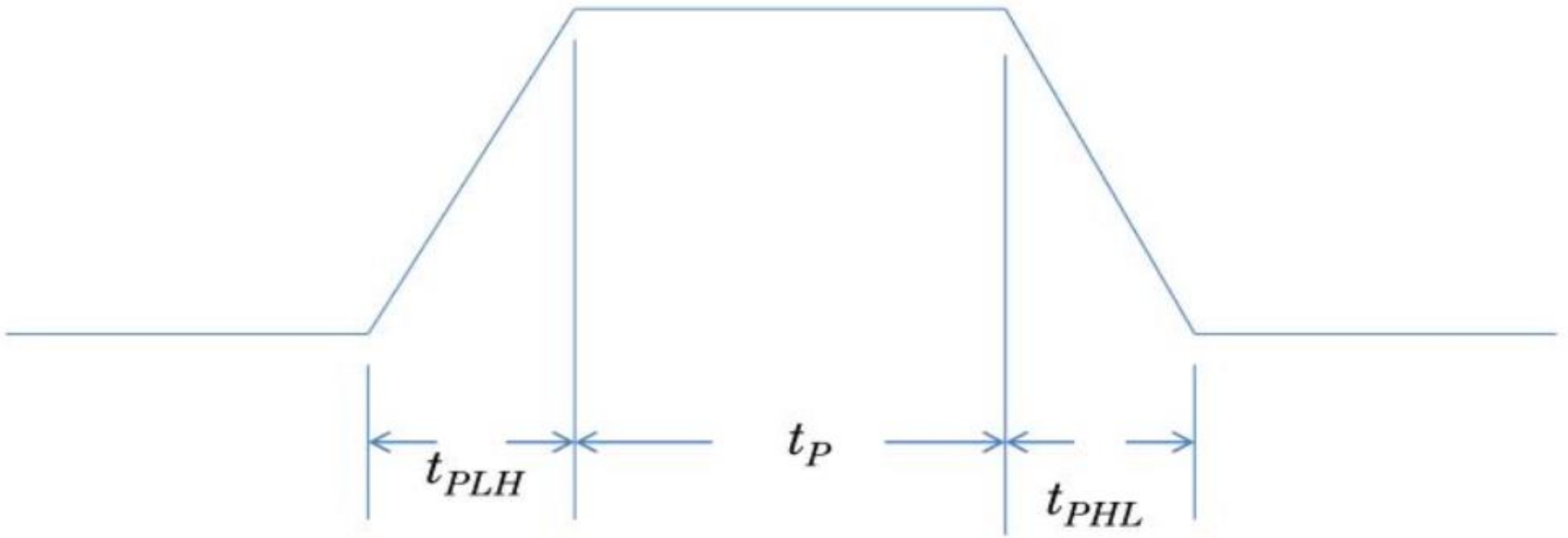
Race Around Condition

- The race-around condition (Problem) occurs when both the inputs of JK-Flip-flop are 1.
- If the width of the clock pulse t_p is too long, the state of the flip-flop will keep on changing from 0 to 1, 1 to 0 , 0 to 1 and so on, and at the end of the clock pulse, its state will be uncertain.
- This phenomenon is called the *rece around condition*.

- The race-around condition can be avoided if clock pulse is reduced than the propagation delay of flip-flop , i.e., $t<T_P<T$, but this is not practically feasible. A more practical method for this is the use of master-slave flip-flop.

Clock Pulse



Now $t_{PLH} = t_{PHL} = {}_{\Delta}t$ *(Propagation delay time)*

Race Around Condition

- The *race around condition* occurs if $t_p >> \Delta t$.

How we can avoid race-around condition?

We can avoid race around condition by the following way.

1. If $t_p < \Delta t$.
2. By using edge triggering flip-flop.
3. By using Master-Slave JK Flip-flop.

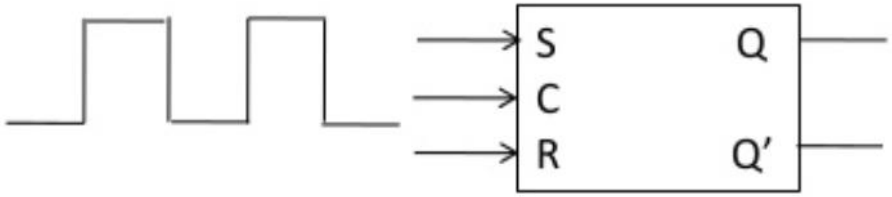
Triggering Methods

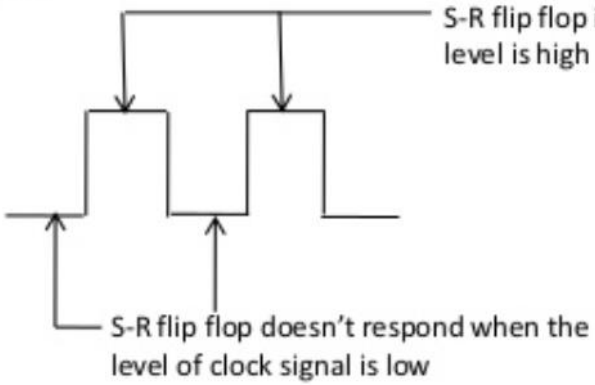
Depending on which portion of clock signal the latch or flip flop responds to, classify them into two types:-

1. Level Triggering.

2. Edge Triggering.

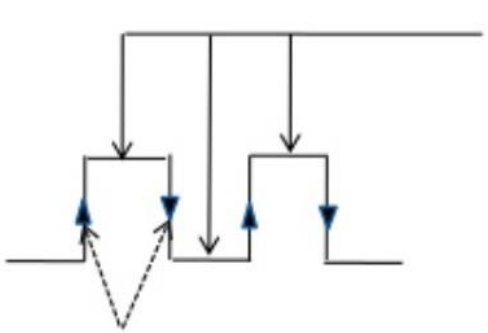
LEVEL TRIGGERING:-Circuit respond to change in their input, if their enable input(E) held at an active level which may be steady high or low level .





Types of Level Triggering Flip Flops

1. Positive Level Triggering :-Output of a flip flop respond to the input changes, only when its clock inputs are high (1) level.
2. Negative Level Triggering :-Output of a flip flop respond to the input changes, only when its clock inputs are low (0) level.



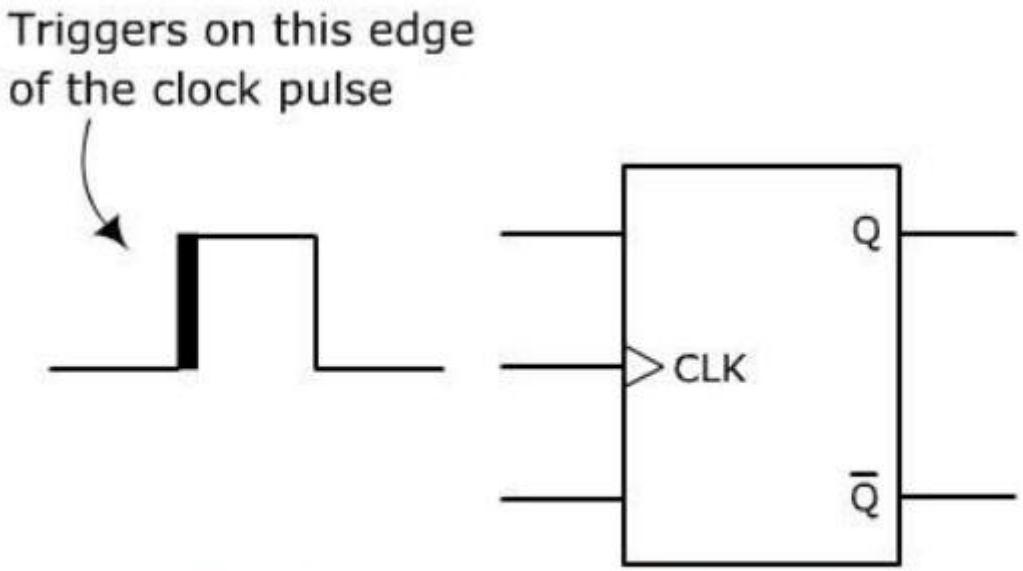
The level triggered flip flop output changes when clock input is either at high or low level

The edge triggered flip flop samples the input at the positive or negative edge and changes its outputs accordingly

Edge Triggering Flip flop

- **Positive Edge Triggering**

When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used. It is mainly identified from the clock input lead along with a triangle. Take a look at the symbolic representation shown below.

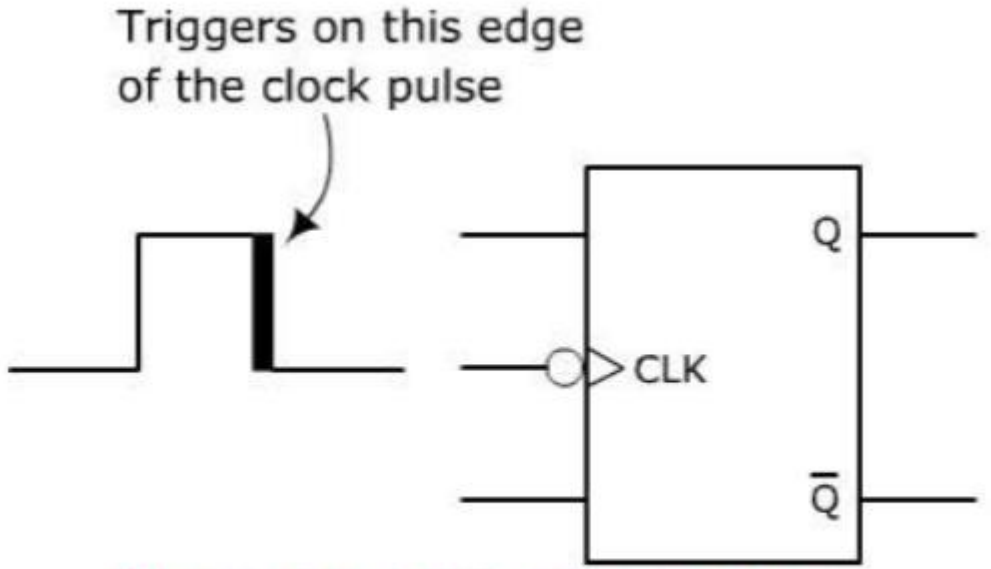


Positive Edge Triggering

Edge Triggering Flip flop

- **Negative Edge Triggering**

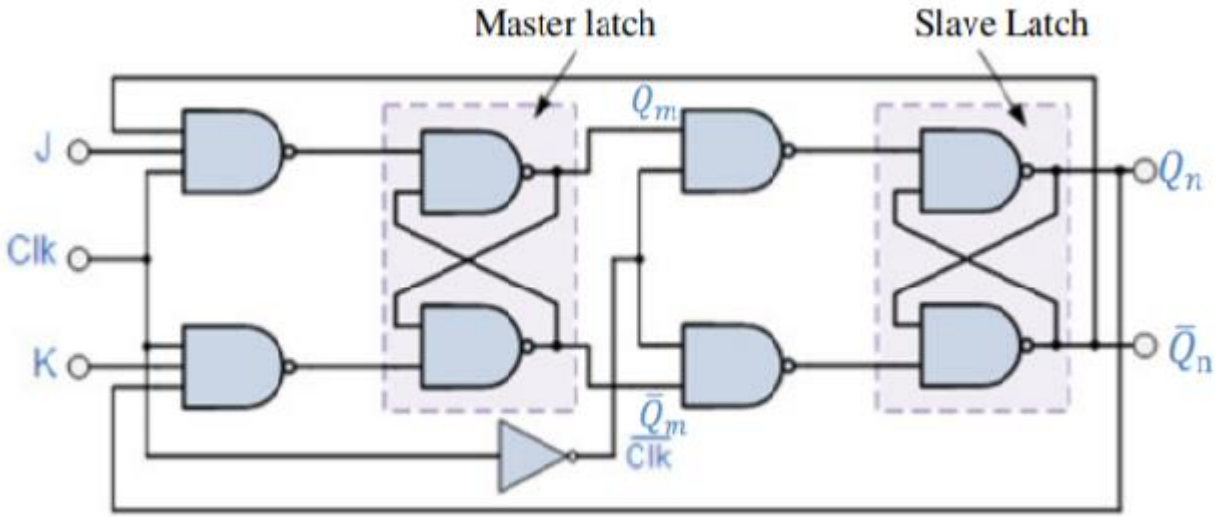
When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used.. It is mainly identified from the clock input lead along with a low-state indicator and a triangle. Take a look at the symbolic representation shown below.



Negative Edge Triggering

Master Slave JK Flip Flop

- The master-slave JK flip flop consists of two JK flip flops. The first flip flop, or master is driven by +ve edge of the clock pulse, then it disables the second, or slave. The second flip flop is driven by –ve edge of the clock pulse.
- When the clock input has the +ve edge master acts according to its JK inputs but slave does not response.
- When the clock input has the –ve edge the slave flip flop copies the master outputs but master does not respond to the feedback from **Qn** or **Qn'.**
- Thus the master slave flipflop does not have any race-around condition.



Master Slave JK Flip Flop contd.

1. J=0, K=0, input does not produce any change.
2. J=1, K=0, the master flip flop sets on the +ve clock edge. The high Q(1) output of the master drives to the input (J) of the slave. The slave flip flop copies the action of the master flip flop.
3. J=0, K=1, the master resets the loading edge of the clock pulse. Once again the slave flip flop copies the action of the master flip flop.
4. J=K=1, the master flip flop toggles on the positive edge & the slave toggles on the negative clock edge.