Design a MOD-6 synchronous counter using J-K Flip-Flops.

Design of Mod-6 Counter: To design the Mod-6 synchronous counter, contain six counter states (that is, from 0 to 5). For this counter, the counter design table lists the three flip-flop and their states as 0 to 5 and the 6 inputs for the 3 flip-flops.

Input pulse count	**Counter States**			**Flip-Flop Inputs**					
	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	X	0	X	0	X
1	1	0	0	X	1	1	X	0	X
2	0	1	0	1	X	X	0	0	X
3	1	1	0	X	1	X	1	1	X
4	0	0	1	1	X	0	X	X	0
5	1	0	1	X	1	0	X	X	1
6(0)	0	0	0						

Counters Design Table for Mod-6 Counter

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	X	1
A	X	X	X	X

Map for J_A
$J_A = 1$
Fig.(i)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	X
A	1	1	X	1

Map for K_A
$K_A = 1$
Fig.(ii)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	X	X
A	1	0	X	X

Map for J_B
$J_B = A\bar{C}$
Fig.(iii)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	0
A	X	X	X	1

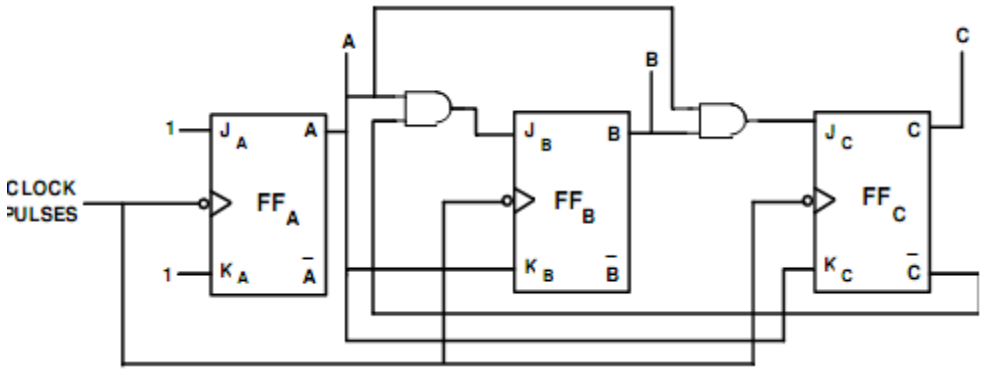
Map for K_B
$K_B = A$
Fig.(iv)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	X	X	0
A	0	X	X	1

Map for J_C
$J_C = AB$
Fig.(v)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	0	X	X
A	X	1	X	X

Map for K_C
$K_C = A$
Fig.(vi)



Logic Diagram for MOD-6 Synchronous Counter

Decade Counter

8.15.3 Design of BCD or Decade (MOD-10) Counter

To design a BCD or Decade (MOD-10) counter that has ten states i.e., 0 to 9 the number of flip-flops required is four. Let us assume that the MOD-10 counter has ten states, viz. *a, b, c, d, e, f, g, h, i* and *j*.

Step 1 State diagram Now the state diagram for the MOD-10 counter can be drawn as shown in Fig. 8.23. Here, it is assumed that the state transition from one state to another takes place when the clock pulse is asserted. When the clock is unasserted, the counter remains in the present state.

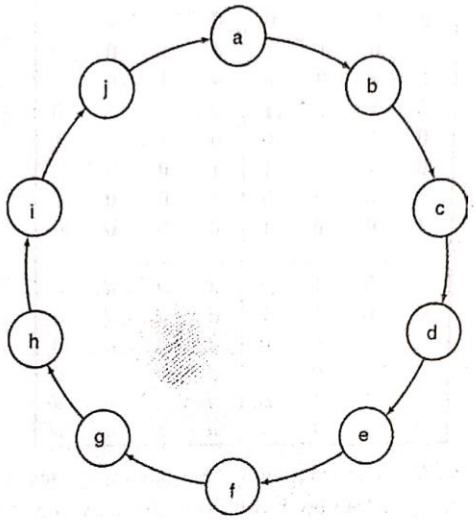


Fig. 8.23 *State diagram of MOD-10 counter*

Step 2 State table From the above state diagram, one can draw the PS-NS table as shown in Table 8.14.

Table 8.14 *PS-NS table for MOD-10 counter*

Present state (PS)	Next state (NS)
a	*b*
b	*c*
c	*d*
d	*e*
e	*f*
f	*g*
g	*h*
h	*i*
i	*j*
j	*a*

The above state table does not have any redundant state because no two states are equivalent. So, there is no modification required in the above state table.

Step 3 State assignment Let us assign four state variables to these states *a, b, c, d, e, f, g, h, i* and *j* as follows: $a = 0000, b = 0001, c = 0010, d = 0011, e = 0100, f = 0101, g =$

0110, $h = 0111$, $i = 1000$ and $j = 1001$. Then, the above PS–NS table can be modified as shown in Table 8.15.

Table 8.15 PS–NS table for MOD-10 counter

Present state (PS)				Next state (NS)			
q_3	q_2	q_1	q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
.....				.....			
1	0	1	0	*d*	*d*	*d*	*d*
1	0	1	1	*d*	*d*	*d*	*d*
1	1	0	0	*d*	*d*	*d*	*d*
1	1	0	1	*d*	*d*	*d*	*d*
1	1	1	0	*d*	*d*	*d*	*d*
1	1	1	1	*d*	*d*	*d*	*d*

Step 4 Excitation table The excitation table having entries for flip-flop inputs (J_3K_3, J_2K_2, J_1K_1 and J_0K_0) can be drawn, from the above PS–NS table using the application table of *JK* flip-flop given earlier, as shown in Table 8.16.

Table 8.16 Excitation table for MOD-10 counter

PS				NS				Excitation inputs							
q_3	q_2	q_1	q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	*d*	0	*d*	0	*d*	1	*d*
0	0	0	1	0	0	1	0	0	*d*	0	*d*	1	*d*	*d*	1
0	0	1	0	0	0	1	1	0	*d*	0	*d*	*d*	0	1	*d*
0	0	1	1	0	1	0	0	0	*d*	1	*d*	*d*	1	*d*	1
0	1	0	0	0	1	0	1	0	*d*	*d*	0	0	*d*	1	*d*
0	1	0	1	0	1	1	0	0	*d*	*d*	0	1	*d*	*d*	1
0	1	1	0	0	1	1	1	0	*d*	*d*	0	*d*	0	1	*d*
0	1	1	1	1	0	0	0	1	*d*	*d*	1	*d*	1	*d*	1
1	0	0	0	1	0	0	1	*d*	0	0	*d*	0	*d*	1	*d*
1	0	0	1	0	0	0	0	*d*	1	0	*d*	0	*d*	*d*	1
.....				.....				.....				.....			
1	0	1	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	0	1	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	0	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	0	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	1	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	1	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*

Step 5 Excitation maps The excitation maps for $J_3, K_3, J_2, K_2, J_1, K_1, J_0$ and K_0 inputs of the counter can be drawn as shown in Fig.8.24 from the Excitation Table 8.16.

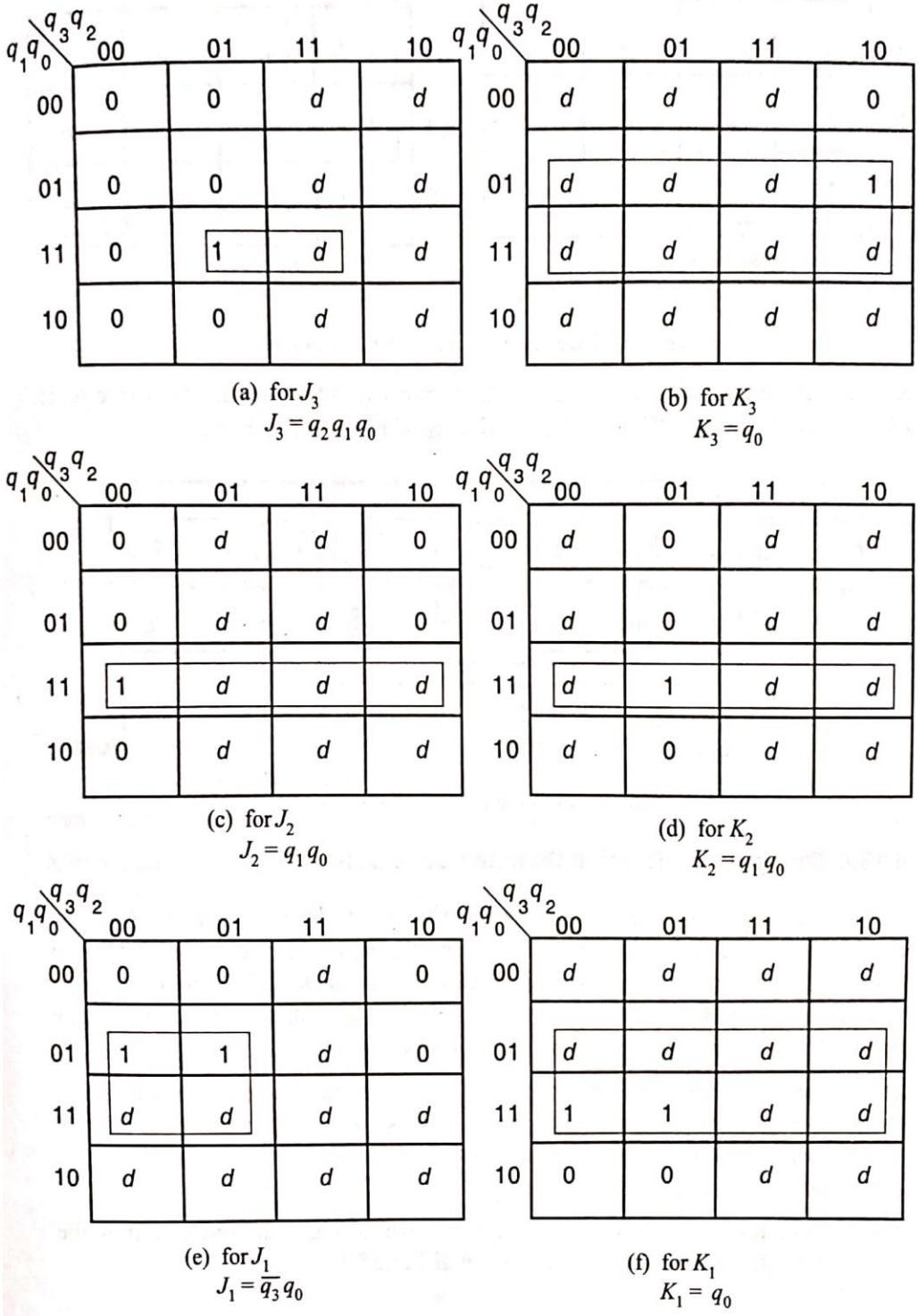


Fig. 8.24 *Excitation maps for MOD-10 counter*

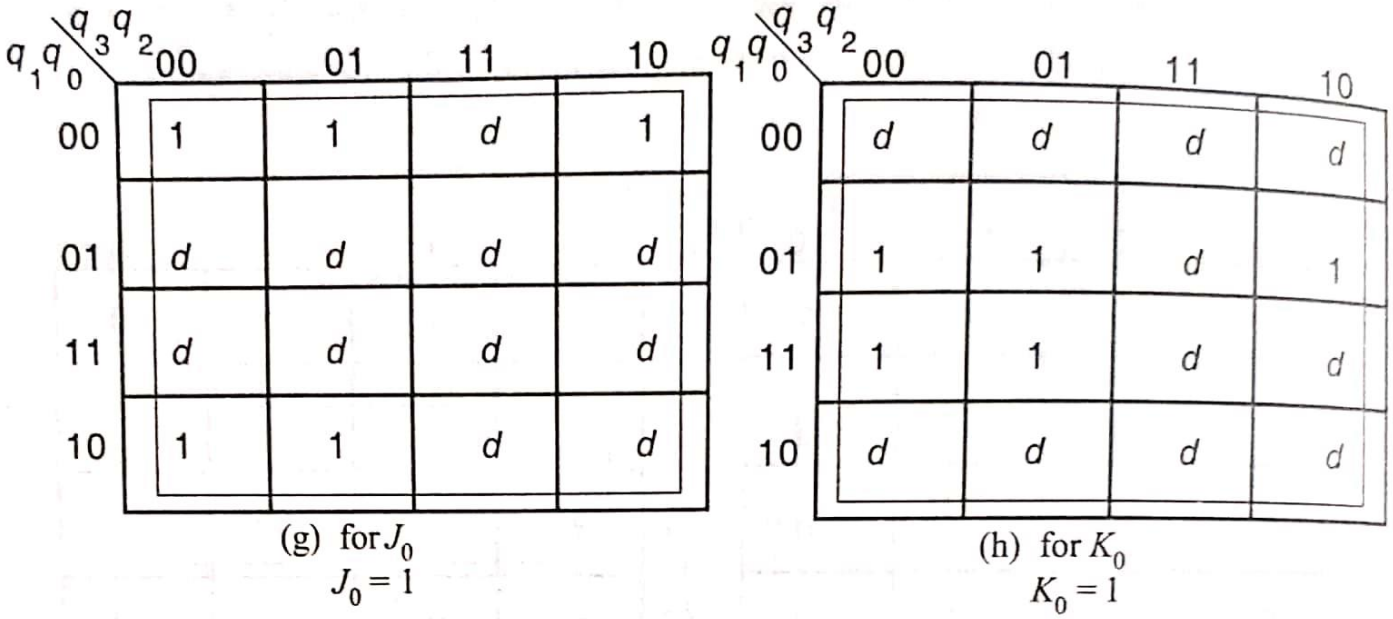


Fig. 8.24 Excitation maps for MOD-10 counter

Step 6 Schematic diagram Using the above excitation equations, the circuit diagram for the MOD-10 counter can be drawn as shown in Fig. 8.25.

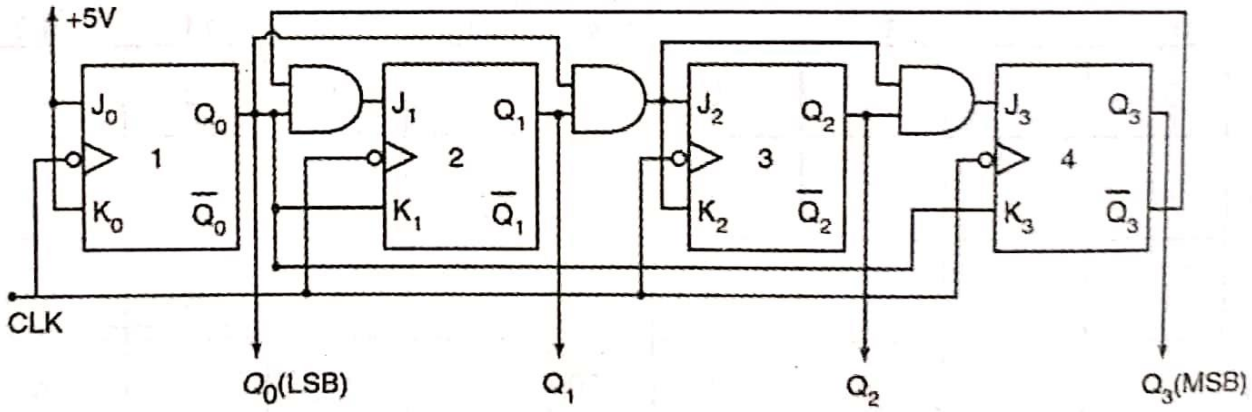


Fig. 8.25 Circuit diagram for MOD-10 synchronous counter