Types of Registers:

1. Segment Registers – There are four segment registers corresponding to four memory segments
    a. DS – Data segment register
    b. CS – Code segment register
    c. ES – Extra segment register
    d. SS – Stack segment register

    Each register should be initialized according to the segment address before use.
2. Offset Pointers
    a. SP – (Stack Pointer) Keeps offset value of a stack segment
    b. BP – (Base Pointer) Keeps offset of Code segment
3. General purpose registers
    a. AX – (Accumulator register) used as an accumulator
    b. BX – (Base Register) Used to keep base address.
    c. CX – (Count register) Used to count a number and "loop" instructions continues until CX≠0
    d. DX – (Data register) Used to keep data

    AX, BX, CX and DX can be used as general purpose registers for any mathematical operations etc. Each of these four register consists of two parts – high and low. For example AH denotes high part of AX and AL denotes the low parts. Similar for BH & BL, CH & CL, DH & DL they have same convention.
4. Index register
    a. SI – (Source Index register) Used as a source index for any string in data segment.
    b. DI – (Destination index register) Used to keep index of data segment string as destination index.

    SI and DI may also be used as a general purpose register.
5. Flag register – There is only one flag register of 16 bits. Out of 16 bits, 9 bits are active. Among those 9 bits 6 bits are conditional flag bits and 3 bits are control flag bits.
    a. Conditional flag bits (status indicator)
        i. AF – Auxiliary flag bit. Checks if there be any carry for four bits (nibble)
        ii. SF – Sign flag bit. Checks sign for an operation. Ex. 0 for positive & 1 for negative
        iii. PF – Parity flag bit
        iv. OF – Overflow flag bit. Indicates if any overflow occurred. 1 for overflow, otherwise 0.
        v. ZF – Zero flag bit. If this bit is 1 then the result is 0, neither positive nor negative.
        vi. CF – Carry flag bit. Indicates if there be any carry in an operation
    b. Control flag bits
        i. TF – Trap flag bit. When it is set to 1, a single step interrupt occurs after the next instruction executes.
        ii. IF – Interrupt flag bit. This indicates whether makeable interrupt will cause the CPU transfer control to an interrupt vector specified location or not

iii. DF – Direction flag bit. Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.

X	X	X	X	OF	DF	IF	TF	SF	ZF	X	AF	X	PF	X	CF

Flag Register with 9 flags