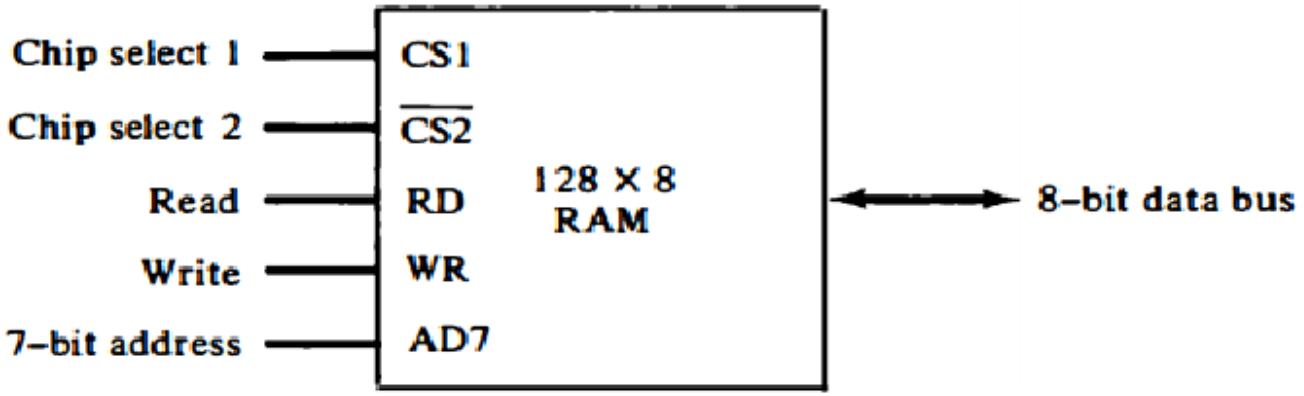
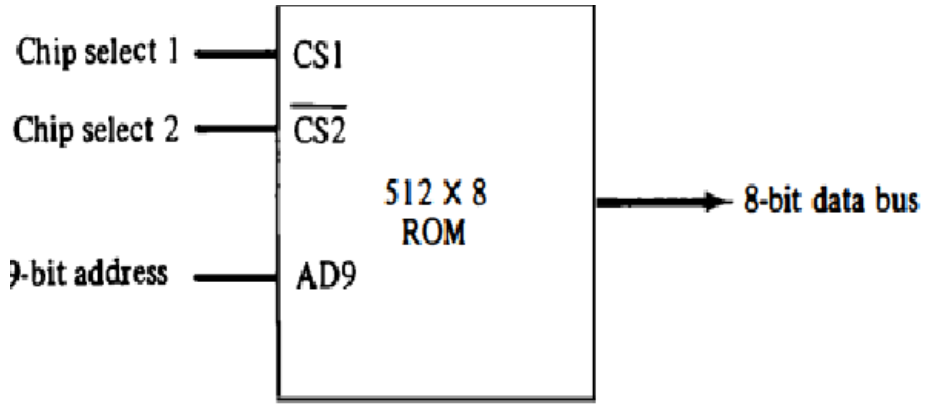
Memory Interconnection (Vertical Expansion)

Typical RAM chip.

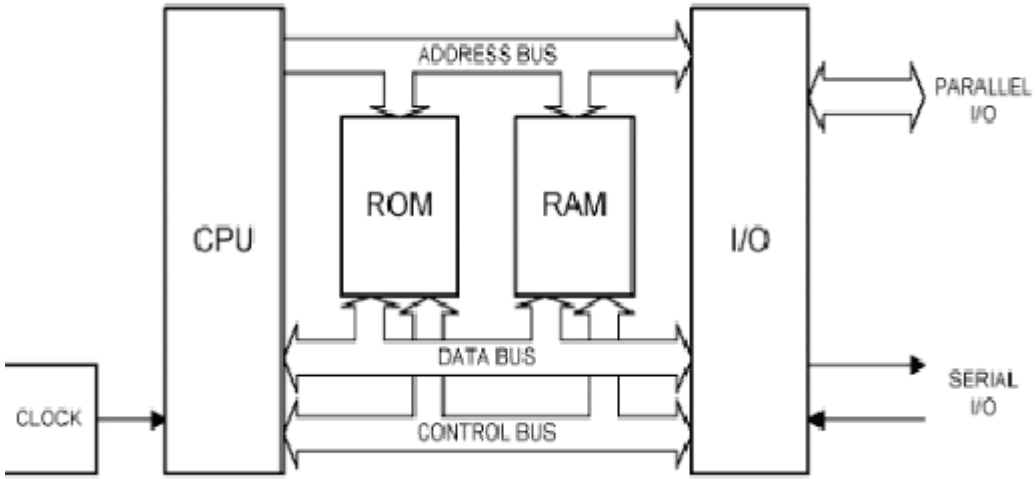


CS1	$\overline{CS2}$	RD	WR	Memory function	State of data bus
0	0	×	×	Inhibit	High-impedance
0	1	×	×	Inhibit	High-impedance
1	0	0	0	Inhibit	High-impedance
1	0	0	1	Write	Input data to RAM
1	0	1	×	Read	Output data from RAM
1	1	×	×	Inhibit	High-impedance

Function table



Typical ROM chip.



Q. SUPPOSE WE HAVE 2 SETS OF MEMORIES WITH RAM OF SIZE 128 X 8 AND ROM OF SIZE 512 X 8, we need to design a memory of capacity 1024 x 8. Draw the memory mapping table.

Solution:

FOR EACH RAM (128 X 8):

ADDRESS BUS SIZE = 7 BITS

DATA BUS SIZE = 8 BITS

FOR ROM (512 X 8):

ADDRESS BUS SIZE = 9 BITS

DATA BUS SIZE= 8 BITS

VERTICAL/ HORIZONTAL

SMALLEST ADDRESS (RAM) – 0

LARGEST ADDRESS (RAM) – 127

SMALLEST ADDRESS (ROM) – 0

LARGEST ADDRESS (ROM) – 511

For the required expanded memory size 1024 X 8 (EXPANDED)

SMALLEST ADDRESS (EXPANDED) = 0

LARGEST ADDRESS (EXPANDED) = 1023

ADDRESS BUS SIZE ((EXPANDED) = 10

DATA BUS SIZE (EXPANDED) = 8

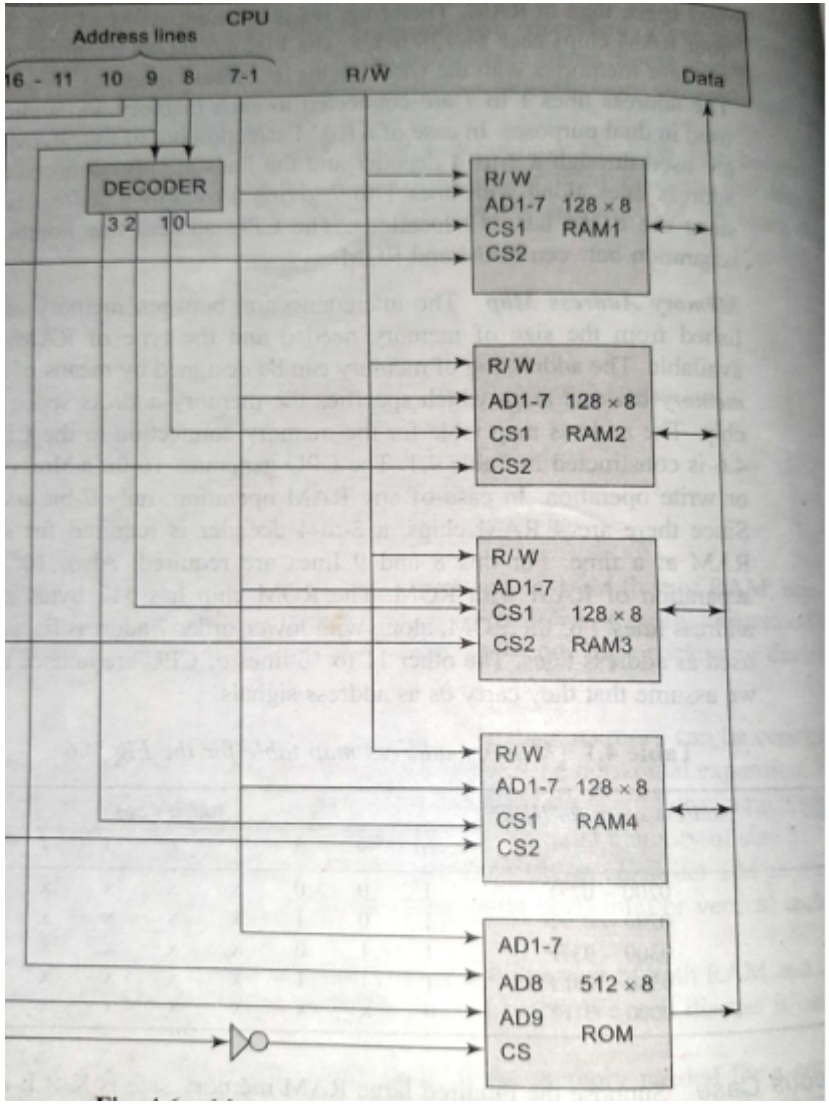
Memory Mapping Table:

ITEMS	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

RAM1	1/0	0	0	X	X	X	X	X	X	X
RAM2	1/0	0	1	X	X	X	X	X	X	X
RAM3	1/0	1	0	X	X	X	X	X	X	X
RAM4	1/0	1	1	X	X	X	X	X	X	X
ROM	0/1	X	X	X	X	X	X	X	X	X

Vertical Expansion:

Memory Interconnection Diagram for a 16 bit CPU


CPU
Address lines
16 - 11
10
9
8
7-1
R/W
Data
DECODER
3 2
1 0
R/ W
AD1-7
CS1
CS2
128 × 8
RAM1
R/ W
AD1-7
CS1
CS2
128 × 8
RAM2
R/ W
AD1-7
CS1
CS2
128 × 8
RAM3
R/ W
AD1-7
CS1
CS2
128 × 8
RAM4
AD1-7
AD8
AD9
CS
512 × 8
ROM