20MCA103	DIGITAL FUNDAMENTALS & COMPUTER ARCHITECTURE	CATEGORY	L	T	P	CREDIT
		GENERAL	3	1	0	4

Preamble:

The primary aim of this course is to understand the fundamentals behind the digital logic design and gain the experience to design digital circuits and systems. Students should also acquire some understanding and appreciation of a computer system's functional components, their characteristics, performance and interactions. They need to understand the computer architecture in order to make best use of the software tools and computer languages they use to create programs.

Prerequisite: NIL

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply the basics of digital electronics to design and realize simple combinational logic circuits
CO 2	Apply the digital electronics principles to design sequential logic circuits.
CO 3	Understand the different design features of computer architecture, Five key components of a computer, processor and memory making technologies, addressing modes & instruction formats.
CO 4	Understand Processor logic design conventions and data path, pipelining and hazards, I/O organization, Interrupts and direct memory access
CO 5	Understand and different types of memories - RAM, ROM, Cache memory, virtual memory etc. Apply the different memory design techniques.
CO 6	Understand the concept of single board computers like Arduino, Raspberry Pi etc. and apply the same in practical applications.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	2	1	-	-	1	-	-	-	-	-
CO 2	3	3	2	1	-	-	1	-	-	-	-	-
CO 3	1	1	-	1	-	-	1	-	-	-	-	-
CO 4	1	1	-	-	-	-	1	-	-	-	-	-
CO 5	2	2	1	1	-	-	1	-	-	-	-	-
CO 6	1	1	2	-	2	-	2	2	2	-	2	2

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	20	20	20
Apply	20	20	20
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 8 marks
Continuous Assessment Test (2 numbers) : 20 marks
Assignment/Quiz/Course project : 12 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 6 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1):

1. Minimize the Boolean Expression $f(A,B,C) = \Sigma m(1,3,5,6,7)$ using K-map.

2. Convert the decimal number $3.257 * 10^4$ into single precision floating point binary representation

3. Express -31 in sign magnitude,1's complement and 2's complement notations

Course Outcome 2 (CO2)

1. Explain J-K flipflop with its truth table

2. Design an asynchronous decade counter.

3. Describe the working of a Parallel in Serial Out register.

Course Outcome 3 (CO3):

1. Describe the key components of a computer.

2. Define addressing mode. List 5 addressing modes with examples.

3. Differentiate between fixed length encoding and variable length encoding.

Course Outcome 4 (CO4):

1. Define pipeline, describe how pipeline improves the performance of the machine.

3. List different types of pipeline hazards with examples.

2. Explain how interrupts from multiple devices handled?

Course Outcome 5 (CO5):

1. Illustrate different cache mapping techniques with neat diagrams.

2. Discuss about Read Only Memories

3. Design 2M*32 memory module using 512K *8 static memory chips.

Course Outcome 6 (CO6):

No questions for university examination, for internal assessments practical assignment for configuring a PC / arduino or raspberry and programming assignments using HDL like Verilog or VHDL can be given.

Model Question paper

Reg No.:_____		Name:_____	
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FIRST SEMESTER M.C.A.DEGREE EXAMINATION, MODEL QUESTION PAPER			
Course Code: 20MCA103			
Course Name: DIGITAL FUNDAMENTALS & COMPUTER ARCHITECTURE			
Max. Marks: 60		Duration: 3 Hours	

PART A

			Marks
		Answer all questions, each carries 3 marks.	
1		Represent +45,-45 in 1's complement and 2's complement form.	(3)
2		Implement a full adder using 8:1 MUX	(3)
3		How could you convert RS flip flop to D flip flop?	(3)
4		What is meant by modulus of a counter? Realize a mod-8 synchronous counter.	(3)
5		Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?	(3)
6		Describe about little endian and big endian byte ordering.	(3)
7		Explain 4 stage pipelining with a diagram.	(3)
8		Differentiate between memory mapped I/O and Isolated I/O	(3)
9		What is static RAM ?	(3)
10		Define temporal locality and spatial locality.	(3)

PART B

Answer any one question from each module. Each question carries 6 marks.

		Module I	
11		Explain about single precision floating point representation with an example	(6)
		OR	
12		Minimize the Boolean expression f(A,B,C,D)=Σm(1,5,6,7,9,15)+d(2,3,11,13) using Karnaugh map and realize it using NAND gates.	(6)

		Module II	
13		Demonstrate the working of a JK flip flop. How does it eliminate the invalid condition in SR flip flop? List out its applications.	(6)
		OR	
14		Design a mod-12 asynchronous counter.	(6)
		Module III	
15		Explain the five classic components of a computer with diagram.	(6)
		OR	
16		Describe the code sequence of C=A+B in different types of instruction set architecture.	(6)
		Module IV	
17		Draw a single datapath representation for memory instructions and R-type instructions	(6)
		OR	
18		What is Direct Memory Access? Explain two types of bus arbitration schemes	(6)
		Module V	
19		Elaborate the various cache memory mapping techniques with an example for each.	(6)
		OR	
20		Explain the internal organization of memory chips and design a 1K*1 memory chip using decoder.	(6)

Syllabus

Module I (11 Hours)

Representation of signed numbers – 1's complement and 2's complement ,Logic gates – AND - OR – NOT - NAND- NOR - XOR , Boolean algebra - Basic laws and theorems , Boolean functions - truth table, Standard forms of Boolean Expressions – Sum of Products and Product of Sums - minimization of Boolean function using Karnaugh map method - Realization using logic gates, Floating point numbers

Combinational Circuits - Half adder - Full Adder- Decoder -Encoder- Multiplexer – Demultiplexer

Module II (10 Hours)

Sequential circuit - Clocking, Flip flops - SR – JK- D -T flip flops, Counters - Synchronous and asynchronous counters - UP/DOWN counters , Registers - Serial in serial out - Serial in parallel out - Parallel in serial out - Parallel in parallel out registers

A practical assignments may be given in configuring a PC / configuring arduino - Implementing simple programs for blinking an LED - Input from an external switch - fading an LED - serial monitor and debugging / installing & configuring Raspberry pi.

Module III (10 Hours)

Computer abstractions and technology - Introduction, Computer architecture -8 Design features, Application program - layers of abstraction, Five key components of a computer, Technologies for building processors and memory, Performance, Instruction set principles – Introduction, Classifying instruction set architectures, Memory addressing, Encoding an instruction set.

Module IV (9 Hours)

The Processor - Introduction, Logic design conventions, Building a datapath, A simple implementation scheme, An overview of pipelining - Pipelined datapath and control - Structural hazards - Data hazards - Control hazards

I/O organization - Accessing I/O devices, interrupts - handling multiple devices, Direct memory access

Programming assignments may be given in any HDL like Verilog or VHDL to create gate level/ Dataflow/Behavioural level models of gates, multiplexers, adders, flip-flops, registers etc. No detailed teaching of HDL is necessary. The students can be given a basic tutorial write up on gate level modelling.

Module V (8 Hours)

The Memory System – basic concepts, semiconductor RAM memories - organization – static and dynamic RAM, Structure of larger memories, semiconductor ROM memories, Speed, Size and cost ,Cache memory – mapping functions – replacement algorithms , Virtual memory – paging and segmentation.

Text Books

1. Floyd, "***Digital Fundamentals***", Pearson Education, 10th Edition (2011).(Module 1 & 2)
2. J. Hennessy and D. Patterson, "***Computer Organization and Design: The Hardware/Software Interface***", 5th Edition. (Module 3 & 4)
3. J. Hennessy and D. Patterson, "***Computer Architecture, A quantitative approach***", 5th Edition. (Module 3)
4. Hamacher, Vranesic & Zaky, "***Computer Organization***" (5th Ed), McGraw Hill. (Module 4 & 5)

References

1. William Stallings, "***Computer Organization and Architecture: Designing for Performance***", Pearson, 9/e, 2013.
2. R.P.Jain ,"***Modern Digital Electronics***", McGraw Hill.,Fourth Edition,2009
3. Mano, "***Digital Design : With an Introduction to Verilog HDL***", Pearson Education, 5th Edition (2014)

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
	Module 1	**11**
1	Representation of signed numbers – 1's complement and 2's complement, Logic gates - AND, OR, NOT, NAND, NOR, XOR	2
1.1	Boolean algebra - Basic laws and theorems, Boolean functions - truth table.	2
1.2	Standard forms of Boolean Expressions – Sum of Products and Product of Sums - minimization of Boolean function using Karnaugh map method - Realization using logic gates.	2
1.3	Floating point numbers	1
1.4	Combinational Circuits - Half adder - Full Adder	2
1.5	Decoder – Encoder - Multiplexers – Demultiplexers	2
	Module 2	**10**
2.1	Sequential circuit - Clocking, Flip flops -RS – JK- D -T flip flops	3
2.2	Counters - Synchronous and asynchronous counters - UP/DOWN counters.	3
2.3	Registers - Serial in serial out - Serial in parallel out - Parallel in serial out - Parallel in parallel out registers	2
2.4	Introduction to arduino and raspberry pi	2
	Module 3	**10**
3.1	Computer abstractions and technology - Introduction, Computer architecture	4
3.2	Technologies for building processors and memory, Performance, instruction	4
3.3	Classifying instruction set architectures, Memory addressing, Encoding an	2
	Module 4	**9**
4.1	The Processor - Introduction, Logic design conventions, Building a datapath, A simple implementation scheme.	3
4.2	An Overview of pipelining - Pipelined datapath and control - Structural hazards - Data hazards - Control hazards	3
4.3	I/O organization - Accessing I/O devices, Interrupts - Handling multiple devices- Direct memory access	3

No	Topic	No. of Lectures
	Module 5	**8**
5.1	The memory system – basic concepts, semiconductor RAM memories, organization	2
5.2	Static and dynamic RAM, Structure of larger memories, semiconductor ROM memories, Speed, size and cost	2
5.3	Cache memory – mapping functions – replacement algorithms,	2
5.4	Virtual memory – paging and segmentation.	2

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