

Final Project — Design of an interleaved flyback converter

Ye Yuan

ECE Department, University of Toronto

Student Number: 1001614247

Abstract. Interleaving topology has many advantages over traditional converter topology, the most significant one is that we can reduce the value of inductor and capacitor while keep the same ripple level. This report illustrates how to build an interleaved flyback converter for both power stage and the controller design. The First part is the power stage design, about the selection of duty ratio D, output capacitor C and flyback inductor L. After this part, we can make sure our converter meet the specifications in steady state. The second part is about controller. We work out the line-to-out transfer function $G_{vg}(s)$, control-to-output transfer function $G_{vd}(s)$ and output impedance $Z_{out}(s)$. Based on the bode diagram of $G_{vd}(s)$, We can design our compensator using algebra on graph method, Then we can easily derive the analog implementation of the controller .We also design an input filter and digital compensator. At last, We verify all the design work in PLECS, confirm all the work based on theoretical analysis is correct.

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1 Introduction

Interleaving topology is quite useful because it enhance the performance of the converter in many aspects,such as ripple level, RMS value of current of the inductor, ect. More specifically [1]:

Reduced RMS current in the input capacitors enabling the use of less expensive and fewer input capacitors

Ripple current cancellation in the output capacitor, enabling the use of less expensive and fewer output capacitors

Reduction of peak currents in primary and secondary transformer windings

Improved transient response as a result of reduced output filter inductance and higher output ripple frequency

So let's analyze why this topology has so much merits.

2 Power stage design

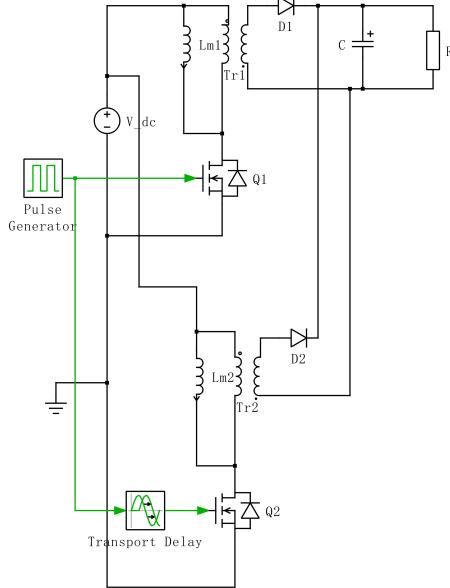


Figure 1: The Scheme of interleaved flyback converter

The interleaved flyback converter is shown in Fig 1. The design specifications are:

Input voltage: 100V

Output voltage: 5V

Output current: 10A

Maximum output capacitor voltage ripple: 1%

Maximum inductor current ripple: 20%

Maximum input current ripple: 5%

2.1 Interleaved flyback converter analysis

Fig 1 clarify what "two phase" means. The input current is divided into two branches. The circuit is exactly the same for the two branches except there's a phase delay of $\frac{1-2D}{2}T_s + DT_s = \frac{1}{2}T_s$ (It's allowed to place the phase delay randomly even without phase delay, all these won't influence the transfer function of the conveter). However, if we place the on-time for each phase evenly, we can minimize the ripple level of output capacitor). Compare with the traditional flyback converter, the most significant advantage of this topology is the ability of reducing the output voltage ripple level.

In Fig 2, the i_{lm1} and i_{lm2} refer to the current of L_{m1} and L_{m2} , respectively. i_{ls} represent the summation of the current after D_1 and D_2 . For each subinterval, we can obtain:

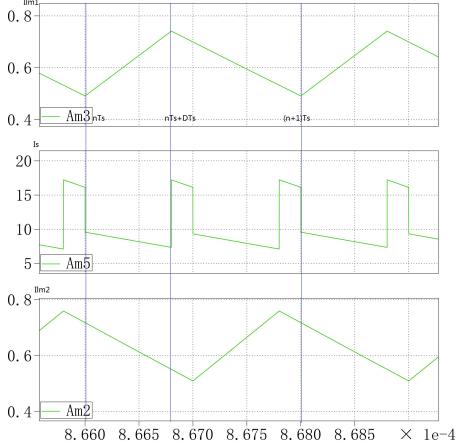


Figure 2: The waveform of i_{lm} and i_s

$$\frac{di_{lm}}{dt} = \frac{V_g}{L_m} \dots \text{When MOSFET is on} \quad (2.1)$$

$$\frac{di_{lm}}{dt} = \frac{-nV_{out}}{L_m} \dots \text{When MOSFET is off} \quad (2.2)$$

When the MOSFET is on for one phase, the corresponding diode in the secondary side is off. i_{lm} increases linearly. After MOSFET turns off, i_{lm} decreases linearly. Fig 2 shows the case when duty ratio D is less than 0.5.

For $nT_s \sim nT_s + DT_s$, MOSFET1 is on, the only conducting diode in this subinterval is D_2 . For $nT_s + DT_s \sim 0.5DT_s + nT_s$ and $(n+1)T_s - \frac{1-2*DT_s}{2} \sim (n+1)T_s$, all of the two diodes are conducting. The current i_s becomes $n(i_{lm1} + i_{lm2})$! For all the other part, D_1 is conducting. These behaviors can significantly reduce the size of output capacitor due to the continuous secondary side current. Also, because there're two inductors used for energy transfer, the average current value of each inductor is only a half of the traditional flyback converter.

2.2 Interleaved flyback converter design

We can do the steady state analysis for this converter:

$$v_{Lm} = V_g \dots \text{When MOSFET is on} \quad (2.3)$$

$$v_{Lm} = -nV_{out} \dots \text{When MOSFET is off} \quad (2.4)$$

$$i_c = n(i_{lm1} + i_{lm2}) - \frac{v}{R} \dots nT_s + DT_s \sim .nT_s + 0.5T_s \text{ and } (n+1)T_s - \frac{1-2*DT_s}{2} \sim (n+1)T_s \quad (2.5)$$

$$i_c = ni_{lm1} - \frac{v}{R} \text{ or } i_c = ni_{lm2} - \frac{v}{R} \dots \text{for all the other time} \quad (2.6)$$

For the two phase are exactly the same except a phase delay:

$$I_{Lm1} = I_{Lm2} \quad (2.7)$$

Using capacitor charge balance, inductor charge balance and small ripple approximation, we can obtain:

$$\langle v_{Lm} \rangle_{T_s} = DV_g - D'nV \quad (2.8)$$

$$\langle i_c \rangle_{T_s} = n * 2 * I_{Lm}(1 - 2 * D) + n * 2 * DI_{Lm} - \frac{V}{R} = (2 - 2D)nI_{Lm} - \frac{V}{R} \quad (2.9)$$

$$\langle i_g \rangle_{T_s} = 2DI_{Lm} \quad (2.10)$$

We can now obtain the DC solution of this interleaved flyback converter:

$$V = \frac{D}{D'n}V_g \quad (2.11)$$

$$I_{Lm} = \frac{V}{R(2 - 2D)n} \quad (2.12)$$

$$I_g = 2D \frac{V}{R(2 - 2D)n} \quad (2.13)$$

Let:

$$\Delta v = 1\%V \quad (2.14)$$

$$\Delta i_{Lm} = 20\%I_{Lm} \quad (2.15)$$

Then we write down the expressions for the ripple:

$$2\Delta V = \frac{\Delta Q}{C} \quad (2.16)$$

$$\Delta Q = \frac{1 - 2D}{2} T_s (2nI_{Lm} - I) \quad (2.17)$$

$$2\Delta I_{Lm} = \frac{V_g}{L} DT_s \quad (2.18)$$

Note that the frequency I_{ls} is two times of the frequency of I_{Lm} , which means: for one period of the switch, the output capacitor has been charging and discharging twice! So we just need calculate one of them. For each subinterval, when only one diode conducts, the capacitor is discharging due to nI_{Lm} is less than I . The time period for two diodes conduct simultaneously is $\frac{1-2D}{2}T_s$.

Let's assign the switching frequency and duty ratio to be:

$$f_s = 500Khz \quad (2.19)$$

$$D = 0.4 \quad (2.20)$$

The duty ratio of the switch is 0.4 (just as the case we analyzed before when D is less than 0.5). Plug in all the known quantities, we can solve all the unknowns of this converter. The solutions of this converter are shown next part.

2.3 Summary of the power stage design and component selection

$$L_{m1} = L_{m2} = 320\mu H \quad (2.21)$$

$$C = 13.33\mu F \quad (2.22)$$

$$n = 200 : 15 \quad (2.23)$$

$$D = 0.4 \quad (2.24)$$

$$R = \frac{V}{I} = 0.5\Omega \quad (2.25)$$

$$I_{Lm} = 0.625A \quad (2.26)$$

Also, we can obtain:

$$i_{Lm1max} = i_{Lm2max} = 0.75A \quad (2.27)$$

$$v_{Lm1max} = v_{Lm2max} = 100V \quad (2.28)$$

$$v_{Qmax} = 166.6V \quad (2.29)$$

$$i_{Qmax} = 0.75A \quad (2.30)$$

$$v_{Dmax} = -12.5V \quad (2.31)$$

$$i_{Dmax} = i_D(DTs) = 17.22A \quad (2.32)$$

$$i_{Cmax} = i_C(DTs) = 7.22A \quad (2.33)$$

We can choose:

$$\text{PowerMOSFET : STF7NK30Z}(N - \text{CHANNEL}, 300V, 0.80\text{Ohm}, 5A) \quad (2.34)$$

$$\text{PowerDiode : SMCJ20CA - LF}(20V, 46.3A) \quad (2.35)$$

$$\text{Inductor : PF0553.823NL}(320\mu H, V_{max}570V, i_{max}2A) \quad (2.36)$$

$$\text{Capacitor : BP - Tseries}(100V, Bi - polarCapacitor) \quad (2.37)$$

2.4 Verify power stage in PLECS

To verify the design, an interleaved flyback converter is built in PLECS. Fig 3 shows the detailed ripple.

Fig 3 clearly shows the ripples (or the values of capacitor and inductor) level meets the design specs.

3 Small signal analysis and controller design

3.1 Small signal analysis

To obtain the transfer function of the converter, the first thing we need to do is small signal analysis. After averaging and perturbation, all the variables can be expressed like:

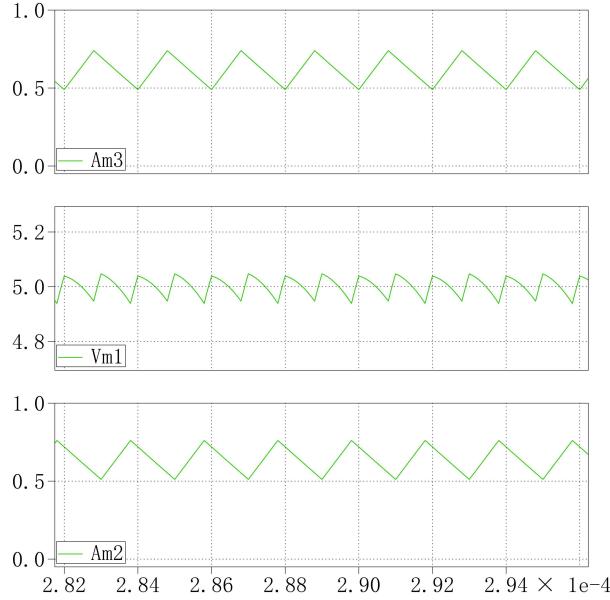


Figure 3: ripples

$$v(t) = V + \hat{v} \quad (3.1)$$

$$i_{Lm}(t) = I_{Lm} + i_{Lm}^{\hat{}} \quad (3.2)$$

$$i_g(t) = I_g(t) + i_g^{\hat{}}(t) \quad (3.3)$$

$$D(t) = D + \hat{d} \quad (3.4)$$

$$v_g(t) = V_g + \hat{v}_g \quad (3.5)$$

After applying volt-second balance and capacitor charge balance, we can obtain the mathematical model of this perturbed system:

$$Lm \frac{d(I_{Lm} + i_{Lm}^{\hat{}})}{dt} = (D + \hat{d})(V_g + \hat{v}_g) - (D' - \hat{d})n(V + \hat{v}) \quad (3.6)$$

$$C \frac{d(V + \hat{v})}{dt} = n * 2 * (I_{Lm} + i_{Lm}^{\hat{}})(1 - D - \hat{d}) - \frac{V + \hat{v}}{R} \quad (3.7)$$

$$I_g(t) + i_g^{\hat{}}(t) = 2(D + \hat{d})(I_{Lm} + i_{Lm}^{\hat{}}) \quad (3.8)$$

We can see three types of terms arise in the right side of the equations[2]:

Dc terms

First-order ac terms

Second-order ac terms

Collect all the DC terms, we can get the large signal model:

$$\langle V_{Lm} \rangle_{T_s} = 0 = DV_g - D'nV \quad (3.9)$$

$$\langle I_c \rangle_{T_s} = 0 = n * 2 * I_{Lm}(1 - 2 * D) + n * 2 * DI_{Lm} - \frac{V}{R} = (2 - 2D)nI_{Lm} - \frac{V}{R} \quad (3.10)$$

$$\langle I_g \rangle_{T_s} = 2DI_{Lm} \quad (3.11)$$

Because the second-order terms are much smaller than the linear terms, we can neglect them so that we can get our linearized small signal model :

$$Lm \frac{d\hat{i}_{Lm}}{dt} = \hat{d}V_g + \hat{v}_g D - D'n\hat{v} + \hat{d}nV \quad (3.12)$$

$$C \frac{d(\hat{v})}{dt} = 2D'n\hat{i}_{Lm} - 2\hat{d}nI_{Lm} - \frac{\hat{v}}{R} \quad (3.13)$$

$$\hat{i}_g = 2\hat{d}I_{Lm} + 2D\hat{i}_{Lm} \quad (3.14)$$

3.2 Equivalent circuit

Based on the analysis above, we can draw the equivalent circuit for both large signal and small signal. Drawing these equivalent circuits will simplify our later analysis greatly. Fig 4 and Fig 5 show the result.

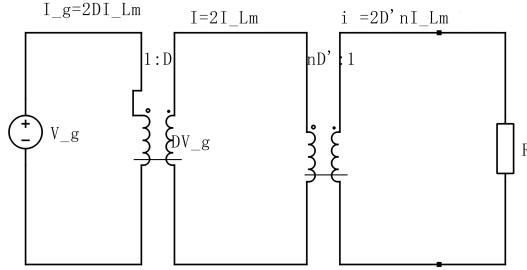


Figure 4: Large signal equivalent circuit

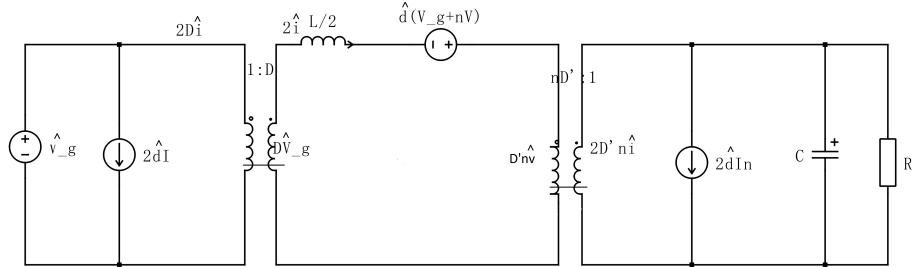


Figure 5: Small signal equivalent circuit

3.3 Obtaining the transfer function

From small signal equivalent circuit, we can obtain the transfer functions of this converter, including: line-to-out $G_{vg}(s)$, control-to-output transfer function $G_{vd}(s)$ and output impedance $Z_{out}(s)$.

When we calculate the control-to-output transfer function $G_{vd}(s)$, just let $\hat{v}_g = 0$. We can derive:

$$\hat{v} = \frac{\hat{d}(V_g + nV)}{D'n} \frac{R \parallel \frac{1}{sC}}{R \parallel \frac{1}{sC} + \frac{sL/2}{(D'n)^2}} - 2\hat{d}I_{Lm}n(R \parallel \frac{1}{sC} \parallel \frac{sL/2}{(D'n)^2}) \quad (3.15)$$

Then can obtain:

$$G_{vd} = \frac{\hat{v}}{\hat{d}} = \frac{Vg}{D'^2n} \left(\frac{2RD'^2n^2 - \frac{D}{R}sLR}{2RD'^2n^2 + Ls + s^2LRC} \right) \quad (3.16)$$

Finally, plug in all the known quantities. Then the transfer function is given by:

$$G_{vd} = 20.83 \frac{1 - 2 * 10^{-6}s}{1 + 5 * 10^{-6}s + 3.33 * 10^{-11}s^2} \quad (3.17)$$

If let all $\hat{d} = 0$, from the equivalent circuit, we can derive line-to-out transfer function $G_{vg}(s)$:

$$\frac{\hat{v}}{\frac{D\hat{v}_g}{D'n}} = \frac{R \parallel \frac{1}{sC}}{R \parallel \frac{1}{sC} + \frac{sL/2}{(D'n)^2}} \quad (3.18)$$

Again, we can obtain the result:

$$G_{vg} = \frac{\hat{v}}{\hat{v}_g} = \frac{D}{D'n} \frac{1}{1 + s \frac{L}{2(D'n)^2 R} + s^2 \frac{LC}{2(D'n)^2}} \quad (3.19)$$

$$G_{vg} = 0.05 \frac{1}{1 + 5 * 10^{-6}s + 3.33 * 10^{-11}s^2} \quad (3.20)$$

Similarly, we can obtain the output impedance by inspecting from the output port, which is:

$$Z_{out}(s) = \frac{sL}{2(D'n)^2} \parallel \frac{1}{sC} \quad (3.21)$$

$$Z_{out}(s) = \frac{sL}{2(D'n)^2 + s^2LC} \quad (3.22)$$

$$Z_{out}(s) = \frac{2.5 * 10^{-6}s}{1 + 3.33 * 10^{-11}s^2} \quad (3.23)$$

3.4 Verify the transfer function in PLECS

PLECS provides us a convenient way to analyse the transfer function of the converter, thus we can use this analysis tools to verify our solution by adding perturbations around operating point like Fig 6:

The simulated transfer function is the same as what we obtained before. (For the PLECS doesn't allow open circuit when we measure output impedance, the output impedance is simulated in MATLAB).

3.5 Design of PID compensator

Fig 8 shows the transfer function of G_{vd} . To improve the system's performance, we can increase the low frequency gain and also improve the phase margin on crossover frequency (Which is the frequency when $|G_{vd}| = 0$). Also, due to the characteristic of op-amp, the high frequency gain can't be too high.

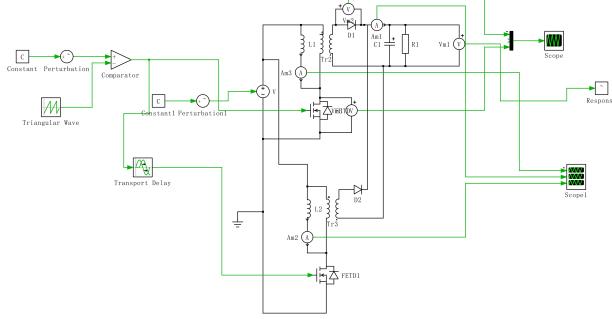


Figure 6: Small signal analysis in PLECS

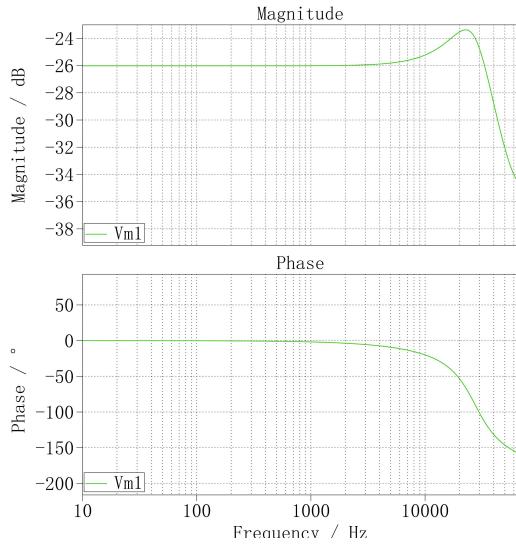


Figure 7: Simulated bode diagram of G_{vg}

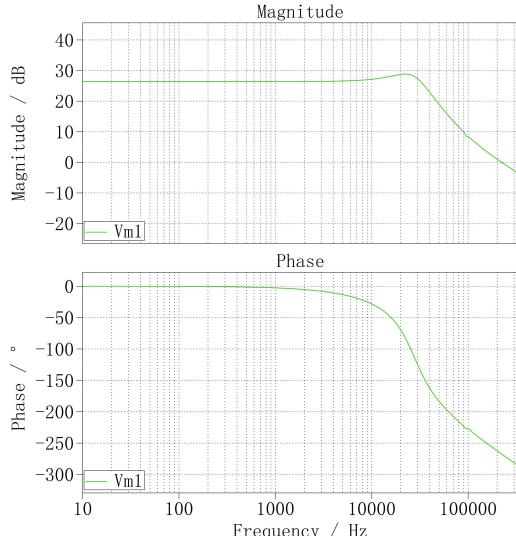


Figure 8: Simulated bode diagram of G_{vd}

Assume that the voltage divisor $H(s)$ and maximum voltage of Pulse-Width-Modulator are $\frac{1}{5}$ and 2V, respectively, we can get:

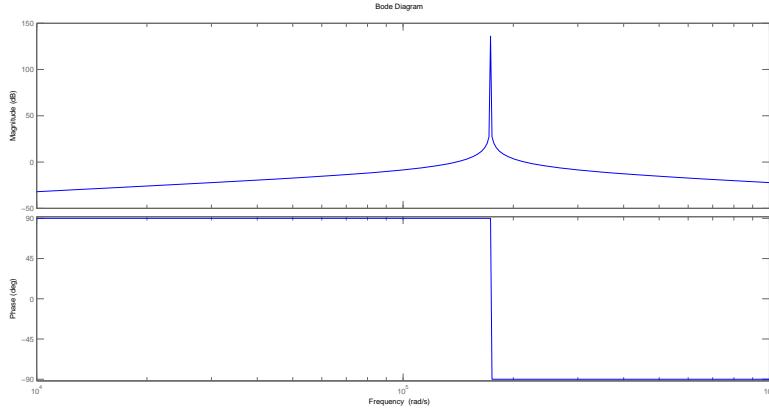


Figure 9: Simulated bode diagram of Z_{out}

$$H(s) = \frac{1}{5} \quad (3.24)$$

$$PWM(s) = \frac{1}{V_m} = \frac{1}{2} \quad (3.25)$$

$$V_{ref} = 1V \quad (3.26)$$

Also, before we start our design, let's just make crossover frequency $\omega_c = 300Krad/s$, which is slightly lower than $\frac{1}{10}$ of the switching frequency. Based on our requirements, the bode diagram of our PID should be like Fig 10[2]:

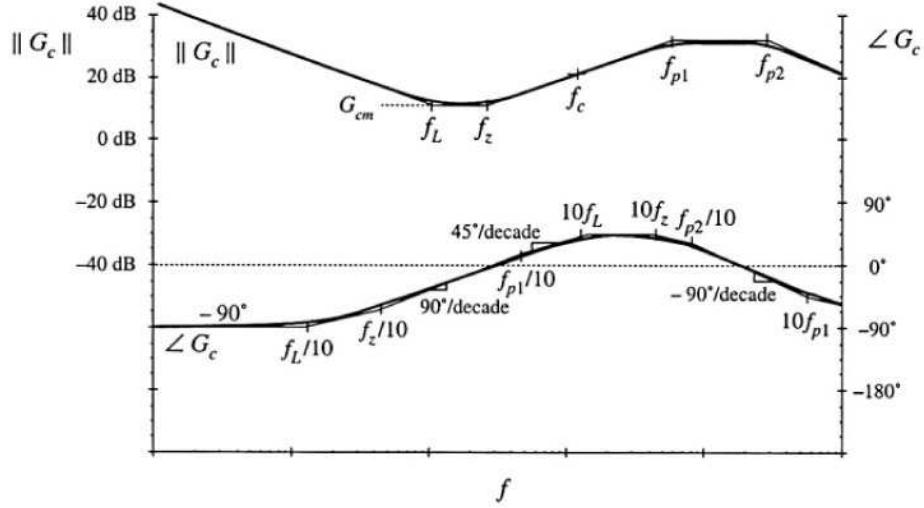


Figure 10: Magnitude and phase asymptotes of the combined (PID) compensator

The corresponding transfer function is:

$$G_c(s) = G_c \frac{(1 + \frac{\omega_L}{s})(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \quad (3.27)$$

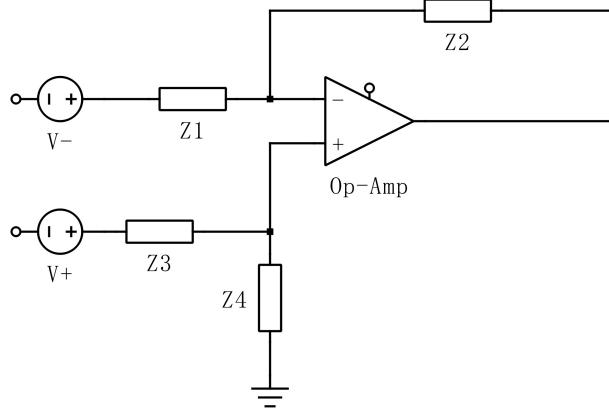


Figure 11: op-amp circuit example

3.6 Using algebra on graph method constructing the op-amp compensator

For Fig 11, if $Z_3 = Z_1$ and $Z_4 = Z_2$, we can get:

$$V_{out} = \frac{Z_2(s)}{Z_1(s)}(V^+ - V^-) \quad (3.28)$$

If we don't consider the negative feedback and the reference right now, our goal is to construct a combination of impedance to make the bode diagram of $\frac{Z_2(s)}{Z_1(s)}$ just like what we have shown in Fig fig:PID. Now things become much easier, if the magnitude of $\frac{1}{Z_1(s)}$ and Z_2s are like:

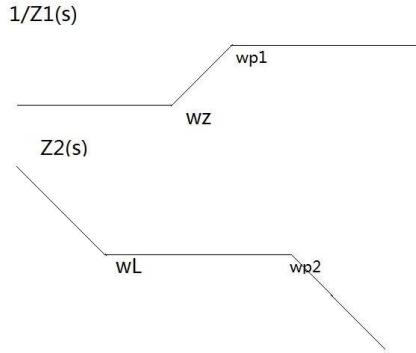


Figure 12: Constructing the bode diagram of $\frac{1}{Z_1}$ and Z_2

Based on our previous experience, we can construct circuit like Fig 13.

These circuits make sense because of algebra on graph method. The method told us when two or more elements are in series, the impedance will be the largest one. Also, when two or more elements are in parallel, the whole impedance will be determined by the smallest one.

For Z_2 , when in low frequently, $\frac{1}{sC_2} + R_2$ are the dominant term, for even lower frequency, C_2 is the dominant term because low frequency the impedance of capacitor is nearly infinity. As frequency becomes higher, the impedance of C_2 drop gradually. After the frequency larger than $\frac{1}{sC_2} = R_2$, R_2 become the leading term of the two series component (Because R_2 now is the

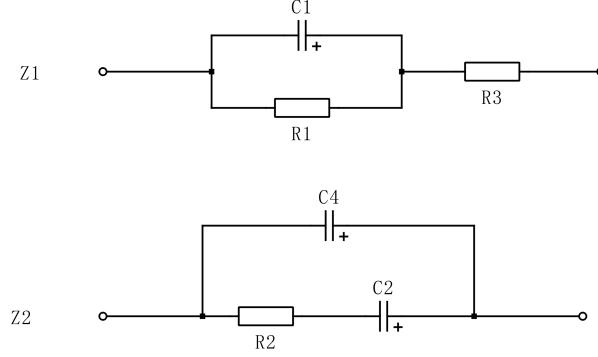


Figure 13: Constructing of Z_1 and Z_2

larger one of the two component). When frequency becomes even higher, such that $\frac{1}{sC} = R_2$, C_4 becomes the dominant term because it's impedance is the smaller one of the two branches'.

It's the same manner why we construct Z_1 like Fig 13. For the algebra on graph method, it's really convenient for us to calculate all the values of R, L and C. All we need to do is figure out all the corner frequency. After that, we can get the equations for R, L and C directly.

In this example, for our desired crossover frequency $\omega_c = 300Krad/s$, read the magnitude and phase from bode diagram, we can obtain:

$$\| G_{vd} \| = 19.9dB = 10 \quad (3.29)$$

$$\angle G_{vd} = -186^\circ \quad (3.30)$$

Our desired design is to improve the phase margin 60° at crossover frequency. In other words, make sure we have 54° phase margin at crossover frequency. Now just using the equations:

$$\omega_z = \omega_c \sqrt{\frac{1 - \sin\theta}{1 + \sin\theta}} \quad (3.31)$$

$$\omega_{p1} = \omega_c \sqrt{\frac{1 + \sin\theta}{1 - \sin\theta}} \quad (3.32)$$

$$G_{c0} = \sqrt{\frac{\omega_z}{\omega_{p1}}} \quad (3.33)$$

G_{c0} is the gain to make sure this PD part won't change the magnitude of the original system but just improve the phase margin. For we already have:

$$H(s) = \frac{1}{5} \quad (3.34)$$

$$PWM(s) = \frac{1}{V_m} = \frac{1}{2} \quad (3.35)$$

$$V_{ref} = 1V \quad (3.36)$$

At crossover frequency, our loop gain is already 1, so just put $G_{c0} = \sqrt{\frac{\omega_z}{\omega_{p1}}}$ to keep the magnitude unchanged. Since we Also want to improve the low frequency gain as much as possible but also don't want the inverted zero at ω_L change our phase margin at ω_c , so we just

let $\omega_L = \frac{1}{10}\omega_c = 30Krad/s$. Same thing for $\omega_{p2} = 10\omega_c = 3Mrad/s$. Now we can get all the values for R,L and C in our compensator:

$$\omega_z = 300 * 0.26Krad/s = 80.4Krad/s = \frac{1}{R_1 C_1} \quad (3.37)$$

$$\omega_{p1} = 300 * 3.73Krad/s = 1.12Mrad/s = \frac{1}{C_1 R_3} \quad (3.38)$$

$$G_{c0} = \sqrt{\frac{\omega_z}{\omega_{p1}}} = 0.27 = \frac{R_2}{R_1} \quad (3.39)$$

$$\omega_L = 30Krad/s = \frac{1}{R_2 C_2} \quad (3.40)$$

$$\omega_{p2} = 3Mrad/s = \frac{1}{R_2 C_4} \quad (3.41)$$

Since we have more unknowns than equations, we just let $R_2 = 100K\Omega$, then we can get:

$$C_2 = 3.33 * 10^{-10}F \quad (3.42)$$

$$R_1 = 370K\Omega \quad (3.43)$$

$$C_1 = 3.36 * 10^{-11}F \quad (3.44)$$

$$R_3 = 26.6K\Omega \quad (3.45)$$

$$C_4 = 3.33 * 10^{-12}F \quad (3.46)$$

3.7 Combination of H(s) and compensator component R_3

Since we have R_3 as part of Z_1 , also, voltage divisor is just made of resistors. It's nice if we can combine these resistors together like Fig 14:

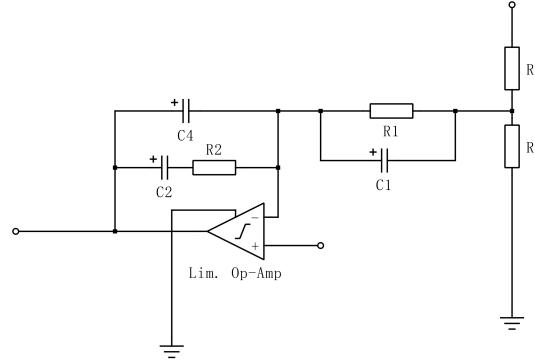


Figure 14: Combined voltage divisor and compensator

To combine all these resistors together R_x and R_y should satisfy:

$$R_x \parallel R_y = 26.6K\Omega \quad (3.47)$$

$$\frac{R_y}{R_x + R_y} = H(s) = \frac{1}{5} \quad (3.48)$$

From which, we can obtain the value of R_x and R_y . Now we have finished all the compensatory design part.

$$R_x = 1.33 * 10^5 \Omega \quad (3.49)$$

$$R_y = 3.33 * 10^4 \Omega \quad (3.50)$$

4 Input filter design

In this section, we will first design an undamped LC input filter (Because of the resonance, this filter will influence the transfer function of the system), then damp it.

4.1 Undamped input filter design

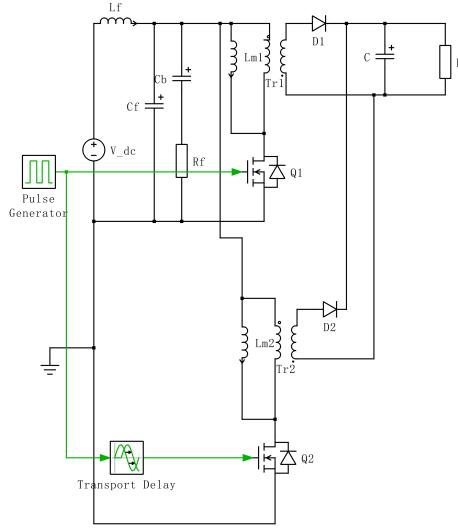


Figure 15: Input filter

Fig 15 shows the configuration of input filter. If we don't consider R_f and C_b right now, we can get:

$$i_{Cf} = i_{Lf} - i_{Lm} \dots \text{for } 0 \sim DTs \quad (4.1)$$

$$i_{Cf} = i_{Lf} \dots \text{for } DTs \sim 0.5Ts \quad (4.2)$$

If we want the ripple $\Delta V_{Cf} = 0.5V$ and $\frac{\Delta i_{Lf}}{I_{Lf}} = 5\%$, then we can obtain:

$$2\Delta v_{Cf} = \frac{\Delta Q}{C} = \frac{I_g * (0.5 - D)Ts}{C} \quad (4.3)$$

$$2\Delta i_{Lf} = \frac{\frac{1}{2} * \frac{0.5Ts}{2} * 0.5}{L} \quad (4.4)$$

Plug in all the DC terms, we can obtain:

$$L_f = 2.5 * 10^{-6} H \quad (4.5)$$

$$C_f = 10^{-7} F \quad (4.6)$$

4.2 Damping the input filter

Now for the LC filter, $R_{of} = \sqrt{\frac{L}{C}} = 0.5\Omega$, [2], using the optimum damping described by:

$$\| Z_o \|_{mm} = R_{of} \frac{\sqrt{2(2+n)}}{n} \quad (4.7)$$

$$Q_{opt} = \frac{R_f}{R_{of}} = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \quad (4.8)$$

Let $\| Z_o \|_{mm} = 10\Omega$, we can obtain:

$$n = 1.28 \quad (4.9)$$

$$C_b = 1.28 * 10^{-7} F \quad (4.10)$$

$$R_f = 6.1\Omega \quad (4.11)$$

4.3 Confirm the input filter design by Middlebrook's extra element theorem

Fig 5 show the small signal equivalent circuit, now we can use it again to confirm our input filter design. Middlebrook's extra element theorem is employed to determine how addition of the input filter modifies the control-to-output transfer function:

$$G_{vd}(s) = G_{vd}(s) |_{Z_o(s)=0} \frac{1 + \frac{Z_o(s)}{Z_N(s)}}{1 + \frac{Z_o(s)}{Z_D(s)}} \quad (4.12)$$

$Z_D(s)$ is equal to the converter input impedance when $\hat{d} = 0$. $Z_N(s) = \frac{v_{test}(s)}{i_{test}(s)}$, when $i_{test}(s)$ and $v_{test}(s)$ are adjusted such that the output is a null element.

If the the output impedance of the input filter is much smaller than the magnitude of $Z_D(s)$ and $Z_N(s)$,we can say that the input filter does not substantially alter the control-to-output transfer function .

So let's first figure out the $Z_D(s)$ and $Z_N(s)$. When we short circuit all the \hat{d} terms, we can obtain $Z_D(s)$. For $Z_N(s)$, we should first derive appropriate $i_{test}(s)$ and $v_{test}(s)$.

$$Z_D(s) = \frac{L}{2D^2} + \frac{(D'n)^2}{D^2} \left(\frac{1}{sC} \| R \right) \quad (4.13)$$

$$Z_N(s) = \frac{v_{test}(s)}{i_{test}(s)} = \frac{\frac{1}{D}[(sL\frac{2\hat{d}I}{D'}) - \hat{d}(V_g + nV)]}{2\hat{d}I + \frac{2\hat{d}ID}{D'}} \quad (4.14)$$

After all the calculations, we can obtain:

$$Z_D(s) = 200 \frac{1 + 5 * 10^{-6}s + 3.33 * 10^{-11}s^2}{1 + 6.66 * 10^{-6}s} \quad (4.15)$$

$$Z_N(s) = -200(1 - 4 * 10^{-6}s) \quad (4.16)$$

Since $\| Z_o \|_{mm} = 10\Omega$ is the maximum value of the output impedance of our input filter, if the magnitude of $Z_D(s)$ and $Z_N(s)$ are much greater than 10Ω , our input filter is well designed.

We draw the magnitude plot of $Z_D(s)$ and $Z_N(s)$ in Fig 16. This time we use linear scale and use absolute values. It clearly shows that $Z_D(s)$ and $Z_N(s)$ satisfy the impedance inequalities(The minimum value of $Z_D(s)$ and $Z_N(s)$ is over 10 times greater than 10Ω , which is the maximum value of our input filter impedance.).

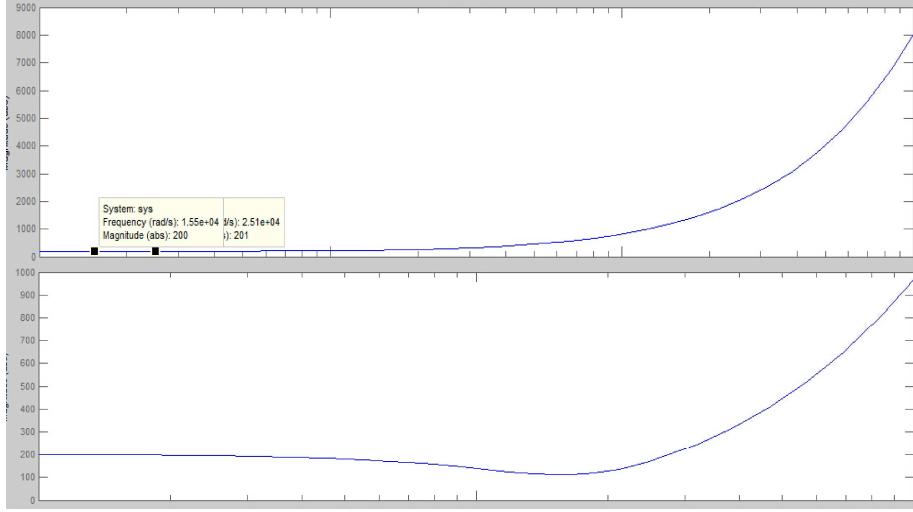


Figure 16: The magnitude of $Z_D(s)$ and $Z_N(s)$

4.4 Confirm the input filter design by PLECS

After we plug in the input filter, we can use the PLECS to do the analysis again to make sure our system's transfer function G_{vd} doesn't change significantly. Fig 17 shows the bode plot of the new G_{vd} transfer function for this system.

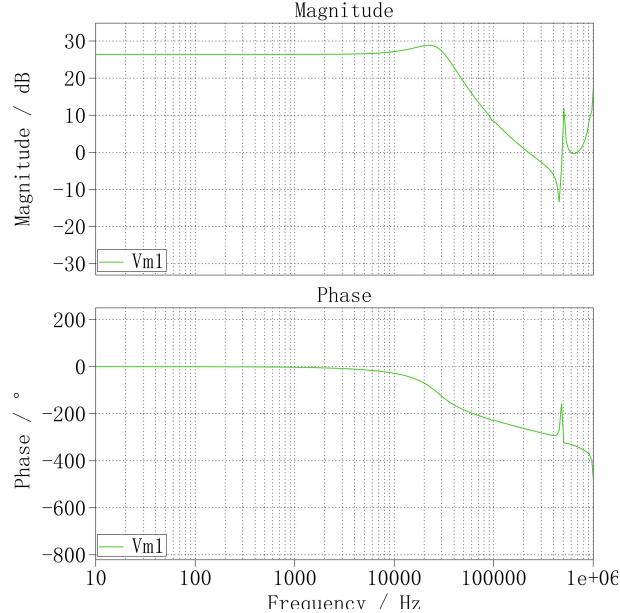


Figure 17: G_{vd} transfer function with input filter

5 Simulation in PLECS

5.1 Analog controller

We made our simulation for both ideal case and nonideal case. For nonideal case, we add $R_L = 0.2\Omega$, $R_{on} = 0.2\Omega$, $V_D = 0.4V$. We monitor 4 variables, which are i_g , v_{out} , i_{Lm1} , i_{Lm2} . Here are the simulation results for both transient response and steady state response.

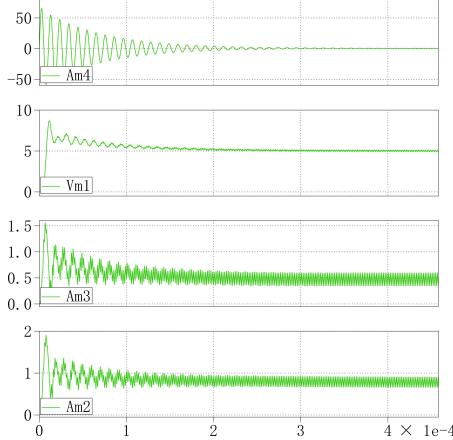


Figure 18: Transient response for ideal case

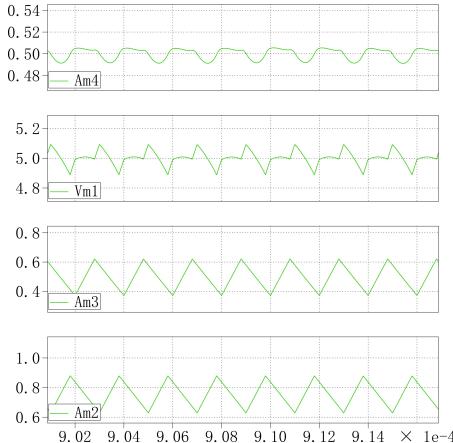


Figure 19: Steady state response for ideal case

Fig 18 ~ to Fig 21 shows the transient and steady state response of the converter. We can see the steady state value of V_{out} is always $5V$, which is exactly our desired output.

5.2 An improvement for both transient and steady state response

The previous figures show that our system is acceptable, for not very large overshoot and precise output voltage. There's a problem that the two phase inductor don't share the same current. This is because when we apply a step input reference, at the very beginning, the duty ratio is pretty large. When the first MOSFET starts conducting, the voltage across the input filter capacitor is relative small, but when it turns to the second MOSFET conducting, V becomes larger. Before the steady state, there's always more voltage apply to L_{M2} , which cause the difference of the current.

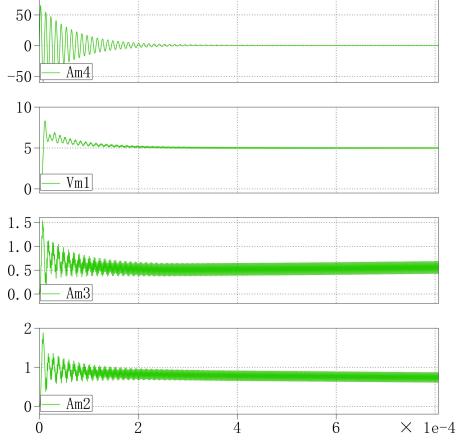


Figure 20: Transient response for nonideal case

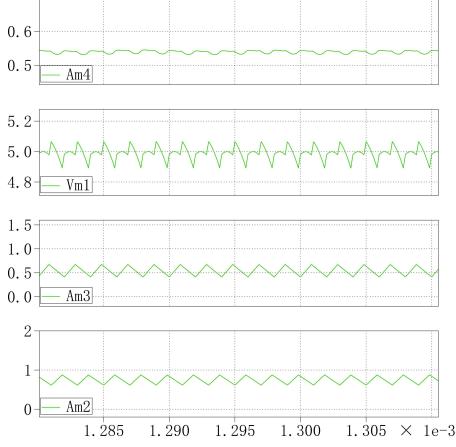


Figure 21: Steady state response for nonideal case

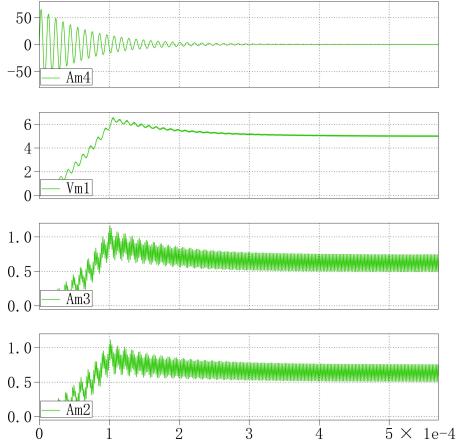


Figure 22: Transient response for soft start-up

When we try to start the converter softly, that is, to apply a ramp reference rather than a step reference, things become different. Because at the very beginning, the error signal is relatively small, which will cause a slow change of input voltage, then we can realize the same current in both two inductor. Also, the same current is helpful to our output voltage ripple.

Fig 22 show the simulated result for transient response.

5.3 Digital controller

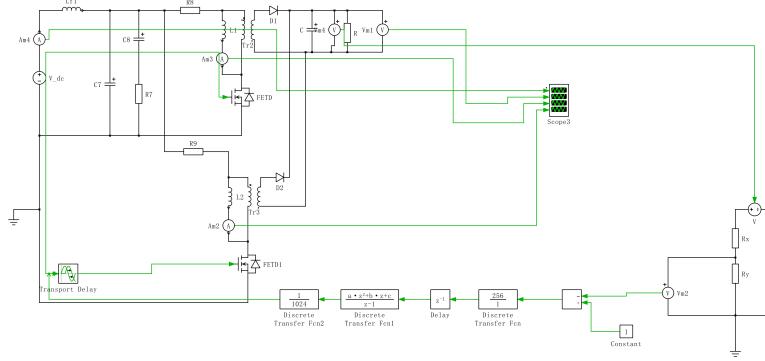


Figure 23: Digital control schematic

Fig 23 shows the schematic for digital controller.

6 Digital design

6.1 Minimal resolutions of ADC and DPWM

[3] A/D converter has to enable error lower than the allowed variation of the output voltage Δv_o :

$$\frac{\Delta v_o}{V_o} H > \frac{V_{maxA/D}}{2^{nA/D} V_o} \quad (6.1)$$

Let $V_{ref} = 1V$, we can obtain $n_{A/D} = 8$. Also, for flyback converter, The minimum resolution of DPWM should be:

$$n_{DPWM} = int[\log_2(\frac{1}{1-D}(\frac{V_{ref}}{DV_{maxA/D}} 2^{nA/D} + 1))] \quad (6.2)$$

Hence, we can obtain $n_{DPWM} = 10$. These are the steady state case, for dynamic condition, let's confirm:

$$\Delta V_{Q_{ADC}} > \frac{4}{\pi} \| G_{vd}(j\omega_{LC}) \| \Delta V_{DPWM} \quad (6.3)$$

Our design satisfy all the steady state conditions and dynamic condition.

6.2 Digital PID compensator design

For the ADC and DPWM we choosed, we can obtain:

$$K_{DPWM} = \frac{1}{2^{10}} \quad (6.4)$$

$$K_{ADC} = 2^8 \quad (6.5)$$

We can obtain the controlled plant of a digitally controlled switching regulator:

$$G_{ed}(j\omega) = K_{DPWM}e^{-j\omega DT_s} K_{ADC}e^{-j\omega T_{A/D}} G_{vd}(j\omega) H(j\omega) \quad (6.6)$$

Then we can design our compensator using discrete control law.

References

- [1] Brian Shaffer, "Interleaving Contributes Unique Benefits to Forward and Flyback Converters "
- [2] Robert W. Erickson, Dragan Maksimovi, "Fundamentals of power electronics "
- [3] Aleksandar Prodic, Dragan Maksimovic and Robert W.Erickson "Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter"