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ank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18 in	Notes (1), (2), (
lumber	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
1	VREFB1N0	VCCD_PLL3		-	1	F5	F6	J9									
1		GNDA3			0	E5	F5	H9		-							
1		VCCA3			2	E4	G6	Л9 J8		-							
1		IO	DIFFIO_L1p		3	B2	G4	D3		DQ1L	DQ1L						
1		10	DIFFIO_L1p			B1	G3	C2		DQTL	DQIL				DQ2L	DQ1L	DQ1L
1	VREFB1N0		DII I IO_EIII		4	ы	65	02							DQZL	DQTL	DQTL
<u>'                                     </u>		GND			5												+
1	VREFB1N0				J			M9									+
1	VREFB1N0		DIFFIO L2p			1	B2	D2				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
<u>.</u> 1	VREFB1N0		DIFFIO L2n			1	B1	D1				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
<u>.                                      </u>	VREFB1N0		VREFB1N0		6	C2	G5	H7					DQIL	54.2	DQLL	DQIL	
1			DIFFIO_L3p		Ü	02	00	E5									+
 I		IO	DIFFIO_L3n			C1		E4		DQ1L	DQ1L						+
			DIFFIO_L4p	nRESET		C3	E4	G6		54.2	54.2	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
<u> </u>		IO	DIFFIO L4n	THE CE T			E3	G5				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
		IO	DIFFIO_L5p					H4					DQIL	54.2	DQLL	DQIL	
	VREFB1N0		DIFFIO_L5n	+				H3	1	<del> </del>	<del> </del>	1	1	<del> </del>		1	+
		10	DIFFIO L6p	+				J5	1	<del> </del>	<del> </del>	1	1	<del> </del>		1	+
	VREFB1N0		5.1 1 10_L0p	+	7	1	<del>                                     </del>	30	<del> </del>	t	<b>†</b>	<b>†</b>	+	<b>†</b>	<b>†</b>		+
		10	DIFFIO_L6n	+	<u> </u>		<b>†</b>	G7	<b>†</b>	<b>—</b>	<b>-</b>	<b>†</b>	-	<b>-</b>	1		+
	VREFB1N0		Dil 110_LUII	+	8		<del>                                     </del>	31	<b>†</b>	<b>†</b>	<b> </b>	<del> </del>		<b> </b>	<b>†</b>		+
	VINELDIINU	JIND	1	+	U	1	<del>                                     </del>	1	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,
	VREFB1N1	10	DIFFIO L7p		9	D3	C2	E3	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0
<u> </u>	VREFB1N1	VCCINT	5o_e.p		10	50	02		OD: OLITO	OD! OLITO	OD: OE:10	ODI OLITO	OD! OLIKO	OD: OE:10	ODI OLINO	OB. OLIKO	OB. CERC
	VREFB1N1		DIFFIO_L7n		10	+	C1	F3				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
	VREFB1N1		DII I IO_E/II		11	+	CI	13			<u> </u>	DQZL	DQIL	DQIL	DQZL	DQTL	DQTL
	VREFB1N1	IO	DIFFIO_L8p		-	D2	D2	F5		DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
		10	DIFFIO_L8p	DATA1, ASDO	12	D1	D2 D1	F4		DQTL	DQIL	DQZL	DQIL	DQTL	DQZL	DQTL	DQTL
		10	VREFB1N1	DATAT, ASDO	13	F3	H7	L5									+
		10	DIFFIO L9p		13	гэ	H6	G4				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
		10	DIFFIO_L9p				J6	G3				DQ2L DQ2L	DQ1L DQ1L	DQ1L DQ1L	DQZL	DQTL	DQTL
		10	DIFFIO_L9II	FLASH nCE, nCSO	14	E2	E2	E2				DQZL	DQTL	DQIL			+
		10		FLASH_NCE, NCSO	14		E2 E1			2011	2011		2011	DO41			_
			DIFFIO_L10n		-	E1	E1	J6		DQ1L	DQ1L		DQ1L	DQ1L		2041	2041
		10	DIFFIO_L11p			-		E1		-	-			-		DQ1L	DQ1L
		10	DIFFIO_L11n			-		J7		-	-						
		10	DIFFIO_L12p			-	F2	F2		-	-	DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0
	VREFB1N1		DIFFIO_L12n			-	F1	F1		-	-	DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L
		IO	DIFFIO_L13p					K4									_
	VREFB1N1	10	DIFFIO_L13n			-		K3									
		IO	DIFFIO_L14p				H8	K7									_
		IO	DIFFIO_L14n		<u> </u>	1	J8	L6	ļ			ļ			ļ		4
		IO	DIFFIO_L15p		<u> </u>	1-		L8	ļ			ļ	ļ				
	VREFB1N2		DIFFIO_L15n		<u> </u>	1	ļ	L7	ļ	<b></b>	<b></b>	ļ		<b></b>			
	VREFB1N2		DIFFIO_L16p		<b></b>	1	ļ	M8	ļ			ļ			ļ		
		IO	DIFFIO_L16n		L		<b>.</b>	M7	ļ	<b></b>		ļ					
	VREFB1N2		ļ	1	15	1	<u> </u>	<u> </u>	ļ	ļ	ļ	ļ	ļ	ļ			4
	VREFB1N2	IO	DIFFIO_L17p	1	<u> </u>	1	<u> </u>	L4	ļ	ļ	ļ	ļ	ļ	ļ			4
	VREFB1N2				16	1											
	VREFB1N2		DIFFIO_L17n		<u> </u>			L3									
		Ю	DIFFIO_L18p					H6									
		Ю	DIFFIO_L18n				J5	H5	[								
	VREFB1N2		DIFFIO_L19p		1			J4									
		IO	DIFFIO_L19n					J3							DQ0L	DQ1L	DQ1L
	VREFB1N2			nSTATUS	17	G5	K6	M6									
	VREFB1N2		VREFB1N2		18	H6	H5	N8									
	VREFB1N2	VCCINT			19												
	VREFB1N2	IO	DIFFIO_L20p			G2	L8	G2		DQ1L	DQ1L				DQ0L	DQ1L	DQ1L
	VREFB1N2	GND	·		20												
	VREFB1N2	IO	DIFFIO_L20n			G1	K8	G1		DQ1L	DQ1L						T
	VREFB1N2	IO	DIFFIO L21p		1		J7	M3	İ			İ			İ		1
	VREFB1N2		DIFFIO_L21n			1	K7	K1	İ	İ	İ	İ	1	İ	DQ0L	DQ1L	DQ1L
	VREFB1N2		DIFFIO_L22p	1		1	<u> </u>	N4	1	1	1	1	1	1		1	1
	VREFB1N2		DIFFIO L22n		1	1	1	N3	1	<b>I</b>	<b>-</b>	1		<b>-</b>	1		+
	TANKET DITAL	10	5 / IO_LZZII	+		-		M4	<b>-</b>	<del>                                     </del>		<b>-</b>	+		1		



		L-1.															Notes (1), (2), (3
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780
									DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,
B1	VREFB1N3				21	H2	J4	K2	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0
B1	VREFB1N3		DIFFIO_L23p DIFFIO L23n				H2	L2				DQ0L DQ0L	DQ1L	DQ1L	DQ0L	DOM	DO41
B1	VREFB1N3 VREFB1N3	10 10	VREFB1N3		22	H1	H1 J3	L1 M5				DQUL	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L
B1	VREFB1N3	10	DIFFIO_L24p	1	22	п	J2	M2				DQ0L	DQ1L	DQ1L			
B1	VREFB1N3	10	DIFFIO L24n					M1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L
B1	VREFB1N3	10	DIFFIO L25p					P2				5402	54.2	Dair	5402	54.2	54.2
B1		10	DIFFIO_L25n					P1							DQ0L	DQ1L	DQ1L
B1	VREFB1N3			DCLK	23	H4	K2	P3									
B1	VREFB1N3	Ю		DATA0	24	H3	K1	N7									
B1	VREFB1N3			nCONFIG	25	H5	K5	P4									
B1	VREFB1N3	TDI		TDI	26	J6	L5	P7									
B1	VREFB1N3			TCK	27	J1	L2	P5									
B1	VREFB1N3	TMS		TMS	28			P8									
B1	VREFB1N3	TDO		TDO	29	J5		P6									
B1	VREFB1N3	nCE	DIFFOLIC -	nCE	30	K6		R8			-	1				1	1
B1	VREFB1N3		DIFFCLK_0p	1	31	F2	_	J2		-	<del>                                     </del>	1	1	1	ļ	-	-
B1	VREFB1N3 VREFB2N0	CLK1 CLK2	DIFFCLK_0n DIFFCLK 1p	1	32			J1	1	ļ	<del>                                     </del>	1	+	1	<del> </del>	<del> </del>	+
B2		CLK2 CLK3			33 34	N2		Y2 Y1			<b>_</b>				<b> </b>		+
B2 B2	VREFB2N0 VREFB2N0	IO	DIFFCLK_1n DIFFIO L26p		34	N1 K2	11 L6	R2		DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L
B2	VREFB2N0 VREFB2N0		DIFFIO_L26p		35	N2	LO	K2		DQTL	DQTL	DQUL	DQTL	DQTL	DQUL	DQTL	DQIL
B2			DIFFIO L26n		33	K1	M6	R1		DQ1L	DQ1L	DQ0L	DQ1L	DQ1L		DQ1L	DQ1L
B2	VREFB2N0		DII 110_L20II		36	KI	IVIO	IX I		DQTL	DQTL	DQUL	DQIL	DQIL		DQIL	DQIL
B2	VREFB2N0		DIFFIO_L27p		00		M2	U3				DQ0L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1
B2	VREFB2N0		DIFFIO L27n					U2				2402	DQ1L	DQ1L	DINIOL	Dimite i/Bironite	Dill'I E I/ B I I G I I E I
B2	VREFB2N0		DIFFIO L28p		37			R3	DQ1L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1	DQ1L	DQ3L	DQ1L
B2	VREFB2N0	Ю	DIFFIO_L28n		38			R6	DQ1L	DM1L/BWS#1L	DM1L0/BWS#1L0	DQ1L	DQ3L	DQ1L			
B2	VREFB2N0	Ю	DIFFIO_L29p					R4				DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L
B2	VREFB2N0	Ю	DIFFIO_L29n				N1	R7				DQ1L	DQ3L	DQ1L			
B2	VREFB2N0	Ю	DIFFIO_L30p					T4							DQ1L	DQ3L	DQ1L
B2	VREFB2N0	Ю	DIFFIO_L30n				L7	T3									
B2	VREFB2N0	Ю	VREFB2N0		39	L6		T8									
B2	VREFB2N0	Ю	DIFFIO_L31p					U4									
B2			DIFFIO_L31n					R5							DQ1L	DQ3L	DQ1L
B2	VREFB2N0				40												
B2	VREFB2N0		DIFFIO_L32p		41	L2	P2	U1	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L
B2	VREFB2N0				42												
B2	VREFB2N0	10	DIFFIO_L32n		1		P1 R2	V4		DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L
B2 D0	VREFB2N0 VREFB2N0	.0	DIFFIO_L33p DIFFIO_L33n	+	43			V3 V2	DQ1L	DQ3L DQ3L	DQ1L DQ1L	DQ1L DQ1L	DQ3L DQ3L	DQ1L DQ1L	DQ1L	DQ3L	DQ1L
B2	VREFB2N0 VREFB2N1		DIFFIO_L33N		43	L3		V2 V9	DQTL	DQ3L	DQIL	DQ1L DQ1L	DQ3L DQ3L	DQ1L	DQTL	DQ3L	DQTL
B2			DIFFIO_L34p		44	M2	P4	AB2	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1
B2	VREFB2N1	Ю	DIFFIO_L34n		45	M1	P3	AB1	DQ1L			DQ1L	DQ3L	DQ1L			
B2	VREFB2N1							V1							DQ1L	DQ3L	DQ1L
B2	VREFB2N1	Ю	DIFFIO_L35p				U2	W2				DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	DQ1L	DQ3L	DQ1L
B2		Ю	DIFFIO_L35n				U1	W1				DQ3L	DQ3L	DQ1L	DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2
B2	VREFB2N1		DIFFIO_L36p	<u> </u>	1	<u> </u>		W3			<b></b>				ļ		1
B2	VREFB2N1		DIFFIO_L36n					W4									
B2	VREFB2N1		DIFFIO_L37p			<u> </u>		V6			-	1				1	1
B2	VREFB2N1	10	DIFFIO_L37n	1		<u> </u>		U5	ļ	1	-	DOOL	DON	2011		1	1
D2	VREFB2N1 VREFB2N1	10	DIFFIO_L38p DIFFIO_L38n		-	1		Y5 Y6			<b>-</b>	DQ3L DQ3L	DQ3L DQ3L	DQ1L DQ1L	<b> </b>	1	+
B2 B2		10	DIFFIO_L38n DIFFIO_L39p	1		-		Y6 V5	-		-	DQ3L	DUJL	DQTL	<b>+</b>	<b> </b>	+
B2		10	DIFFIO_L39p DIFFIO_L39n		1	1	-	V5 U6			1				DQ3L	DQ3L	DQ1L
B2	VREFB2N1 VREFB2N1	10	DIFFIO_L39n DIFFIO_L40p		1	1	-	AA7			1				DUSL	DW3F	DQTL
B2	VREFB2N1 VREFB2N1		DIFFIO_L40p DIFFIO L40n	1	1	1		AA6			<b>+</b>	+	<b>-</b>	<b>-</b>	+	1	+
B2	VREFB2N1	10	VREFB2N1	+	46	M3	P5	T7		<del> </del>	<del>                                     </del>	<del> </del>			<u> </u>	<u> </u>	+
B2		10	DIFFIO_L41p	†	40	IVIU		AA8	1	<del> </del>	<del>                                     </del>	DQ3L	DQ3L	DQ1L	<b>†</b>	<del> </del>	+
B2	VREFB2N1		DIFFIO_L41p		1	<del>                                     </del>		Y7	1		<b>-</b>	- QUL		- WIL	<b>†</b>	1	+
B2	VREFB2N1		5.1 1 IO_L41II		47	<del>                                     </del>		l'	1		<b>-</b>		<b>+</b>	+	<b>†</b>	1	+
		10	DIFFIO L42p	+	+	+	M8	Y4	+	<b></b>		+	+	<b>+</b>	DQ3L	DQ3L	DQ1L



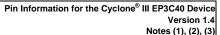
Bank	VREFB	Pin Name /	Optional	Configuration	Q240	E324	E494 /	F780	DOS for Y8/Y0 in	DOS for Y9/Y9 in	DOS for V16/V19 in	DOS for Y9/Y0 in	DQS for X16/X18 in	DOS for Y22/Y26 in	DOS for Y9/Y9 in	DOS for Y16/Y19 in	Notes (1), (2), (3
bank Number	Group	Function	Function(s)	Function	Q240	F324	U484	F/8U	Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
											1						
32	VREFB2N1	GND			48												
32	VREFB2N2		DIFFIO_L42n				N8	Y3									
32	VREFB2N2	Ю	DIFFIO_L43p					T9									
32	VREFB2N2	Ю	DIFFIO_L43n					AC2							DQ3L	DQ3L	DQ1L
32	VREFB2N2	Ю	DIFFIO_L44p		49	P2	W2	W8	DQ1L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L			
32	VREFB2N2		DIFFIO_L44n			P1	W1	AC1		DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L
B2	VREFB2N2	IO	DIFFIO_L45p			R2	Y2	V7		DQ3L	DQ1L	DQ3L	DQ3L	DQ1L			
B2	VREFB2N2		DIFFIO_L45n				Y1	AC3				DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L
B2	VREFB2N2	IO	DIFFIO_L46p		1			AD2							DQ3L	DQ3L	DQ1L
B2	VREFB2N2	10	DIFFIO_L46n		1			AD1									
B2	VREFB2N2	10	DIFFIO_L47p		1		-	AB3							DQ3L	DQ3L	DQ1L
B2	VREFB2N2	10	DIFFIO_L47n		1			AA4 W9	-	-					DQ3L	DQ3L	DQ1L
B2 D0	VREFB2N2 VREFB2N2		DIFFIO_L48p	+				AB7		-							
B2 B2	VREFB2N2 VREFB2N2	10	DIFFIO_L48p DIFFIO L48n		1			AC7									
B2	VREFB2N2	10	VREFB2N2		50	R1	T3	V8									
B2	VREFB2N2	10	DIFFIO_L49p		30	IXI	N7	AE1									
B2	VREFB2N2		DIFFIO_L49p	1	1		P7	AE2	1	1	1		1		DQ3L	DQ3L	DQ1L
B2	VREFB2N2	IO	DIFFIO L50p	1	1		AA2	AA5	1	1	1		1				
B2	VREFB2N2	Ю	DIFFIO_L50n	İ			AA1	AF2	1	1	1	DQ3L	DQ3L	DQ1L	DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3
B2	VREFB2N3	IO	DIFFIO_L51p					AB6				-					
B2	VREFB2N3		DIFFIO_L51n					AB5									
B2	VREFB2N3	IO						AA3									
B2	VREFB2N3	Ю	RUP1		51	T2	V4	U7	DQ1L								
B2	VREFB2N3	Ю	RDN1		52	T1	V3	U8	DQ1L								
B2	VREFB2N3	IO	DIFFIO_L52p			T3	P6	AC4		DQ3L	DQ1L						
B2	VREFB2N3	VCCINT			53												
B2	VREFB2N3	Ю	DIFFIO_L52n			R3		AD3		DQ3L	DQ1L						
B2	VREFB2N3				54												
B2	VREFB2N3	Ю					T5	AD4				DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3			
							L.		DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,
B2	VREFB2N3				55	M5	T4	AE3	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1
B2		10	VREFB2N3		56 57	R5	R5	AB4	2011	DAMOU /DVA/O //OI	D141 4 (D)410 ((4) 4						
B2 B2	VREFB2N3 VREFB2N3	10	DIFFIO L53p		57	R4	R6 R7	AB8 AC5	DQ1L	DM3L/BWS#3L	DM1L1/BWS#1L1						
	VREFB2N3 VREFB2N3		DIFFIO_L53p DIFFIO_L53n	+			T7	AD5		-							
B2 B2	VREFB2N3 VREFB2N3	10	DIFFIO_L53h DIFFIO_L54p		1		17	AE4									
B2	VREFB2N3	10	DIFFIO_L54n					AF3									
B2	VREFB2N3	VCCA1	DII 1 IO_LU4II		58	N5	T6	Y8									
B2	VREFB2N3	GNDA1			59	P5	U5	AA9									
B2	VREFB2N3	VCCD_PLL1			60	P4	U6	Y9									
B3	VREFB3N3	VCCINT			61												
B3	VREFB3N3		DIFFIO B1p			U1	V6	AC11									
B3	VREFB3N3	GND			62												
B3	VREFB3N3	IO	DIFFIO_B1n			V1	V5	AD11				DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3			
B3	VREFB3N3	IO	DIFFIO_B2p					AD12									
B3	VREFB3N3	Ю	DIFFIO_B2n					AE6							DM1B		
B3	VREFB3N3	Ю	DIFFIO_B3p				U7	AF4							DQ1B		
B3	VREFB3N3	Ю	DIFFIO_B3n				U8	AB12	ļ	ļ	ļ		ļ			ļ	
B3	VREFB3N3	Ю	VREFB3N3	ļ	63	T4	Y4	Y10	ļ	ļ	ļ	1	ļ			ļ	1
B3	VREFB3N3	IO	DIFFIO_B4p				Y3	AG4				DQ3B	DQ3B	DQ5B			1
B3	VREFB3N3	VCCINT			64		<b> </b>										
B3	VREFB3N3	10	DIFFIO_B4n	+	05		<b> </b>	AG3	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>		<del>                                     </del>		DQ1B	<del>                                     </del>	
B3	VREFB3N3	GND	DIEEIO DE-	1	65	-	1	A E 7	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	1	<del>                                     </del>	1	ļ	<del>                                     </del>	1
B3	VREFB3N3		DIFFIO_B5p	1	cc		-	AE7	<b>-</b>	<b>-</b>	-	-	-		<b> </b>	-	+
B3	VREFB3N3	VCCIO3	DIEEIO DE-	-	66		<u> </u>	450	<b>-</b>	<b>-</b>	<b>_</b>	-	<b>_</b>		<b> </b>	<b>_</b>	+
B3 B3	VREFB3N3 VREFB3N3	.0	DIFFIO_B5n	1	67	<del>                                     </del>	<b>-</b>	AE8	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	-	-		1	-	+
DJ	VKEFB3N3	GIND		1	0/	<del>                                     </del>	<b>-</b>		DQS1B/CQ1B#,	DQS1B/CQ1B#,	DOS1B/CO1B#	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,
В3	VREFB3N3	10	DIFFIO_B6p		68	P6	Y6	AD7	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2
B3			DIFFIO_B6n	1	30			Y12							1		
B3	VREFB3N2	Ю	PLL1_CLKOUTp	İ	69	U2	AA3	AE5	1	1	1		1	İ	1	1	
B3	VREFB3N2	IO	PLL1_CLKOUTn	İ	70	V2	AB3	AF5	1	1	1		1	İ	1	1	
B3	VREFB3N2	IO	DIFFIO B7p				W6	AH3				DQ3B	DQ3B	DQ5B	DQ1B		



Bank	VREFB	Pin Name /	Optional	Configuration	Q240	E224	F484 /	F780	DOS for Y8/Y0 in	DOS for Y9/Y9 in	DOS for Y16/Y18 in	DOS for V9/V9 in	DOS for V16/V18 in	DOS for Y22/Y26 in	DOS for Y9/Y0 in	DQS for X16/X18 in	Notes (1), (2), (3
Number	Group	Function	Function(s)	Function	Q240	F324	U484	F/80	Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
· · · · · · · · · · · · · · · · · · ·	Group	i unction	i unction(s)	T dilotion			0404		42-0	1 024	1 324	1 404/0404	1 404/0404	1 404/0404	1700	1700	1700
D0	VDEEDONO	VOCINIT			71				-	-	-						
B3	VREFB3N2	VCCINT	DIFFIO D7		/1	-	V7	14/40									
B3	VREFB3N2 VREFB3N2	GND	DIFFIO_B7n		72		V/	W10									
B3	VREFB3N2	IO			12	1	AA4	AF6		-		DQ3B	DQ3B	DOEB	DQ1B		
B3	VREFB3N2	10	VREFB3N2		73	T6	AB4	AA12				DQ3B	DQ3B	DQ5B	DQIB		
B3	VREFB3N2	IO	DIFFIO B8p		73	16	AA5	AC12		-		DQ3B	DQ3B	DQ5B			
B3	VREFB3N2	10	DIFFIO_B8p		1	1	AB5	AH4				DQ3B	DQ3B	DQSB	DQ1B		
B3	VREFB3N2	10	DIFFIO_B8II DIFFIO_B9p		1	1	ADS	AC10							DQIB		
B3	VREFB3N2	10	DIFFIO B9n	1	<b>-</b>			AD8							DQ1B		
B3	VREFB3N2	10	DIFFIO_B9II		1	1		AG6							DQ1B		
B3	VREFB3N2	10	DIFFIO B10n	1	<b>-</b>			AB13							DQID		
B3	VREFB3N2	IO	DIFFIO_B11p	1	<b>-</b>		T8	AH6							DQ1B		
B3	VREFB3N2	IO	DIFFIO_B11n	1	<b>-</b>		T9	AA13							DQID		
B3	VREFB3N2	IO	DIFFIO_B12p		1	1	W7	AB9				DQ3B	DQ3B	DQ5B	DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3
B3	VREFB3N2	VCCINT	Біі Гіо_Бігр	1	74		VV /	VD9				DQJD	DQ3B	DQJB	DIVISD/DVVS#3D	DIVIDE I/BVVO#3B1	DIVIDBO/DVVO#3D3
B3	VREFB3N2	IO	DIFFIO_B12n		, -	1	Y7	AD10				DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	GND	DII 1 10_D12II		75	1		ADTO				DQOD	DQOD	DQOD	DQOD	DQOD	DQOD
B3	VREFB3N2	IO	DIFFIO B13p	1	1.		U9	AG7	<del> </del>	<del> </del>	<del> </del>	DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B13n	-	<b>-</b>		V8	Y13				DQ3B DQ3B	DQ3B	DQ5B	DQSB	DQ3B	DQSB
B3	VREFB3N2	10	Dii 110_D13i1	+	<del>                                     </del>		W8	AH7	<b>†</b>	<b>†</b>	<b> </b>	DQ3B DQ3B	DQ3B DQ3B	DQ5B DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO B14p		1	1	AA7	AC8				DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2	DQ3B	DQ3B DQ3B	DQ5B
B3	VREFB3N1 VREFB3N1	IO	DIFFIO_B14p DIFFIO B14n	+	1		AB7	AA10	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	DM5B/BWS#5B DQ5B	DQ3B	DQ5B	DQ3B DQ3B	DQ3B DQ3B	DQ5B DQ5B
		10	DIFFIO_B14II		1	-		Y14					DQ3B DQ3B		DQSB	DQ3B	DQSB
B3	VREFB3N1	IO	DIEEIO DAG-		-		Y8					DQ5B	DQ3B	DQ5B	DOOD	DOOD	DOED
B3	VREFB3N1		DIFFIO_B15p		<del>                                     </del>	-	T10	AG8							DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B15n		<u> </u>		T11	Y15									
B3	VREFB3N1	IO	VREFB3N1		76	P7	V9	AB11									
B3	VREFB3N1	VCCIO3			77	1											
									DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,
B3	VREFB3N1	IO	DIFFIO_B16p		78	U3	V10	AE10	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2
B3	VREFB3N1				79	1											
B3	VREFB3N1	10	DIFFIO_B16n			V3		AH8		DM3B/BWS#3B	DM5B1/BWS#5B1				DQ3B	DQ3B	DQ5B
B3	VREFB3N1	Ю	DIFFIO_B17p			U4		AF7		DQ3B	DQ5B				DQ3B	DQ3B	DQ5B
B3	VREFB3N1	Ю	DIFFIO_B17n		80	V4	U10	AH10	DM5B/BWS#5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	10	DIFFIO_B18p		81	U5	AA8	AF9	DQ5B			DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	10	DIFFIO_B18n		82	V5	AB8	AH12	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B19p					AF8							DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2
B3	VREFB3N1	Ю	DIFFIO_B19n					AF12									
B3	VREFB3N1	IO	DIFFIO_B20p					AE9							DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B20n					AF13									
B3	VREFB3N1	Ю	DIFFIO_B21p			R8	AA9	AF10		DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
В3	VREFB3N1	10	DIFFIO B21n		83	Т8	AB9	AF11	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3
B3	VREFB3N0	Ю	VREFB3N0		84	P8	U11	AA14									
B3	VREFB3N0	IO	DIFFIO B22p					AG10							DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO B22n		1			AE12							DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO B23p	1	1			AE11	<del> </del>	<del> </del>	<del> </del>				DQ5B	DQ3B	DQ5B
B3		VCCINT		1	85				<u> </u>	t	<u> </u>						
B3	VREFB3N0	IO	DIFFIO B23n		00	P9		AG11		DQ3B	DQ5B				DQ5B	DQ3B	DQ5B
B3	VREFB3N0		5 1 IO_D20II	1	86		1	,,,,,,,,,		2 400	2400				2430	2400	2 400
B3	VREFB3N0		DIFFIO_B24p	1	00	U6		AH11		DQ3B	DQ5B				DQ5B	DQ3B	DQ5B
B3	VREFB3N0	10	DIFFIO_B24p	+	<del>                                     </del>	V6		AB14	<b>†</b>	DQ3B	DQ5B DQ5B				DAND	D-40D	DOUB
D3	VREFB3N0	IO	DIFFIO_B24II	+	1	VO		AE13		DQ3B	DQSB				DQ5B	DQ3B	DQ5B
B3	VREFB3N0 VREFB3N0	10	DIFFIO_B25p DIFFIO_B25n	+	1	1	V11	AC14	1	1	<del> </del>	DOER	DQ3B	DOEB	DGOD	DWOD	PASD
D3	VREFB3N0 VREFB3N0	IO	DIFFIO_B25n DIFFIO B26p	+	1	U7	W10	AG12	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	DQ5B DQ5B	DQ3B DQ3B	DQ5B DQ5B	DQ5B	DQ3B	DQ5B
B3				+	-					DOOD	DOED				DQ5B	DQ3B	DQ5B
B3	VREFB3N0	10	DIFFIO_B26n	1	0.7	V7	Y10	AD14	DOED	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	-		<del> </del>
B3	VREFB3N0	10	DIFFIO_B27p	+	87	U8	AA10	AE14		DQ3B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1			<b>!</b>
B3	VREFB3N0	IO	DIFFIO_B27n	1	88	V8	AB10	AF14	DQ5B	DM5B/BWS#5B	DM5B0/BWS#5B0		DQ5B	DQ5B	1		1
B3	VREFB3N0	CLK15	DIFFCLK_6p		89	U9	AA11	AG14									
B3	VREFB3N0	CLK14	DIFFCLK_6n		90	V9	AB11	AH14	<b></b>	<b></b>	L						
B4	VREFB4N3	CLK13	DIFFCLK_7p	1	91	U10	AA12	AG15									
B4	VREFB4N3	CLK12	DIFFCLK_7n		92	V10	AB12	AH15									ļ
B4	VREFB4N3	IO	DIFFIO_B28p		93	U11	AA13	AB15		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B			
B4	VREFB4N3	IO	DIFFIO_B28n		94	V11	AB13	AC15	DQ5B			DQ4B	DQ5B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1
	VREFB4N3	IO	DIFFIO_B29p	_		U12	AA14	AD15	I -	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B			1

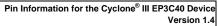


Bank	VREFB	Pin Name /	Optional	Configuration	0240	F324	F484 /	F780	DOS for Y8/Y9 in	DOS for Y8/Y9 in	DOS for ¥16/¥18 in	DOS for Y8/Y9 in	DQS for X16/X18 in	DOS for ¥32/¥36 in	DOS for Y8/Y9 in	DOS for ¥16/¥18 in	Notes (1), (2), (
Number	Group	Function	Function(s)	Function	Q240	F324	U484	F760	Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
	o.oup		(0)	· unotion			0.0.		42.0	. 021	. 02.	. 10 1/0 10 1					
1	VREFB4N3	10	DIFFIO B29n				AB14	AE15	-			DQ4B	DQ5B	DQ5B	-	DQ5B	DQ5B
<del>1</del>		10	DIFFIO_B29II				AD 14	AA16				DQ4B	DQSB	DQSB		DQSB	DQSB
<del>1</del>	VREFB4N3	IO	VREFB4N3		95	V12	V12	AA15									+
1	VREFB4N3	10	DIFFIO_B30p		33	V 12	VIZ	AF15							DQ4B	DQ5B	DQ5B
4	VREFB4N3	10	Біі і ю_взор		96			AI 13							DQ4D	DQJD	DQJB
4	VREFB4N3		DIFFIO_B30n		30			AG17							DQ4B	DQ5B	DQ5B
4		GND	DII I IO_D30II		97			AG17							DQ4D	DQJD	DQJB
4	VREFB4N3	IO	DIFFIO B31p		31			AH17							DQ4B	DQ5B	DQ5B
4		10	DIFFIO B31n					W16							DQ4D	DQJD	DQJB
34	VREFB4N3	10	DIFFIO_B311		98	U13	W13	AF16	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
,- <del>-</del>	VICEI DAINS	10	Біі 1 10_502р		50	010	**10	741 10	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,	DQS4B/CQ5B,
34	VREFB4N3	10	DIFFIO B32n		99	V13	Y13	AF17	DPCLK4	DPCLK4	DPCLK4	DPCLK4	DPCLK4	DPCLK4	DPCLK4	DPCLK4	DPCLK4
34	VREFB4N3	IO	DIFFIO B33p			P10	AA15	AB16		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
34	VREFB4N3		DIFFIO B33n		1	P11	AB15	AE16				DQ4B	DQ5B	DQ5B			
34	VREFB4N3	IO	DIFFIO B34p		100	U14	U12	AE17	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
34		VCCINT	F		101	1											1
34	VREFB4N3	10	DIFFIO_B34n		1	V14		AG18	1	DQ5B	DQ5B	1			DQ4B	DQ5B	DQ5B
34		GND			102	Ť		0.0	1			1					
4		IO	DIFFIO_B35p		103	U15	AA16	AH18	DQ5B	1	1	DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0	DQ4B	DQ5B	DQ5B
34	VREFB4N2	VCCIO4	o_boop		104	1							550,5115,1050	550,5110,1550			
34	VREFB4N2	10	DIFFIO B35n		.54	V15	AB16	AH19	<del> </del>	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0
34		GND	5 1 10_D0011		105	V 10	, .010	, 4115	<b>-</b>	2435	2400	2420	2400	2 400	520	DDD0/D110#3B0	2ODO/D44O#3B0
34	VREFB4N2	IO	DIFFIO_B36p		100	1	T12	AD17	<b>-</b>		-	<b>—</b>			DQ2B	DQ5B	DQ5B
34	VREFB4N2	10	DIFFIO B36n		+	R11	T13	AF18		DQ5B	DQ5B				DQZD	DQOD	DQOD
J4	VICEI D4INZ	10	DII I IO_D30II			KII	113	AI 10	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,
34	VREFB4N2	IO			106	P12	V13	AF18	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5
34	VREFB4N2	.0	VREFB4N2		107	T11		Y17	D. OLINO	D. OLINO	D. 02110	D. OLITO	Di GENO	51 02.10	D. OLITO	D. OLIKO	- Br GERG
34	VREFB4N2	10	DIFFIO_B37p		107	1	****	AG21							DQ2B	DQ5B	DQ5B
34	VREFB4N2	10	DIFFIO_B37p		-			AC17							DQZD	DQSB	DQJB
34	VREFB4N2	IO	DIFFIO_B38p		-			AH21							DQ2B	DQ5B	DQ5B
34 34	VREFB4N2	10	DIFFIO_B38p		-		U13	AG22							DQ2B	DQ5B	DQ5B
34	VREFB4N2	10	DIFFIO_B38II				V14	AH22				DQ2B	DQ5B	DQ5B	DQ2B DQ2B	DQ5B DQ5B	DQ5B DQ5B
34 34	VREFB4N2	10	DIFFIO_B39p				U14	AG19				DQZB	DQSB	DQSB	DQZB	DQSB	DQSB
34	VREFB4N2	10	DIFFIO_B39II		+		U15	AH23							DQ2B	DQ5B	DQ5B
		.0	ЫГГЮ_Б40р		400		013	AUS							DQZB	DQ3B	DQSB
34 34	VREFB4N2	IO	DIEEIO DAO-		108		1/45	A E 4 O				DQ2B	DOED	DOCD	DOOD	DOCE	DOED
34 34	VREFB4N2 VREFB4N1	GND	DIFFIO_B40n		400		V15	AE19				DQZB	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
34 34			DIFFIG D44		109			1501							DOOD	DOED	DOSD
		10	DIFFIO_B41p		-		14/45	AF24				DOOD	DOED	DOED	DQ2B	DQ5B	DQ5B
34		IO	DIFFIO_B41n		-			AF19				DQ2B	DQ5B	DQ5B			
34	VREFB4N1	IO	DIFFIO_B42p		_		T14	AF25							DM0B	DQ5B	DQ5B
34	VREFB4N1	10	DIFFIO_B42n		-		T15	AF20				DQ2B	DQ5B	DQ5B	DQ0B		
34	VREFB4N1	IO					AB18	AD18				DQ2B	DQ5B	DQ5B	DQ0B		4
14	VREFB4N1	10	DIFFIO_B43p		-	<del>                                     </del>	AA17	Y19	1	1	1	1				1	+
34	VREFB4N1	IO	DIFFIO_B43n		1	<b>L</b>	AB17	AE21			ļ	<b></b>			DQ0B		4
34	VREFB4N1	IO	VREFB4N1		110	U16	AA18	AC18									<b>_</b>
34	VREFB4N1	IO	DIFFIO_B44p			<u> </u>		AB18									+
34	VREFB4N1	IO	DIFFIO_B44n		1	V16		AA19	<b></b>	DQ5B	DQ5B	<b></b>					<b>_</b>
34		Ю	DIFFIO_B45p		4			AD19									<b>_</b>
34	VIILE DITT	IO	DIFFIO_B45n		1	<u> </u>		AE20	<b></b>			<b></b>					<b>_</b>
34	VREFB4N1	IO	DIFFIO_B46p			<u> </u>	<u> </u>	AC19	ļ	ļ	ļ	ļ			ļ		1
4	VREFB4N1	IO	DIFFIO_B46n			<u> </u>	<u> </u>	AB19	ļ	ļ	ļ	ļ			ļ		
4	VREFB4N1	IO	RUP2		111	T13	AA19	AA17									
4	VREFB4N1	IO	RDN2		112	T14	AB19	AB17									
4	VREFB4N1	IO						AD21									
14	VREFB4N1	Ю	DIFFIO_B47p			U17		AF21									
34	VREFB4N0	IO	DIFFIO_B47n			V17		AE25							DQ0B		
34	VREFB4N0	IO	DIFFIO_B48p				W17	AC21				DQ2B	DQ5B	DQ5B			
									DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,
34	VREFB4N0	IO	DIFFIO_B48n		113	R13	Y17	AF26	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3
34	VREFB4N0	IO	DIFFIO_B49p				AA20	AG25					DQ5B	DQ5B			
34	VREFB4N0	IO	DIFFIO_B49n				AB20	AH25		İ		DQ2B	DQ5B	DQ5B	DQ0B		1
34	VREFB4N0		VREFB4N0		114	P13	V16	AB20		İ							1
	VREFB4N0		DIFFIO B50p		1		U16	AG23								İ	1
34	VKEFB4NU																



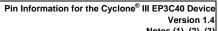


Bank	VREFB	Pin Name /	Optional	Configuration	0240	E224	F484 /	F780	DOS for Y9/Y0 in	DOS for Y9/Y9 in	DOS for V16/V19 in	DOS for Y9/Y0 in	DOS for Y16/Y19 in	DOS for Y22/Y26 in	DOS for Y9/Y0 in	DQS for X16/X18 in	Notes (1), (2), (3
Number	Group	Function	Function(s)	Function	Q240	F324	U484	F/8U		F324		F484/U484	F484/U484	F484/U484	F780	F780	F780
34	VREFB4N0	IO	DIFFIO B50n		-		U17	AF22							DQ0B		
34	VREFB4N0	GND			116												+
34	VREFB4N0	IO	DIFFIO_B51p		1.0			AE24							DQ0B		1
34	VREFB4N0		DIFFIO B51n		1	1		AG26							DQ0B		+
34	VREFB4N0	10	PLL4_CLKOUTp		117	U18	T16	AE23							5405		1
34	VREFB4N0	IO	PLL4_CLKOUTn		118	V18	R16	AF23									+
34	VREFB4N0	IO	DIFFIO B52p		110	V 10	R14	AD22									+
34		VCCINT	Біі і іо_вогр		119	+	1114	ADZZ									+
34		IO	DIFFIO_B52n		113	+	R15	AE22									+
34 34	VREFB4N0		DII I IO_B32II		120		KIS	ALZZ									+
34	VREFB4N0	10	DIFFIO_B53p		120	+		AB21									+
34 34	VREFB4N0	10	DIFFIO_B53p		+	+		AC22								<u> </u>	+
34	VREFB4N0	10	DII 1 IO_B33II			1		AH26									+
B5		VCCD_PLL4			121	P15	V17	Y20									+
B5	VREFB5N3 VREFB5N3				122	P15	V17	AA20									+
						N14											+
35		VCCA4	DIEEIO DEC-		123	N14	U18	Y21									+
35	VREFB5N3	10	DIFFIO_R56n	-	+	+	AA22	AA21				DMOD/DWO#CD	DMOD4/DMC#054	DM4D0/DM0#4D0	-	-	+
35	VREFB5N3	.0	DIFFIO_R56p	1	404	+	AA21	AB22	<del>                                     </del>			DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3	<del>                                     </del>	<del>                                     </del>	+
B5	VREFB5N3		DIEEIO E	1	124	+		ADC:	<del>                                     </del>			-			D140D (D1110 ::	DATOR A IRVINO	D144D0/5:::5::-
B5		Ю	DIFFIO_R55n			1		AB24							DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3
B5	VREFB5N3				125												
B5	VREFB5N3		DIFFIO_R55p			N15		AC24			DM1R1/BWS#1R1						
35	VREFB5N3	Ю	RUP3		126	T16	T17		DQ1R	DQ3R	DQ1R						
35	TITE! BOITO	IO	RDN3		127	R16	T18		DQ1R								
B5	VREFB5N3	Ю						AD25									
										DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,
B5	VREFB5N3	Ю			128	T18	W20	AF27	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4
B5	VREFB5N3	VCCINT			129												
B5	VREFB5N3	IO	DIFFIO_R54n			T17		AE26		DQ3R	DQ1R						
B5	VREFB5N3	GND			130												
35	VREFB5N3	IO	DIFFIO_R54p					AE27									
B5	VREFB5N3	IO	DIFFIO_R53n		131			Y22	DQ1R								
35	VREFB5N3	IO	DIFFIO R53p		132			AD24	DQ1R								
B5	VREFB5N3	IO	VREFB5N3		133	R18	W19	AA24									
B5		IO	DIFFIO R52n					AC25									1
B5	VREFB5N3	IO	DIFFIO R52p					AD26							DQ3R	DQ3R	DQ1R
35	VREFB5N3	IO	DIFFIO_R51n		134		Y22		DQ1R			DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
35	VREFB5N2	IO	DIFFIO_R51p		135		Y21	AA23									
35	VREFB5N2	IO	DIFFIO R50n		100		U20	AD28				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
35		IO	DIFFIO_R50p				U19	Y23									
35		Ю	DIFFIO R49n				W22	AD27				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5		IO	DIFFIO R49p			1	W21	AC26				DQ3R	DQ3R	DQ1R	Daoit	D QUIT	
B5	VREFB5N2	IO	DIFFIO_R48n		1	1	***	Y24				DQOIL	DQUIT	DQIII	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	10	DIFFIO_R48p		+	+	-	W22	<del> </del>						Dan	DOUN	DQIIV
B5	VREFB5N2	10	DIFFIO_R46p	1	+	1		AC28							DQ3R	DQ3R	DQ1R
B5	VREFB5N2	10	DIFFIO_R47h DIFFIO R47p	1	1	1		W21	1						Dan	באסוג	Dalik
B5		10	DIFFIO_R47p DIFFIO_R46n	1	+	1	D15	AC27							DQ3R	DQ3R	DQ1R
			DIFFIO_K40[I	-	126	+	P15	MU21							DUSK	DUJK	DUIK
B5	VREFB5N2 VREFB5N2	IO	DIEEIO DAG-	-	136	+	DAG	AB26	DQ1R						DQ3R	DQ3R	DQ1R
B5		.0	DIFFIO_R46p	1	137	+	P16	AB26	DQTK			-			DQ3K	DQ3K	DQTK
B5	VREFB5N2			1	138	1		1/00	ļ						1	1	+
B5	VREFB5N2	IO		1	1	L		V26	1						1	1	+
B5		IO	VREFB5N2		139	R17	R17	U24									
B5	VREFB5N2			ļ	1	<b>_</b>	P17	V22							L		<del> </del>
35	VREFB5N2	IO	DIFFIO_R45n		1	1	V22	AA26				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	Ю	DIFFIO_R45p	ļ	1	1	V21	U26	ļ			DQ3R	DQ3R	DQ1R	ļ	ļ	1
B5	VREFB5N2	VCCINT			140												
B5	VREFB5N2	IO	DIFFIO_R44n		1		R20	AB28				DQ3R	DQ3R	DQ1R	DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2
B5	VREFB5N2	GND			141												
B5	VREFB5N2	Ю	DIFFIO_R44p					AB27							DQ1R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R43n				U22	V21				DQ3R	DQ3R	DQ1R			
B5	VREFB5N1	IO	DIFFIO_R43p				U21	Y26				DQ3R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	Ю	DIFFIO_R42n		1	P18	R18	U20		DQ3R	DQ1R						1
		IO	DIFFIO_R42p		1	P17	R19	W26		DQ3R	DQ1R	DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2	DQ1R	DQ3R	DQ1R
B5	VREFB5N1																



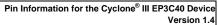


Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484/	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in		Notes (1), (2), (
Number	Group		Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
35	VREFB5N1	IO	DIFFIO_R41p					W28							DQ1R	DQ3R	DQ1R
5	VREFB5N1	Ю	DIFFIO_R40n					AB25									
5	VREFB5N1	Ю	DIFFIO_R40p				N16	V28							DQ1R	DQ3R	DQ1R
35	VREFB5N1	Ю	DIFFIO_R39n				R22	AA25				DQ1R	DQ3R	DQ1R			
35	VREFB5N1	IO	DIFFIO_R39p				R21	V27				DQ1R	DQ3R	DQ1R			
35	VREFB5N1	Ю	VREFB5N1		142	N16	P20	U23									
35	VREFB5N1	IO			1			W25									
35	VREFB5N1	IO	DIFFIO_R38n		1		P22	V25		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
35 35	VREFB5N1	10	DIFFIO_R38p		1	L13	P21	R22		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R			
35 35	VREFB5N1 VREFB5N1	10	DIFFIO_R37n DIFFIO_R37p		1	1		V24 U27									
35	VREFB5N1	10	DIFFIO_R36n		+	L15	N20	V23		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	1		
35	VREFB5N1	10	DIFFIO_R36p		+	L13	N19	U28		DQ3R DQ3R	DQ1R DQ1R	DQIK	DQSK	DQIK	DQ1R	DQ3R	DQ1R
35	VREFB5N1	10	DIFFIO_R35n		1	L14	IN 19	Y25		DQ3K	DQIK				DQIK	DQ3R	DQIK
35	VREFB5N1	10	DIFFIO R35p					T26									
35	VREFB5N0	10	DIFFIO R34n		1	1		W20									
35		10	DIFFIO_R34p		1	1		U22									
35	VREFB5N0	10	DIFFIO R33n		1	M17	N17	V20		DQ3R	DQ1R				1		
35	VREFB5N0	10	DIFFIO_R33p		143	L16	N18		DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6
35	VREFB5N0	.0	DIFFIO R32n	DEV OE	144		N22	T22	D. OLITO	D. OLIKO	D. OLIVO	D. OLINO	D. 02.10	DI OLIKO	D. OLIVO	D. OLIKO	D. OLIKO
35	VREFB5N0		DIFFIO R32p	DEV_OL DEV CLRn	145	L17	N21	T21	1	1	<u> </u>		1	1	1	<u> </u>	1
35	VREFB5N0		DIFFIO R31n				M22	R26				DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R
35	VREFB5N0		DIFFIO_R31p				M21	R25				DQ1R	DQ3R	DQ1R			
35	VREFB5N0	10	DIFFIO_R30n				M20	R28				DQ1R	DQ3R	DQ1R	DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R
35		Ю	DIFFIO_R30p				M19	U25				DQ1R	DQ3R	DQ1R			
35	VREFB5N0	Ю	VREFB5N0		146	L18	M16	R24									
35	VREFB5N0	IO						R27								DQ1R	DQ1R
35	VREFB5N0	VCCINT			147												
35	VREFB5N0	Ю	DIFFIO_R29n			K18		R23		DM1R/BWS#1R	DM1R0/BWS#1R0						
35	VREFB5N0	GND			148												
35	VREFB5N0	IO	DIFFIO_R29p			K17		R21		DQ1R	DQ1R						
35	VREFB5N0	Ю						P21									
35	VREFB5N0		DIFFCLK_3n		149	N18	T22	Y28									
35	VREFB5N0		DIFFCLK_3p		150	N17	T21	Y27									
36	VREFB6N3	CLK5	DIFFCLK_2n		151	F18	G22	J28									
36	VREFB6N3	CLK4	DIFFCLK_2p		152	F17	G21	J27									
36	VREFB6N3	CONF_DONE		CONF_DONE	153	K14	M18	P24									
36	VREFB6N3	VCCIO6			154												
36	VREFB6N3	MSEL0		MSEL0	155	K13	M17	N22									
36	VREFB6N3	GND		MOELA	156	140	1.40	Doo									
36	VREFB6N3 VREFB6N3	MSEL1 MSEL2		MSEL1 MSEL2	157 158	J18 J17	L18 L17	P23 M22							1		
36 36	VREFB6N3 VREFB6N3	MSEL2 MSEL3		MSEL2 MSEL3 (4)	108	J17 J14	K20	M22 P22							1		
36 36	VREFB6N3 VREFB6N3	IO	DIFFIO_R28n	IVIOELO (4)	+	J14	INZU	K25	<del> </del>	<del> </del>	1	1	-	<del> </del>	<del> </del>	1	+
36		10	DIFFIO_R28h	1	<del>                                     </del>	H17	1	M24		DQ1R	DQ1R						+
36	VREFB6N3		DIFFIO_R28p	INIT DONE	159	G18	L22	P26		2411	2411	1				<b>+</b>	+
36	VREFB6N3	10	DIFFIO_R27p	CRC_ERROR	160	G17	L21	P25							1		
36	VREFB6N3	10	DIFFIO R26n				l	H26	1	1	1	1		1	1	1	1
36	VREFB6N3	Ю	DIFFIO_R26p					L25									
36	VREFB6N3	IO	VREFB6N3		161	J13	K19	N21									
36	VREFB6N3	Ю	DIFFIO_R25n					N25									
36	VREFB6N3	Ю	DIFFIO_R25p					G24									
36	VREFB6N3	Ю	DIFFIO_R24n	nCEO	162	E18	K22	P28									
36	VREFB6N3	VCCINT			163												
36	VREFB6N3	Ю	DIFFIO_R24p	CLKUSR	164	E17	K21	P27									
36	VREFB6N3	GND			165												
36	VREFB6N3	Ю	DIFFIO_R23n		166	H16	J22	N26	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7
36		10	DIFFIO_R23p				J21	L22				DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1			
36	VREFB6N3	10	DIFFIO_R22n				H22	M28				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R
٠	VREFB6N2	IO	DIFFIO_R22p				H21	M23			1	DQ0R	DQ1R	DQ1R			<u> </u>
36 36	VREFB6N2	10						M27							DQ0R	DQ1R	DQ1R





																N	Notes (1), (2), (3
Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324		F780								DQS for X16/X18 in	
Number	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
																	ļ
B6	VREFB6N2		DIFFIO_R21p		<u> </u>			M26							DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R20n		<u> </u>		K17	K22									<b></b>
B6	VREFB6N2	Ю	DIFFIO_R20p				K18	L23				DQ0R	DQ1R	DQ1R			ļ
B6		VCCINT			167												
B6	VREFB6N2	Ю						J26									ļ
B6	VREFB6N2	GND			168												
B6	VREFB6N2	IO	DIFFIO_R19n		<u> </u>			H25									
B6	VREFB6N2	IO	DIFFIO_R19p					K21									<del>                                     </del>
B6	VREFB6N2	10	VREFB6N2		169	H18	J18	M25				DOOD	DOID	2012			<del>                                     </del>
B6	VREFB6N2	10	DIFFIO_R18n		<u> </u>	-	F22 F21	J23				DQ0R	DQ1R	DQ1R	DOOD	2012	2012
B6 B6	VREFB6N2	10	DIFFIO_R18p		<u> </u>	-	F21	L28 L27				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R DQ1R	DQ1R DQ1R
B6		10	DIFFIO_R17n DIFFIO_R17p		<u> </u>	-		L21 L24							DQ0R DQ0R	DQ1R DQ1R	DQ1R DQ1R
		.0			<del>                                     </del>										DQUR	DQIR	DQIK
B6 B6	VREFB6N2 VREFB6N2	10	DIFFIO_R16n		<u> </u>	-		E25							DQ0R	DQ1R	DQ1R
	VREFB6N2		DIFFIO_R16p		1			K28	-						DQUR	DQIR	DQIK
B6 B6	VREFB6N2 VREFB6N1	10	DIFFIO_R15n	-	<del>                                     </del>		<del>                                     </del>	F24 K27	<b>_</b>		<b>_</b>	<del>                                     </del>			DQ0R	DQ1R	DQ1R
		10	DIFFIO_R15p	<b>+</b>	1	1	1	J24	<b>-</b>		-	<del>                                     </del>			DQUK	טעוג	אואט
B6 B6	VREFB6N1 VREFB6N1	10	DIFFIO_R14n DIFFIO_R14p	-	<del>                                     </del>		<del>                                     </del>	J24 L26	<b>_</b>		<b>_</b>	<del>                                     </del>			DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0
B6	VREFB6N1 VREFB6N1	10	DIFFIO_R14p DIFFIO_R13n	<b>+</b>	1	1	H20	H23	<b>-</b>		-	DQ0R	DQ1R	DQ1R	DIVIZK	DINITRO/BWS#1R0	DIVI (RU/BWS#1RU
		.0			<del>                                     </del>											DOAD	DO4D
B6 B6	VREFB6N1 VREFB6N1	IO VCCIO6	DIFFIO_R13p	-	170	1	H19	J25	<b>_</b>		<b>_</b>	DQ0R	DQ1R	DQ1R	-	DQ1R	DQ1R
	VREFB6N1 VREFB6N1	VCCIO6	DIFFIO R12n	nWE		D10	E22	Cae	DQ1R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6 B6		GND	DIFFIO_R12h	nvvE	171 172	D18	E22	G28	DQ1R	DQ1R	DQ1R	DQUR	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
		GND	DIFFIO R12p	nOE	1/2	D47	F04	007		DOAD	DOAD		DQ1R	2012	DQ2R	2012	DQ1R
B6	VREFB6N1 VREFB6N1	10	DIFFIO_R12p DIFFIO_R11n	nOE	<u> </u>	D17	E21	G27		DQ1R	DQ1R		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
B6 B6		10	DIFFIO_R11p		1			H22 H24	-								+
B6	VREFB6N1	10	VREFB6N1		173	H15	1140	M21									<del> </del>
	VREFB6N1	10	DIFFIO R10n		173	ніэ	H18 J17	G25									
B6	VREFB6N1	10	DIFFIO_R10n DIFFIO R10p		<del>                                     </del>		_								DQ2R	DOAD	DQ1R
B6 B6		10			<del>                                     </del>		H16 D22	K26				DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0	DQZR	DQ1R	DQTR
	VREFB6N1 VREFB6N1	10	DIFFIO_R9n DIFFIO_R9p		1		D22 D21	G26	-			DIVIZR	DQ1R	DQ1R			+
B6 B6	VREFB6N1	10	DIFFIO_R9p DIFFIO R8n	nAVD	1	H14	F20	G23 F28	-	DQ1R	DQ1R	DQ2R	DQ1R DQ1R	DQ1R DQ1R	DQ2R	DQ1R	DQ1R
B6				NAVD	1			F27	-						DQZR	DQIR	DQTR
	VREFB6N1	10	DIFFIO_R8p DIFFIO_R7n	PADD23	<del>                                     </del>	H13	F19 G18			DQ1R	DQ1R DQ1R	DQ2R DQ2R	DQ1R DQ1R	DQ1R	DOOD	DO4D	DQ1R
B6 B6	VREFB6N1	10	DIFFIO_R/II	PADD23	1	G14	H17	E28 G22	-	DQ1R	DQTR	DQZR	DQIK	DQ1R	DQ2R	DQ1R	DQTR
		10			1			E27				DOOD	DOAD	DO4D	DOOD	DO4D	DOAD
B6 B6	VREFB6N1 VREFB6N0	10	DIFFIO_R6n DIFFIO_R6p		1		C22 C21	H21				DQ2R DQ2R	DQ1R DQ1R	DQ1R DQ1R	DQ2R	DQ1R	DQ1R
B6		10	DIFFIO_Rop				C21	F26				DQZK	DQTK	DQIK	DQ2R	DQ1R	DQ1R
B6	VREFB6N0				174			F26							DQZR	DQIR	DQTR
B6		IO	DIFFIO_R5n	PADD22	174	C18	DOO	D28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R			+
B6		GND	DIFFIO_RSII	PADD22	175	C18	BZZ	D28		DQIK	DQTR	DQZR	DQIK	DQTK			+
B6	VREFB6N0	IO	DIFFIO_R5p	PADD21	173	C17	B21	D27		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
ы	VIVELDOINO	10	אפא_טו־ז ווע	FADDEI	<b>-</b>	017	DZ I	UZI	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQ1R DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,
B6	VREFB6N0	10	DIFFIO R4n	PADD20	176	B18	C20	C27	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5
B6		10	DIFFIO_R4p		.,,	510	020	F25	02.10	02.10			02.0	02.10	02.10	02.10	02.10
B6		10	VREFB6N0		177	B17	D20	J22	1		1	1					
B6		10	DIFFIO R3n		<del>'''</del>	<u> </u>		E26	1		1	1					
B6	VREFB6N0	10	DIFFIO_R3p					E24	İ	İ	İ	1					
B6	VREFB6N0	10	DIFFIO R2n				F17	D25	İ	İ	İ	DQ2R	DQ1R	DQ1R			
B6	VREFB6N0	10	DIFFIO_R2p				G17	D24	İ	İ	İ						
B6	VREFB6N0	10	DIFFIO_R1n	1			i e	D26	İ	İ	İ	İ		İ		1	
B6		10	DIFFIO_R1p	1		t —	l	C26	1	1	1	1				1	1
B6	VREFB6N0			1	178	F14	F18	J21	İ	İ	İ	İ		İ		1	
B6	VREFB6N0		İ	1	179	F15	E18	H20	İ	İ	İ	İ		İ		1	
B6	VREFB6N0	VCCD PLL2			180	E15	E17	J20									
B7	VREFB7N0	VCCINT			181												1
B7	VREFB7N0	IO	İ	1	1			G21	İ	İ	İ	İ		İ		1	
B7		GND			182	1			1		1	1					
B7	VREFB7N0	IO	DIFFIO_T52n			1		B26	1		1	1			DQ0T		
B7		10	DIFFIO_T52p	1		t	1	D22	1		1	t			DQ0T	1	1
B7		10	DIFFIO_T52p	1		t	F16	E22	1		1	t			DQ0T	1	1
B7	VREFB7N0	10	DIFFIO_T51p	1		t —	E16	J19	1	1	1	DQ2T	DQ5T	DQ5T		1	1
B7	VREFB7N0	10	DIFFIO_T50n	1		t	F15	A26	1		1	DQ2T	DQ5T	DQ5T	DQ0T	1	1
	1 * (LI D/ 140		DIO_10011				. 10	, .20		l		10461	10401	2401	- 401	1	



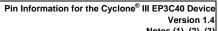


ank umber	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 F780
umber	Group	runction	runction(s)	Function			U404		Q240	F324	F324	F404/U404	F404/U404	F404/U404	F760	F760	F700
7	VREFB7N0	IO	DIFFIO_T50p				G16	G20									
,	VREFB7N0	Ю						B25							DQ0T		
	VREFB7N0	Ю	DIFFIO_T49n			C16	G15	G19									
	VREFB7N0	IO	DIFFIO T49p		183	D16	F14	A25	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6
		10	DIFFIO T48n		103	D10	H15	F21	CDFCLRO	CDFCLRO	CDFCLRO	CDFCLRO	CDFCERO	CDFCLRO	DQ0T	CDFCLRO	CDFCLRO
	VREFB7N0	IO	DIFFIO_T48p			A18	H14	C25		DQ5T	DQ5T				DQ0T		
	VREFB7N0	IO	VREFB7N0		184	A17	D17	F22									
	VREFB7N0	Ю						A23							DQ0T		
	VREFB7N0		DIFFIO_T47n				C19	H19 B23				DQ2T DQ2T	DQ5T DQ5T	DQ5T DQ5T	DM0T		
	VREFB7N0 VREFB7N0		DIFFIO_T47p PLL2 CLKOUTn		185	C14	D19 A20	C23				DQ21	DQ51	DQ51	DM01		
	VREFB7N1	10	PLL2_CLKOUTp		186	D14	B20	D23									
	VREFB7N1	IO	DIFFIO T46n		100	<u> </u>	DEO	C24							DQ2T	DQ5T	DQ5T
	VREFB7N1	IO	DIFFIO_T46p				C17	E21				DQ2T	DQ5T	DQ5T			
	VREFB7N1	IO	RUP4		187	E14	B19	F19									
	VREFB7N1	IO	RDN4		188	E13	A19	E19									
		IO IO	DIEEIO TAG-	ļ	+	-	A10	C22	<del>                                     </del>			DOST	DOST	DOST	DQ2T	DQ5T	DQ5T
	VREFB7N1 VREFB7N1	IO	DIFFIO_T45n DIFFIO_T45p	PADD0	+	E12	A18 B18	D21 B22	<del> </del>	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
	VREFB7N1	10	VREFB7N1	LVDDA	189	D12	D15	F18		DQ31	DQJI						
	VREFB7N1	10	DIFFIO_T44n	İ	1.00	1	E15	C21	1			DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
		IO	DIFFIO_T44p				G14	D19									
	VREFB7N1	IO	DIFFIO_T43n					A22							DQ2T	DQ5T	DQ5T
	VREFB7N1	Ю	DIFFIO_T43p					A21							DQ2T	DQ5T	DQ5T
		VCCINT			190	<u> </u>											
	VREFB7N1	10	DIFFIO_T42n		404		G13	B21							DQ2T	DQ5T	DQ5T
	VREFB7N1 VREFB7N1	GND	DIFFIO_T42p		191			E18							DQ2T	DQ5T	DQ5T
		VCCIO7	DIFFIO_142p		192			E10							DQZI	DQST	DQST
	VREFB7N1	IO	DIFFIO T41n	PADD1		A16	A17	C18				DQ2T	DQ5T	DQ5T		DQ5T	DQ5T
	VREFB7N2	GND	-		193												
	VREFB7N2	IO	DIFFIO_T41p	PADD2	194	B16	B17	D18	DQ5T	DQ5T	DQ5T		DQ5T	DQ5T			
	VREFB7N2	Ю	DIFFIO_T40n				A16	C20				DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0	DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5
	VREFB7N2		DIFFIO_T40p				B16	H17				DQ4T	DQ5T	DQ5T			
	VIII DIIIL	10	VREFB7N2 DIFFIO_T39n	-	195	C12	C15	G17 D20	-						DQ4T	DQ5T	DQ5T
	VREFB7N2 VREFB7N2	IO	DIFFIO_T39h			1		C19							DQ4T	DQ5T	DQ5T
	VREFB7N2	10	DIFFIO T38n	PADD3	196	A15	E14	C17		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
	VREFB7N2	IO	DIFFIO_T38p		197			G18	DQ5T								
	VREFB7N2	IO						H15									
	VREFB7N2				198												
			DIFFIO_T37n					F17									
	VREFB7N2	GND	1	<del>                                     </del>	199	+		<b> </b>	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,
	VREFB7N2	IO	DIFFIO T37p	PADD4	200	B15	F13	D17	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8	DQS21/CQ31, DPCLK8
	VREFB7N2	10	DIFFIO_T36n	PADD5	201	A14	A15	A19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
	VREFB7N3		DIFFIO_T36p	PADD6	202	B14	B15	B19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
	VREFB7N3	IO	DIFFIO_T35n	PADD7		A13	C13	A18									
	VREFB7N3		DIFFIO_T35p	PADD8		B13	D13	B18		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
	VREFB7N3		DIFFIO_T34n	<b> </b>	<del> </del>	<del>                                     </del>		E17	1		1	1	1	<b> </b>	DQ4T	DQ5T	DQ5T
	VREFB7N3 VREFB7N3	10	DIFFIO_T34p	-	+	+		J16 J17	-		-	<b> </b>	-	-	-	-	+
	VREFB7N3 VREFB7N3	IO	DIFFIO_T33n DIFFIO_T33p	<del> </del>	+	+		J17 H16	<del> </del>		1	1	1	<del> </del>		1	1
	VREFB7N3	10	DIFFIO_133p	<b>+</b>	+	1		G16	<b>†</b>		<del> </del>	<b>†</b>	+	<b>+</b>	1	<u> </u>	1
	VREFB7N3	10	DIFFIO_T32p		1	1		F15									
	VREFB7N3	10	VREFB7N3		203	E11	E13	G15									
	VREFB7N3	10	DIFFIO_T31n	PADD9		A12	A14	C16		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
	VREFB7N3	VCCINT			204												
	VREFB7N3	IO	DIFFIO_T31p	PADD10	1	B12	B14	D16				DQ4T	DQ5T	DQ5T			
	VREFB7N3		DIFFIG TOO	<b> </b>	205	<del>                                     </del>		114.	1		1	1	1	<b> </b>	1	1	1
	VREFB7N3 VREFB7N3	10	DIFFIO_T30n DIFFIO_T30p	-	+	+		H14 K15	-		-	<b> </b>	-	-	-	-	+
			IDIFFIO 1300	1		1		L ID	1	1	1	1	1	1	1	1	1



## Pin Information for the Cyclone® III EP3C40 Device Version 1.4 Notes (1), (2), (3)

																ľ	lotes (1), (2), (3)
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780
37	VREFB7N3	VCCIO7			206												
B7	VREFB7N3	Ю	DIFFIO T29p	PADD12	207	B11	B13	B17	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9
37	VREFB7N3	GND			208												
B7	VREFB7N3		DIFFIO_T28n					E15							DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1
B7	VREFB7N3	IO	DIFFIO_T28p			<u> </u>	E12	J14					DQ5T	DQ5T			
B7	VREFB7N3	IO IO	DIFFIO_T27n	PADD13 PADD14		C10 D10	E11	C15 D15		DM5T/BWS#5T	DM5T0/BWS#5T0	DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1	DQ5T	DQ3T	DQ5T
B7	VREFB7N3 VREFB7N3	CLK8	DIFFIO_T27p DIFFCLK 5n	PADD14	209	A10	F11 A12	A15				DM41	DM511/BW5#511	DM511/BW5#511	DQ51	DQ31	DQ51
B7	VREFB7N3	CLK9	DIFFCLK_5p		210	B10	B12	B15									
B8	VREFB8N0	CLK10	DIFFCLK 4n		211	A9	A11	A14									
B8	VREFB8N0	CLK11	DIFFCLK_4p			В9	B11	B14									
B8	VREFB8N0	IO	DIFFIO_T26n				D10	C13				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	Ю	DIFFIO_T26p				E10	D13							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T25n				A10	C14				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	10	DIFFIO_T25p	PADD15		E10	B10	D14		DOST	DOST	DOST	DOST	DOST	DOST	DOST	DOST
B8	VREFB8N0 VREFB8N0	10	DIFFIO_T24n	PADD16	213	C9	A9	C12		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	AVEL BOING	v CCIO8	<del>                                     </del>		213	<del>                                     </del>	1	<del>                                     </del>	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,
B8	VREFB8N0	Ю	DIFFIO_T24p	PADD17	214	D9	В9	D12	DPCLK10	DPCLK10		DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10
B8	VREFB8N0	GND			215												
B8	VREFB8N0	IO	DIFFIO_T23n					A12							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	Ю	DIFFIO_T23p					B12									
B8	VREFB8N0	IO	VREFB8N0		216	E9	C10	G14									
B8	VREFB8N0	IO	DIFFIO_T22n		217		G11	K13	DQ5T								
B8 B8	VREFB8N0 VREFB8N0	10	DIFFIO_T22p					F14 E14							DQ5T	DQ3T	DQ5T
B8	VREFB8N0	10	DIFFIO T21n		1			H12							DQST	DQ31	DQ51
B8		10	DIFFIO T21p		+			J12									
B8	VREFB8N0	IO	DIFFIO T20n	DATA2	218	A8	A8	A11		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T20p	DATA3	219	B8	B8	B11	DQ5T			DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T19n	PADD18		A7	A7	A10		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T			
B8	VREFB8N1	VCCINT			220												
B8	VREFB8N1	IO	DIFFIO_T19p	DATA4		B7	B7	B10	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2
B8 B8	VREFB8N1 VREFB8N1	GND	DIFFIO T18n	PADD19	222	4.0	A6	040		DOST	DOST	DOST	DOST	DOST			
B8	VREFB8N1	10	DIFFIO_T18p	DATA15	1	A6 B6	B6	G13 H13		DQ3T	DQ5T	DQ5T DQ5T	DQ3T DQ3T	DQ5T DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T18p	DATAIS	+	DO	БО	B8				DQJI	DQSI	DQJI	DQ31	DQ31	DQJI
B8	VREFB8N1	IO	DIFFIO T17p					C10							DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO						D11									
B8	VREFB8N1	IO	VREFB8N1		223	C7	E9	F11									
									DQS3T/CQ3T#,	DQS3T/CQ3T#,		DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,
B8	VREFB8N1	IO	DIFFIO_T16n	DATA14	224	A5	C8	E12	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11
B8		10	DIFFIO_T16p	DATA13		B5	C7	F12				DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2			
B8 B8	VREFB8N1 VREFB8N1	IO IO	DIFFIO_T15n DIFFIO_T15p	<b> </b>	1	<del>                                     </del>	<del>                                     </del>	D10 F10	-		<del>                                     </del>			<b>_</b>	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	10	DIFFIO_115p		<del>                                     </del>		H11	E11	<u> </u>		<u> </u>			<del> </del>	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	10	DIFFIO_T14II		<b>†</b>	<b>†</b>	H10	E8	1		1	1		1	_ 40.	_ 40.	- 40.
B8	VREFB8N1	10	DIFFIO_T13n	1	1		1	E10									
B8	VREFB8N2	Ю	DIFFIO_T13p					E7									
B8	VREFB8N2	10	DIFFIO_T12n					A7							DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T12p		<u> </u>	<u> </u>	ļ	G10									
B8	VREFB8N2	10	DIFFIO_T11n		00-	<u> </u>	<b> </b>	G11	1		1			1		ļ	
B8 B8	VREFB8N2 VREFB8N2		DIFFIO_T11p	DATA5	225 226	C5	A5	B7	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	GND	DII FIO_I I I I	באואט	227	CO	70	וטו	וטעטו	DUST	DQJI	DQ31	וטעטו	DQJI	וטעטו	DQJI	DQJ1
B8	VREFB8N2	IO	DIFFIO T10n	1		<u> </u>	<b>1</b>	B3	†		1				1		
B8	VREFB8N2	VCCINT			228			<u> </u>									
B8	VREFB8N2	Ю	DIFFIO_T10p	1				J10									
38	VREFB8N2	GND			229												
B8	VREFB8N2	10	DIFFIO_T9n					F8			ļ						
B8	VREFB8N2	IO	DIFFIO_T9p		<u> </u>	<u> </u>		F7									
B8	VREFB8N2	10	VREFB8N2		230	D7	B5	G12									
B8	VREFB8N2	IO	DIFFIO_T8n	1	1	<u> </u>	G10	A6	l	l		l		L		L	





																l	Notes (1), (2), (
Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324		F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 i
umber	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
8	VREFB8N2 VREFB8N2	10	DIFFIO_T8p DIFFIO_T7n	DATA6 DATA7	231 232	E8 A4	F10 C6	B6 C11	DQ5T DM5T/BWS#5T	DQ3T DQ3T	DQ5T DQ5T	DQ3T DQ3T	DQ3T DQ3T	DQ5T DQ5T	DQ3T DQ3T	DQ3T DQ3T	DQ5T DQ5T
В		10	DIFFIO_T7p	DATA	232	A4	D7	H10	DIVIST/BVVS#ST	DQ31	DQ51	DQ31	DQ31	DQ51	DQ31	DQ31	DQ51
3		10	DII 110_17p			1	<i>D1</i>	G8									
8		10	DIFFIO_T6n				A4	C9				DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
8		VCCINT	_		233												
8		Ю	DIFFIO_T6p	DATA8		B4	B4	D9				DQ3T	DQ3T	DQ5T			
8	VREFB8N3	GND			234												
8	VREFB8N3	Ю	DIFFIO_T5n	DATA9		E7	F8	A8		DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3
3	VREFB8N3	Ю	DIFFIO_T5p				G8	C8							DQ1T		
3	VREFB8N3							D8							DQ1T		
3	VREFB8N3		DIFFIO_T4n	DATA10		A3	A3	C7		DM3T/BWS#3T	DM5T1/BWS#5T1	DQ3T	DQ3T	DQ5T	DQ1T		
3	VREFB8N3		DIFFIO_T4p	DATA11		B3	B3	D7				DQ3T	DQ3T	DQ5T			
В	VREFB8N3		VREFB8N3		235	E6	D6	G9									
В	VREFB8N3					1		D6							DQ1T		
3	VREFB8N3	10	DIFFIO_T3n			1	C3	A4				DQ3T	DQ3T	DQ5T	DQ1T		
									DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,	DQS1T/CQ1T#,
3	VREFB8N3	IO	DIFFIO_T3p	DATA12	236	D5	C4	B4	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7
3	VREFB8N3		DIEEIO TO	<b></b>	237	1		4.0	<del>                                     </del>				<b></b>		DOAT		
3	VREFB8N3 VREFB8N3		DIFFIO_T2n	<b>—</b>	220	1		A3	<del>                                     </del>				<del>                                     </del>		DQ1T	<del>                                     </del>	
3	VREFB8N3 VREFB8N3	IO	DIFFIO T2p	-	238	-		C6	<b>-</b>				-		DQ1T	-	1
3		10	DIFFIO_T2p			1	F7	H8				DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3	DQTI		
3	VREFB8N3		DIFFIO_T1p			1	G7	C4	1			DIVIST/BWS#31	DIVISTI/BVVS#3TT	DIVISTS/BVVS#STS	DQ1T		
3	VREFB8N3		ЫПТЮ_ПР			1	F9	D4							DM1T		
	VREFB8N3		PLL3 CLKOUTn		239	A1	E6	C5							DIVITI		
	VREFB8N3		PLL3_CLKOUTp		240	A2	E5	D5									
1	VREFB8N3		r eed_derkoorp		2.10	1	G9	C3									
		VCCINT				G7	J11	K9									
		VCCINT				G8	J12	K11									
		VCCINT				G10	L14	L16									
		VCCINT			1	G11	M14	K17									
		VCCINT				G12	P11	K19									
		VCCINT				H7	P12	L10									
		VCCINT				H12	L9	L12									
		VCCINT				J7	M9	L14									
		VCCINT				J12	J13	L18									
		VCCINT				K7	J14	N20									
		VCCINT				K12	K14	M11									
		VCCINT				L7	J10	M13									
		VCCINT				L12		M15									
		VCCINT		<b></b>		M7	N9	M17	<del>                                     </del>				<b></b>				1
		VCCINT		<b></b>		M8		M19	<del>                                     </del>				<b></b>				
		VCCINT		-	<u> </u>	M9 M11	P10 P13	N10 N12	<del>                                     </del>	-			-		1	+	1
	1	VCCINT		1	1	M11 M12	P13	N12 N14	1				-		1		1
	1	VCCINT		1	1	F10		N14 N16	1				-		1		1
		VCCINT	<del> </del>	<del>                                     </del>	<del>                                     </del>	F10	J16	N18	<del>                                     </del>	<del> </del>	<del> </del>	<del> </del>	<del>                                     </del>	<del> </del>	1	1	<del> </del>
		VCCINT			<del>                                     </del>	F6		P9	<b>-</b>							<b> </b>	1
		VCCINT	1	<del> </del>		F8	L16	P11	<b>†</b>	1	1	1	<del> </del>	1	İ	<u> </u>	1
		VCCINT	1	<del> </del>		G13	M15	P13	<b>†</b>	1	1	1	<del> </del>	1	İ	<u> </u>	1
		VCCINT	İ	İ		M6		P15	İ	İ		İ	1		İ		İ
		VCCINT	İ	İ		N11		P17	İ	İ		İ	1		İ		İ
		VCCINT				N13	R8	P19									
		VCCINT				N7	H9	R10									
		VCCINT				N9		R12									
		VCCINT						R14									
		VCCINT						R16									
		VCCINT						R18									
		VCCINT						R20									
		VCCINT						T11									
		VCCINT						T13									
		VCCINT				$oxed{\Box}$		T15									
	1	VCCINT	<u> </u>					T17									



																l I	otes (1), (2), (
ank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36
umber	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	F780	F780
		VCCINT						T19									
		VCCINT						U10									
		VCCINT						U12									
		VCCINT						U14									
		VCCINT						U16									
		VCCINT						U18									
		VCCINT						V11									
		VCCINT						V15									
	1	VCCINT				1		V17									
	1	VCCINT				1		V19									
	1	VCCINT				1		V13									
		VCCINT	+		_	+		W12			<u> </u>					-	
	1	VCCINT			-	+		W14									<del> </del>
	1	VCCINT			-	+		W18									<del> </del>
	1	VCCIN1			-	E4	D4										<del> </del>
		VCCIO1			_	F4 G4		B1 H1									
	1		1							-	-					-	
		VCCIO1	<del> </del>		-	J4		K5	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>			-	<del>                                     </del>	<del></del>
		VCCIO1	1	+	-	1		K8	1	1	1	1			1	1	<del>                                     </del>
		VCCIO1	1	+	-	1		N1	1	1	1	1			1	1	<del>                                     </del>
	1	VCCIO1			-	1		N5									<b></b>
		VCCIO2				K4	N4	AA1									<b></b>
		VCCIO2	ļ	1		M4		AG1	ļ	ļ	ļ	ļ				ļ	1
		VCCIO2				N4		T1									
		VCCIO2					R4	T5									
		VCCIO2						W7									
		VCCIO2						W5									
		VCCIO3				R6	AB2	AA11									
		VCCIO3				R7	W5	AD6									
		VCCIO3				R9		AD9									
		VCCIO3					W11	AD13									
		VCCIO3						AH2									
		VCCIO3						AH5									
		VCCIO3						AH9									
		VCCIO3						AH13									
	1	VCCIO3				1		AB10									
	1	VCCIO4				R10		AA18									
	1	VCCIO4				R12		AD16									
	1	VCCIO4			-	R14	WIZ	AD10									<del>                                     </del>
		VCCIO4	+		_	11.14	W18	AD23			<u> </u>					-	
		VCCIO4			_	1	Y14	AH16									
					_	1	114										
		VCCIO4 VCCIO4	<del> </del>		-	1		AH20 AH24	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>			-	<del>                                     </del>	<del></del>
	1				-	1											
		VCCIO4	<b></b>			1		AH27							ļ		<del></del>
		VCCIO4	<b></b>			1		Y16							ļ		<del></del>
	1	VCCIO5			-			AA28									
		VCCIO5				M15		AG28									
		VCCIO5	ļ	1		R15	Y19	T24	ļ	ļ	ļ	ļ				ļ	1
		VCCIO5	1				T19	T28									
		VCCIO5						U21									
		VCCIO5						W24									1
		VCCIO6				F16	E19	B28									
		VCCIO6				G15	G19	H28									
		VCCIO6				J15	L19	K24									
		VCCIO6	1					L21									
		VCCIO6						N24									
		VCCIO6	Ì		1			N28	İ	İ	İ	İ		İ		İ	
		VCCIO7			1	D11	A21	A16	1		1	1					
		VCCIO7	1		1		D12	A20	<b> </b>	<b>I</b>	<b> </b>	<b> </b>					<b>—</b>
	1	VCCIO7	<b>†</b>		1	D15	D12	A24							<u> </u>		<u> </u>
	1	VCCIO7	1	+	-	נוט	D14	A24 A27	<del> </del>	<del> </del>	<del> </del>	t			1	<del> </del>	<del></del>
	<del>                                     </del>	VCCIO7	1	1	-	1		E16	<del> </del>	+	<del> </del>	<del> </del>	1		1	<del> </del>	<del>                                     </del>
	-		<del>                                     </del>		+	1	סוט		-	-	-	<b>-</b>			-	-	<del></del>
	1	VCCIO7	<del>                                     </del>	+	-	+		E20	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>			1	<del>                                     </del>	<del></del>
	1	VCCIO7	1		+	1	-	E23	-	-	-	-	ļ			<del>                                     </del>	<del></del>
	I	VCCIO7	1			1		H18	1	1	l	1		L		1	1



Bank	VREFB	Pin Name /	Optional	Configuration	0240	F324	F484 /	F720	DOS for Ye/Yo :	DOS for Ye/Yo :-	DOS for Y16/V19 :	DOS for Ye/Yo :-	DOS for ¥16/¥19 :	DOS for Y22/Y26 :	DOS for Ye/Yo :	DOS for ¥16/¥19 :	DOS for Y22/Y26
Sank Number	Group	Function	Function(s)	Function	Q240	F324	U484	F/80	DQS for X8/X9 III	F324	F324	F484/11484	F484/11484	F484/11484	F780	DQS for X16/X18 in F780	F780
unibei	Group	unction	i unction(s)	i dilction			0404		Q240	1 324	1 324	1 404/0404	1 404/0404	1 404/0404	1700	1 700	1700
		VCCIO7						J15									
		VCCIO8				D4	A2	A2									
		VCCIO8				D6		A5									
		VCCIO8				D8		A9									
		VCCIO8					D11	A13									
		VCCIO8					E8	E6									
		VCCIO8						E9									
		VCCIO8						E13									
		VCCIO8						H11									
		VCCIO8						J13									
		GND				G9	L10	K10									
		GND				H9		K12									
		GND				H8	M10	K14									
		GND				J8	M11	K18									
		GND				J9	L12	K20									
		GND			+	J10	L13	L11									
		GND				H10	M12	L15			-						
	<b> </b>	GND	1		+		M13	L15	1		<del> </del>				<del> </del>		<del>                                     </del>
		GND	-	-	+	H11 J11	M13 N11	L17 L19	-		-				-		<del> </del>
	<del>                                     </del>		<del> </del>	+	+				-		<b>_</b>				<del> </del>		<del> </del>
	ļ	GND				K11	K11	L9									
		GND				K10	N12	M10									
		GND				K9		M12									
		GND				K8		M14									
		GND				L8		M16									
		GND				L9	N10	M18									
		GND				L10	K10	N11									
		GND				M10	J9	N13									
		GND				L11	F12	N15									
		GND				F11		N17									
		GND				F13	H13	N19									
		GND				F7	J15	P10									
		GND				F9	K16	P12									
		GND				G6	L15	P14									
		GND				M13	N15	P16									<b>†</b>
		GND				N10	R13	P18			-						
		GND				N12	R11	P20			-						
	-	GND					R9	R11									
						N6					-						
		GND			-	N8	P8	R13									
		GND				1		R15									
		GND				1		R17									
		GND						R19									
		GND						R9									
		GND						T10									
		GND						T12									
		GND						T14									
		GND						T16									
		GND						T18									
		GND						U11									
		GND				1		U13									
		GND			1	1		U15		İ	İ	İ	İ		İ		
		GND		1	1	1		U17							<u> </u>		
		GND	1	1	1	1		U19	1	1	†	1	1	1	1	1	1
	<del>                                     </del>	GND	1	+	+	+	<b>-</b>	V10	1	-	<del>†                                      </del>	-		<del> </del>	<del>                                     </del>	<del> </del>	<del></del>
	<b> </b>	GND	1		+	1		V10	1		<del> </del>				<del> </del>		+
	<b> </b>	GND	1		+	1		V12	1		<del> </del>				<del> </del>		+
			-	-	+	1					<del>                                     </del>				<del>                                     </del>		
	ļ	GND	1	1	-	1		V18	1	-	1	-	-	1	1	1	<del>                                     </del>
	ļ	GND			4	1		W11			L				L		
		GND				1		W15			ļ			ļ	ļ		
		GND				1		W17									
		GND						W19									
		GND				C15	A1	AA2									
		GND				C13		AA27									
		GND				C11		AC6									
	1	GND	1			C8		AC9									

Notes (1), (2), (3)

Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DOS for X8/X9 in	DOS for X8/X9 in	DOS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DOS for X32/X36 in	DQS for X8/X9 in	DOS for X16/X18 in	DOS for X32/X36
Number	Group	Function	Function(s)	Function	4240	. 524	U484	30	Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	DQS for X16/X18 in F780	F780
								1			l /				1	[ ]	
		GND			_	C6		AC13									
		GND				C4	C14	AC16									
		GND				E3	C16	AC20									
		GND				G3	A22	AC23									
		GND				J3	E20	AF1									
		GND				K3	G20	AF28									
		GND				N3	L20	AG2									
		GND				P3	P19	AG5									
		GND				T5	V20	AG9									
		GND				T7	Y20	AG13									
		GND				T9	AB22	AG16									
		GND				T10	Y18	AG20									
		GND				T12	Y16	AG24									
		GND				T15	Y12	AG27									
		GND			-	P16	Y11	B2									
	<del> </del>	GND	†	+	+	M16	Y9	B5	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>			<del>                                     </del>		<del>                                     </del>	<del> </del>
	1	GND	<del>                                     </del>	+	+-	М16 J16	Y9 Y5	B9	-	-	-			-	-	-	-
	1				-												
	<del>                                     </del>	GND GND		_	-	K16	AB1	B13	-	-	-		ļ	-			-
					_	G16	N3	B16									
		GND	<u> </u>			E16	U3	B20									
		GND					W3	B24									
		GND					D3	B27									
		GND					F3	C1									
		GND					K3	C28									
		GND					H3	F6									
		GND					R3	F9									
		GND					AB6	F13									
		GND					Y15	F16									
		GND					T20	F20									
		GND					J19	F23									
		GND					C18	H2									
		GND					D8	H27									
	<u> </u>	GND	1		-		DO	J11			-			-		<u> </u>	
	<u> </u>	GND	1		-			J18			-			-		<u> </u>	
	1	GND			-			K6									
	1				-												
		GND			_			K16									
		GND						K23									
		GND	<u> </u>					L13									
		GND						M20									
		GND						N2									
		GND						N6									
		GND						N9									
		GND						N23									
		GND						N27									
		GND						T2									
		GND						T6									
	İ	GND			1			T20									
	İ	GND			1			T23	1		1			1			
	1	GND	1	1	1			T27	<u> </u>	1							1
	1	GND	1	+	+			U9	<b> </b>		<b> </b>			<b> </b>			1
	1	GND	+	+	+			V16	<del> </del>	1	<del> </del>	1	1	<del> </del>	1	<del> </del>	1
	1	GND	<del> </del>	+	+-	$\vdash$		W6	<del>                                     </del>	-	<del>                                     </del>	-		<del>                                     </del>	-	<del> </del>	-
	<b> </b>		<del>                                     </del>	+	+				<del>                                     </del>	-	<del>                                     </del>			<del>                                     </del>	-	<del>                                     </del>	-
	1	GND	<b></b>	+				W13									
		GND			4			W23									
		GND	1					Y11									
	1	GND				ĺ		Y18									

## Notes:

- (1) DQS pins that do not have the associated DQ pins are not supported.
- (1) But p pin or n pin is not available for the package, the particular differential pair is not supported.

  (3) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

  (3) If dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the core logic.

  (4) Q240 in the EP3C40 device does not have the MSEL[3] pin and does not support the Active Parallel (AP) configuration mode.



## Pin Information for the Cyclone<sup>®</sup> III EP3C40 Device Version 1.4 Note (1)

		Note (1)						
D: 11	Pin Type (1st, 2nd, and							
Pin Name	3rd Function)	Pin Description						
VOODIT	- In	Supply and Reference Pins						
VCCINT	Power	These are internal logic array voltage supply pins.						
		These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and						
		output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI, and TDO) and the following configuration pins: nCONFIG,						
VCCIO[18]	Power	DCLK, DATA[150], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.						
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.						
		Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced						
VREFB[18]N[03]	I/O	pins for the bank. If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins.						
VCCA[14]	Power	Supply (analog) voltage for PLLs[14] and other analog circuits in the device.						
VCCD_PLL[14]	Power	Supply (digital) voltage for PLLs[14].						
		Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RUP must be connected to the						
RUP[14]	I/O, Input	designated RUP pin within the same bank. If not required, this pin is a regular I/O pin.						
		Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RDN must be connected to the						
RDN[14]	I/O, Input	designated RDN pin within the same bank. If not required, this pin is a regular I/O pin.						
GNDA[14]	Ground	Ground for PLL[14]. You can connect these pins to GND plane on the board.						
NC	No Connect	Do not drive signals into these pins.						
		Dedicated Configuration/JTAG Pins						
		Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0						
	Input (PS, FPP, AS)	has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or						
	Bidirectional open drain	PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration,						
DATA0	(AP)	DATA0 is a dedicated bidirectional pin with optional user control.						
		Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller						
MSEL[30]	Input	devices or package options do not support the AP flash programming and do not have the MSEL[3] pin.						
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.						
		Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and						
		tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. The input buffer on this pin supports hysteresis using Schmitt						
nCONFIG	Input	trigger circuitry.						
		This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all						
	Bidirectional	configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high						
CONF_DONE	(open-drain)	after all data is received. Then the device initializes and enters user mode.						
		This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a						
	Bidirectional	status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS						
nSTATUS	(open-drain)	is driven low by an external source during configuration or initialization.						
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.						
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.						
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.						
TDO	Output	Dedicated JTAG output pin.						
		Clock and PLL Pins						
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[07]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.						
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[07]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.						
==: \(\frac{1}{2}\	2.2500,p.00	WO pins that be used as two single-ended clock output pins or one differential clock output pair. These pins can only use the differential I/O						
PLL[14]_CLKOUT[p,n]	I/O, Output	standard if it is being fed by a PLL output.						
[ <u>-</u>		Optional/Dual-Purpose Configuration Pins						
		Configuration clock pin. In PS and PP configuration modes, DCLK is used to clock configuration data from an external source into the Cyclone III						
	Input (PS. FPP)	device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. After AS or AP						
DCLK	I/O, Output (AS, AP)	configuration, this pin is available as a user I/O pin with optional user control.						
nCEO								
IICEO	I/O, Output	Output that drives low when device configuration is complete.						



## Pin Information for the Cyclone<sup>®</sup> III EP3C40 Device Version 1.4 Note (1)

Bidirectional open-drain DATA1, ASDO (AP)  Input (FPP) Input (FPP) Bidirectional open-drain (AP)  Data inputs, Byte-wide or word-wide configuration as user I/O pins during configuration, which means they are tri-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.  After FPP configuration, DATA[7.2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.  After FPP configuration, DATA[7.2] are dedicated bidirectional pins with optional user control.  Bidirectional open-drain DATA[15.8] (AP)  After AP configuration, DATA[7.2] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[7.3]  After AP configuration, DATA[7.3]  After AP configuration, DATA[15.0]  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  (AP)  After AP configuration, DATA[15.0]  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  (AP)  APDD[23.0]  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  AP configuration, DATA[15.0]  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  APD configuration, DATA[15.0]  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  APP and page and the approach of the parallel flash in AP mode.  In Q, Output (AP)  Active-low address valid output, Driving the nAVED pin low during read or write operation indicates to the parallel flash that valid address is pres on the PADD[23.0] address bus.  Active-low write enable to the parallel flash. Driving the nAVE pin low during write operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.  Active-low write en	Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
FLASH_nCE, nCSO  IVO, Output  FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.  This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode.  DATA1 Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7.0] or DATA[15.0] respectively.  In PS configuration, DATA1 as understand the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA1 is a deficiated bidirectional pin with optional user control.  Input (FPP)  Output (AS)  Bidirectional open-drain  (AP)  DATA[7.2]  DATA[7.2]  DATA[7.2]  DATA[7.2]  DATA[7.3]  DATA[8.8]  (AP)  DATA[8.9]  DATA[8.9]  DATA[8.9]  DATA[8.9]  DATA[8.9]  DATA[9.9]  DATA[8.9			This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active.
This pir functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode.  DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7.0] or DATA[15.0] in participation. DATA1 in participation as user I/O pin adding configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin adding configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin adding configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin adding configuration, which means it is tri-stated. After FPP configuration, DATA1 is a dedicated bidirectional pin with optional user control.  DATA1, ASDO  DATA1, ASDO  (AP)  DATA1, ASDO  (AP)  DATA1, ASDO  (AP)  DATA1, ASDO  DATA1, ASDO  (AP)  DATA1, ASDO  (AP)  DATA1, ASDO  (AP)  DATA1, ASDO  DATA1, ASDO  DATA1, ASDO  (AP)  Bidirectional open-drain  (AP)  DATA1, ASDO  DATA1, ASDO  DATA1, ASDO  DATA1, ASDO  (AP)  Bidirectional open-drain  (AP)  DATA1, ASDO  DATA			nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device.
DATA!: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7.0] or DATA[15.0]. In PS configuration scheme, DATA! functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA! is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA! is a dedicated bidirectional pin with optional user control.  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  ADATA! ASDO  Data inputs. Byte-wide or word-wide configuration device in AS mode used to read out configuration data. In AS mode this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.  ADATA! ASDO  ADATA! ASDO  Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7.0] or DATA[15.0] respectively. In AS or PS configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tim-stated.  After FPP configuration, DATA[7.2] are available as user I/O pins user to the partie of the state of these prints are times to the partie of the state of these prints are times to the partie of the state of these prints are times to the partie of the state of these prints are times to the partie of the st	FLASH_nCE, nCSO	I/O, Output	FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.
In PS configuration, DATA1 is available as a user I/O pin during configuration, which means it is tri-stated.  After PFP configuration, DATA1 is available as a user I/O pin during configuration, which means it is tri-stated.  After AP configuration, DATA1 is available as a user I/O pin during on the state of this pin depends on the Dual-Purpose Pin settings.  After AP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings.  After AP configuration, DATA1 is available as user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings.  ASDO. Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode user I/O pin series in ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.  DATA1, SSDO. In AS or RS configuration of the pin series I/O pin series I/O pin series I/O pin series I/O pin series I/O pin series I/O pin series I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.  After AP configuration, DATA1, 22 are dedicated incentional pins with optional user control.  DATA1, SSD. In PS, FSPP or AS configuration scheme, they intendericental pins with optional user control.  After AP configuration, DATA1, 22 are dedicated before the series device on DATA15, 0) in PS, FSPP or AS configuration scheme, they notice into with expensive to the target device on DATA15, 0) in PS, FSPP or AS configuration scheme, they intendericental pins with optional user control.  After AP configuration, DATA11, SSD are dedicated bidirectional pins with optional user control.  After AP configuration, DATA11, SSD, are dedicated bidirectional pins with optional user control.  After AP configuration, DATA11, SSD, are dedicated bidirectional pins with optional user control.  After AP configuration, DATA11, SSD, are dedicated bidirectional pins with optional user contr			This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode.
After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control.  ASDC Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.  DATA1, ASDO  Input (FPP) Bidirectional open-drain DATA[7.2]  ASD PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  After FP configuration, DATA[7.2] are available as user I/O pins during configuration, which means they are tri-stated.  After FPP configuration, DATA[7.2] are deviable configuration with optional user control.  DATA[15.8]  Bidirectional open-drain (AP)  Bidirectional			respectively.  In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated.
ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode Bidirectional open-drain the ASDO in has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.  Data injust. Byte-wide or word-wide configuration data is presented to the target device on DATA[70] or DATA[150] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[72] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings. After FPP configuration, DATA[72] are available as user I/O pins during output user control.  After FPP configuration, DATA[72] are available as user I/O pins during output option in the Dual-Purpose Pin settings. After FPP configuration DATA[150] Data in plus. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data plus. Byte-wide or word-wide configuration data is presented to the target device on DATA[150] Data Plus Plus Plus Plus Plus Plus Plus Plus			
Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7.0] or DATA[15.0] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After PP configuration, DATA[7.2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings. After AP configuration, DATA[7.2] are declicated bidirectional pins with optional user control.  Data inputs. Bips-wide or word-wide configuration data is presented to the target device on DATA[15.0]. Bidirectional open-drain after AP configuration, DATA[15.2] are declicated bidirectional pins with optional user control.  DATA[15.8] (AP)  Bidirectional open-drain and inputs. Bips-wide or word-wide configuration data is presented to the target device on DATA[15.0]. In PS, FPP, or AS configuration, DATA[15.0] is presented to the target device on DATA[15.0]. In PS, FPP, or AS configuration, DATA[15.0] is presented to the target device on DATA[15.0]. In PS, FPP, or AS configuration, DATA[15.0] is presented by the target device on DATA[15.0]. In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15.0] is presented by the target declicated bidirectional pins with optional user control.  PADD[23.0] I/O, Output (AP)  Active-low present the Cyclone III device to the parallel flash in AP mode.  Active-low address valid output. Driving the nRESET pin low during read or write operation indicates to the parallel flash that valid address is presented to the parallel flash (DATA[15.0]) is a control of the PADD[23.0] address bus.  NOE  I/O, Output (AP)  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.  Active-low output enable to the parallel flash. Driving the nOE pin low during with operation indicates to the parallel flash that da		Output (AS)	ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user
Input (FPP) In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  After FPP configuration, DATA[72] are addicated bidirectional prins with optional user control.  Data inputs. Biye-wide or word-wide configuration as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.  After AP configuration, DATA[72] are addicated bidirectional prins with optional user control.  Data inputs. Biye-wide or word-wide configuration data is presented to the target device on DATA[150].  DATA[158] (AP)  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  After AP configuration, DATA[158] are dedicated bidirectional prins with optional user control.  PADD[230] I/O, Output (AP)  Active-low reset output. Driving the nAVD pin low designs in AP mode.  Active-low address bus from the Cyclone III device to the parallel flash in AP mode.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is pres on the PADD[230] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low output enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]) and the parallel flash outputs (DATA[150]) and the parallel flash outputs (DATA[150]) and DATA[150] bus is valid.  Active-	DATA1, ASDO	(AP)	
DATA[72] (AP) After AP configuration, DATA[72] are dedicated bidirectional pins with optional user control.  Data inputs. Blye-wide or word-wide configuration data is presented to the target device on DATA[150].  In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  After AP configuration, DATA[158] are dedicated bidirectional pins with optional user control.  PADD[230] I/O, Output (AP) Active-low reset output. Driving the nAVD pin low during read or write operation indicates to the parallel flash in AP mode.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is pres on the PADD[230] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the UO, Output (AP) DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the NOE of the parallel flash outputs flash that data on the CRC_ERROR  I/O, Output (AP)  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the NOE of the parallel flash that data on the CRC_ERROR		. , ,	In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.
Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15.0].  Bidirectional open-drain (AP) After AP configuration, DATA[15.8] (AP) After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.  After AP configuration, DATA[15.0] and the value of the parallel flash in AP mode.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is preson the PADD[23.0] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash that valid address is preson the PADD[23.0] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that valid address is preson the PADD[23.0] address bus.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that valid address is presonable in the OE pin low during write operation indicates to the parallel flash that valid address i	DATA[72]		
DATA[158] (AP) After AP configuration, DATA[158] are dedicated bidirectional pins with optional user control.  PADD[230] I/O, Output (AP) 24-bit address bus from the Cyclone III device to the parallel flash in AP mode.  RESET I/O, Output (AP) Active-low reset output. Driving the nRESET pin low resets the parallel flash.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is pres on the PADD[230] address bus.  NOE I/O, Output (AP) Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low reare and the parallel flash. Driving the nOE pin low during read or write operation enables. The Davallary and the parallel flash outputs (DATA[150]).  Active-low reare and parallel flash. Driving the nOE pin low during read or write operation indicates to the parallel flash. Driving the nOE pin low during read or write operation indicates to the parallel flash. Driving the nOE pin low during		,	
PADD[230]  I/O, Output (AP)  Active-low reset output. Driving the nRESET pin low resets the parallel flash.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is pres on the PADD[230] address bus.  NOE  I/O, Output (AP)  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-lop write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that valid address is pres  Active-low write enabled to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that valid address is pres  Active-low write enabled to the parallel flash. Driving the nWE pin low during write operation indicates wh		Bidirectional open-drain	In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.
Active-low reset output. Driving the nRESET pin low resets the parallel flash.  Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is preson the PADD[230] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation enables the parallel flash that valid address is preson the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash that valid address is preson the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash that valid address is preson the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash that valid address is preson the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving enables the parallel flash. Driving in the Configuration index enables the parallel flash. Driv	DATA[158]		
Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is preson the PADD[230] address bus.  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nOE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is us when the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.  Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; whis pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation. This pin is enabled by turning on the Enable device-wide output enable (DEV_OC) option in the Quartus II software.  DEV_OE  IND (when option off), Input (when option on)  IVO, Output (when option on)  IVO, Output (when option on)  IVO, Output (when option on)  IVO, Output (when option on)  IVO, Output (open-drain)  IVO, Output (open-drain)  IVO, Output (open-drain)  Optional unit allows you to override all tri-states on the device. When this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins are tri-stated; when this pin is driven low, all Vo pins	PADD[230]	, 1 ( )	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.
nAVD  I/O, Output (AP)  on the PADD[230] address bus.  I/O, Output (AP)  Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).  Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is us Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is us When the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.  Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; we this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins are tri-stated; when this pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.  This is a dual-purpose sta	nRESET	I/O, Output (AP)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.
Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[150] bus is valid.  Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is us when the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.  Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; withis pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation line in the Quartus II software.  Optional pin that allows you to override all tri-states on the device-wide reset (DEV_CLRn) option in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven low, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.  This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE bin cannot be used as a user I/O pin alter configuration. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option.	nAVD	I/O, Output (AP)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[230] address bus.
nWE I/O, Output (AP) DATA[150] bus is valid.  Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is us when the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.  Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; withis pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.  This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option.	nOE	I/O, Output (AP)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150]).
CRC_ERROR  I/O, Output  when the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.  Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; we this pin is driven low, all registers are cleared; we this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.  This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.  Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	nWE	I/O, Output (AP)	
Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; we this pin is driven low, all registers are cleared; we this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operation. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.  This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.  Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	CRC ERROR	I/O. Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled. This pin can be set in Quartus II software to support open-drain output.
DEV_CLRn  Input (when option on)  This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.  Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in to Quartus II software.  This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.  Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option			Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when
I/O (when option off), Input (when option on)  DEV_OE  Input (when option on)  I/O, Output  INIT_DONE  Initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	DEV_CLRn	Input (when option on)	This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.  Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	DEV OF		Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software
INIT_DONE (open-drain) pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.  Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	DEV_01		This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at
Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option	INIT DONE		
	THE STATE OF THE S	(open drain)	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied
ICLINIOSE I/O INDUIT IIDE QUARIUS II SOUWARE	CLKUSR	I/O, Input	Ithe Quartus II software.



## Pin Information for the Cyclone<sup>®</sup> III EP3C40 Device Version 1.4 Note (1)

		Note (1)
	Pin Type (1st, 2nd, and	
Pin Name	3rd Function)	Pin Description
		Dual-Purpose Differential and External Memory Interface Pins
DIFFIO_[L,R,T,B][061][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[05][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCL K[011]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQS[05][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPC	I/O, DQS/CQ, CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
LK[07] DQ[05][L,R,T,B]	I/O, DQ	Optional data signal for use in external memory interfaces.
	,	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results
DM[05][L,R,B,T][01]/BWS#[05][L,R,T,B]	I/O, DM/BWS#	in the memory masking the DQ signals.

#### Note:

(1) The pin definitions are prepared based on the device with the largest density, EP3C120. Refer to the pin list for the availability of pins in each density.



PI	_L3	VREFB8N3	VREFB8N2	VREFB8N1	VREFB8N0	VREFB7N3	VREFB7N2	VREFB7N1	VREFB7N0	PI	.L2
			B8				В	7		' -	
VREFB1N0											VREFB6N0
VREFB1N1	<del>-</del>									9	VREFB6N1
VREFB1N2	B1									B6	VREFB6N2
VREFB1N3											VREFB6N3
VREFB2N0											VREFB5N0
VREFB2N1	B2									B5	VREFB5N1
VREFB2N2	ш									E	VREFB5N2
VREFB2N3											VREFB5N3
PL	_L1		В				ı	4	I	PL	.L4
		VREFB3N3	VREFB3N2	VREFB3N1	VREFB3N0	VREFB4N3	VREFB4N2	VREFB4N1	VREFB4N0		

#### Notes:

- 1. This is a top view of the silicon die.
- 2. This is only a pictorial representation to get an idea of placement on the device.

Refer to the pin list and the Quartus® II software for exact locations.



Version Number	Changes Made	Date
1.0	Initial release.	9/7/2007
1.1	Updated Note(2) in Pin List.	1/4/2008
1.2	Updated pin function for CRC_ERROR pin.	5/23/2008
	Updated DQ/DQS support for UBGA package.	
	Updated pin function for PLL[14]_CLKOUT[p,n] pin.	
	Remove RDY from pin list and pin definitions.	
	Incorporated pin connection guideline into Pin Definitions worksheet.	
	Incorporated VCCA and VCCD Decoupling recommendations.	
1.3	Changed VREFB[18]N[02] to VREFB[18]N[03] in Pin Definitions.	5/7/2009
1.4	Removed Pin Connection Guideline from Pin Definitions worksheet.	10/7/2009
	Removed VCCA and VCCD Decoupling recommendations.	
	Removed PKG notes from Pin List Worksheet.	
	Updated pin function for DCLK pin.	
	Added new note in Pin List.	