Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B1	VREFB1N0	VCCD_PLL3			1	B2	1	D4	F6								
B1	VREFB1N0	GNDA3			2	B1	2	E5	F5								
B1	VREFB1N0	VCCA3			3	A1	3	F5	G6								
B1	VREFB1N0	IO					4		H5								
B1	VREFB1N0	IO	DIFFIO_L1p				5		B2						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L1n				6		B1						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	VCCIO1					7										
B1	VREFB1N0	IO							G5								
B1	VREFB1N0	GND					8										
B1	VREFB1N0	IO	DIFFIO_L2p	nRESET					E4						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L2n						E3						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L3p		4	C1	9	B1	C2			DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0
B1	VREFB1N0	VCCINT			5		10										
B1	VREFB1N0	IO	DIFFIO_L3n						C1						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	GND					11										
B1	VREFB1N0	IO	DIFFIO_L4p					C2	D2						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L4n	DATA1, ASDO	6	D2	12	C1	D1								
B1	VREFB1N0	IO	VREFB1N0		7	D1	13	F3	H7								
B1	VREFB1N0	IO	DIFFIO_L5p						H6						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L5n						J6						DQ2L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L6p	FLASH_nCE, nCSO	8	E1	14	D2	E2								
B1	VREFB1N0	IO	DIFFIO_L6n					D1	E1							DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L7p						F2						DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0
B1	VREFB1N0	IO	DIFFIO_L7n						F1						DQ0L	DQ1L	DQ1L
B1	VREFB1N0	IO	DIFFIO_L8p						G4								
B1	VREFB1N0	IO	DIFFIO_L8n						G3								
B1	VREFB1N1	VCCIO1					15										
B1	VREFB1N1	GND					16										
B1	VREFB1N1	nSTATUS		nSTATUS	9	E2	17	F4	K6								
B1	VREFB1N1	IO	DIFFIO_L9p				18		L8								
B1	VREFB1N1	IO	DIFFIO_L9n					G5	K8								
B1	VREFB1N1	IO	DIFFIO_L10p				19	F2	J7								
B1	VREFB1N1	IO	DIFFIO_L10n				20	F1	K7								
B1	VREFB1N1	IO			10	F2	21	G2	J4	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0
B1	VREFB1N1	IO	DIFFIO_L11p						H2						DQ0L	DQ1L	DQ1L
B1	VREFB1N1	IO	DIFFIO_L11n						H1						DQ0L	DQ1L	DQ1L
B1	VREFB1N1	IO	VREFB1N1		11	F1	22	G1	J3								
B1	VREFB1N1	IO	DIFFIO_L12p						J2						DQ0L	DQ1L	DQ1L
B1	VREFB1N1	IO	DIFFIO_L12n						J1						DQ0L	DQ1L	DQ1L
B1	VREFB1N1	DCLK		DCLK	12	F3	23	H1	K2								
B1	VREFB1N1	IO		DATA0	13	G1	24	H2	K1								
B1	VREFB1N1	nCONFIG		nCONFIG	14	G2	25	H5	K5								
B1	VREFB1N1	TDI		TDI	15	G3	26	H4	L5								
B1	VREFB1N1	TCK		TCK	16	H2	27	H3	L2								
B1	VREFB1N1	VCCIO1			17												
B1	VREFB1N1	TMS		TMS	18	H1	28	J5	L1								
B1	VREFB1N1	GND			19												
B1	VREFB1N1	TDO		TDO	20	H3	29	J4	L4								
B1	VREFB1N1	nCE		nCE	21	H4	30	J3	L3								
B1	VREFB1N1	CLK0	DIFFCLK_0p		22	J2	31	E2	G2								
B1	VREFB1N1	CLK1	DIFFCLK_0n		23	J1	32	E1	G1								
B2	VREFB2N0	CLK2	DIFFCLK_1p		24	K3	33	M2	T2								
B2	VREFB2N0	CLK3	DIFFCLK_1n		25	J3	34	M1	T1								
B2	VREFB2N0	IO	DIFFIO_L13p						L6						DQ0L	DQ1L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L13n						M6						DQ0L	DQ1L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L14p					J2	M2				DQ1L		DQ0L	DQ1L	DQ1L
B2	VREFB2N0	VCCIO2			26		35										
B2	VREFB2N0	IO	DIFFIO_L14n					J1	M1				DQ1L			DQ1L	DQ1L
B2	VREFB2N0	GND			27		36										
B2	VREFB2N0	IO	DIFFIO_L15p						M4						DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1
B2	VREFB2N0	IO	DIFFIO_L15n						M3						DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L16p					K6	N2						DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L16n				37	L6	N1			DQ1L			DQ1L	DQ3L	DQ1L

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B2	VREFB2N0	IO					38		L7			DQ1L					
B2	VREFB2N0	IO	VREFB2N0		28	K1	39	L3	M5								
B2	VREFB2N0	IO	DIFFIO_L17p						P2						DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L17n						P1						DQ1L	DQ3L	DQ1L
B2	VREFB2N0	VCCINT			29		40										
B2	VREFB2N0	IO	DIFFIO_L18p				41		R2			DQ1L			DQ1L	DQ3L	DQ1L
B2	VREFB2N0	GND					42										
B2	VREFB2N0	IO	DIFFIO_L18n				43	K1	R1			DQ1L	DQ1L		DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO							N5						DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L19p		30	L2	44	L2	P4	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1
B2	VREFB2N0	IO	DIFFIO_L19n			K2	45	L1	P3			DQ1L	DQ1L		DQ1L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L20p						U2						DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2
B2	VREFB2N0	IO	DIFFIO_L20n						U1						DQ3L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L21p						V2						DQ3L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L21n						V1						DQ3L	DQ3L	DQ1L
B2	VREFB2N0	IO							P5								
B2	VREFB2N0	IO	DIFFIO_L22p						N6						DQ3L	DQ3L	DQ1L
B2	VREFB2N0	IO	DIFFIO_L22n						M7								
B2	VREFB2N1	IO	DIFFIO_L23p						M8								
B2	VREFB2N1	IO	DIFFIO_L23n						N8								
B2	VREFB2N1	IO	DIFFIO_L24p						W2						DQ3L	DQ3L	DQ1L
B2	VREFB2N1	IO	DIFFIO_L24n						W1						DQ3L	DQ3L	DQ1L
B2	VREFB2N1	IO	DIFFIO_L25p						Y2						DQ3L	DQ3L	DQ1L
B2	VREFB2N1	IO	DIFFIO_L25n						Y1						DQ3L	DQ3L	DQ1L
B2	VREFB2N1	IO	VREFB2N1		31	L1	46	K2	T3								
B2	VREFB2N1	IO	DIFFIO_L26p						N7								
B2	VREFB2N1	VCCIO2					47										
B2	VREFB2N1	IO	DIFFIO_L26n						P7								
B2	VREFB2N1	GND					48										
B2	VREFB2N1	IO	DIFFIO_L27p				49	N2	AA2			DQ1L	DQ1L				
B2	VREFB2N1	IO	DIFFIO_L27n				50	N1	AA1				DQ1L		DQ3L	DQ3L	DQ1L
B2	VREFB2N1	IO	RUP1		32	M1	51	K5	V4			DQ1L	DQ1L				
B2	VREFB2N1	IO	RDN1		33	M2	52	L4	V3			DQ1L	DQ1L				
B2	VREFB2N1	IO	DIFFIO_L28p						P6								
B2	VREFB2N1	VCCINT			34		53										
B2	VREFB2N1	IO	DIFFIO_L28n						R5								
B2	VREFB2N1	GND					54										
B2	VREFB2N1	IO					55	R1	T4			DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1
B2	VREFB2N1	IO	DIFFIO_L29p				56	P2	T5				DQ1L		DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3
B2	VREFB2N1	IO	DIFFIO_L29n				57	P1	R6			DQ1L	DM1L/BWS#1L				
B2	VREFB2N1	IO	DIFFIO_L30p						R7								
B2	VREFB2N1	IO	DIFFIO_L30n						T7								
B2	VREFB2N1	IO	DIFFIO_L31p						P8								
B2	VREFB2N1	IO	DIFFIO_L31n						R8								
B2	VREFB2N1	VCCA1			35	R1	58	L5	T6								
B2	VREFB2N1	GNDA1			36	P1	59	M5	U5								
B2	VREFB2N1	VCCD_PLL1			37	P2	60	N4	U6								
B3	VREFB3N1	IO	DIFFIO_B1p						R9								
B3	VREFB3N1	IO	DIFFIO_B1n						T8								
B3	VREFB3N1	IO	DIFFIO_B2p						R10								
B3	VREFB3N1	IO	DIFFIO_B2n						T9								
B3	VREFB3N1	VCCINT			38		61										
B3	VREFB3N1	IO	DIFFIO_B3p					N3	V6								
B3	VREFB3N1	GND					62										
B3	VREFB3N1	IO	DIFFIO_B3n					P3	V5				DM3B/BWS#3B	DM5B1/BWS#5B1	DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3
B3	VREFB3N1	IO	DIFFIO_B4p						U7								
B3	VREFB3N1	IO	DIFFIO_B4n					R3	U8				DQ3B	DQ5B			
B3	VREFB3N1	IO	VREFB3N1		39	R3	63	T3	Y4								
B3	VREFB3N1	IO	DIFFIO_B5p						R11								
B3	VREFB3N1	IO	DIFFIO_B5n				64		R12								
B3	VREFB3N1	IO	DIFFIO_B6p				65		Y3						DQ3B	DQ3B	DQ5B
B3	VREFB3N1	VCCIO3			40		66										
B3	VREFB3N1	GND			41		67										

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B3	VREFB3N1	IO			42	R4	68	T2	Y6	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2
B3	VREFB3N1	IO	PLL1_CLKOUTp		43	P5	69	R4	AA3								
B3	VREFB3N1	IO	PLL1_CLKOUTn		44	R5	70	T4	AB3								
B3	VREFB3N1	IO	DIFFIO_B7p				71	N5	W6				DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B7n				72	N6	V7				DQ3B	DQ5B			
B3	VREFB3N1	IO	DIFFIO_B8p				73	M6	AA4				DQ3B	DQ5B	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B8n						AB4								
B3	VREFB3N1	VCCINT			45		74										
B3	VREFB3N1	IO	DIFFIO_B9p						AA5						DQ3B	DQ3B	DQ5B
B3	VREFB3N1	GND					75										
B3	VREFB3N1	IO	DIFFIO_B9n						AB5								
B3	VREFB3N1	IO	DIFFIO_B10p						W7						DQ3B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B10n						Y7						DQ3B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B11p						U9						DQ3B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B11n						V8						DQ3B	DQ3B	DQ5B
B3	VREFB3N0	IO							W8						DQ3B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B12p						AA7						DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2
B3	VREFB3N0	IO	DIFFIO_B12n						AB7						DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B13p						Y8						DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B13n			P6											
B3	VREFB3N0	IO	VREFB3N0		46	N5	76	P6	V9								
B3	VREFB3N0	VCCIO3			47		77										
B3	VREFB3N0	IO					78	M7	V10			DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2
B3	VREFB3N0	GND			48		79										
B3	VREFB3N0	IO	DIFFIO_B14p					R5	T10				DQ3B	DQ5B			
B3	VREFB3N0	IO	DIFFIO_B14n				80	T5	U10			DM5B/BWS#5B			DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B15p				81	R6	AA8			DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B15n				82	T6	AB8			DQ5B			DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO						L7	T11				DQ3B	DQ5B			
B3	VREFB3N0	IO	DIFFIO_B16p					R7	AA9				DQ3B	DQ5B	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B16n				83	T7	AB9			DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3
B3	VREFB3N0	IO			49	R6	84	L8	U11	DQ1B	DQ1B		DQ3B	DQ5B			
B3	VREFB3N0	IO	DIFFIO_B17p				85		V11						DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B17n				86		W10						DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B18p		50	R7	87	M8	Y10	DQ1B	DQ1B	DQ5B	DM5B/BWS#5B	DM5B0/BWS#5B0	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B18n		51	P7	88	N8	AA10	DQ1B	DQ1B	DQ5B	DQ5B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1
B3	VREFB3N0	IO						P8	AB10				DQ5B	DQ5B		DQ5B	DQ5B
B3	VREFB3N0	CLK15	DIFFCLK_6p		52	N6	89	R8	AA11								
B3	VREFB3N0	CLK14	DIFFCLK_6n		53	N7	90	T8	AB11								
B4	VREFB4N1	CLK13	DIFFCLK_7p		54	P8	91	R9	AA12								
B4	VREFB4N1	CLK12	DIFFCLK_7n		55	R8	92	T9	AB12								
B4	VREFB4N1	IO	DIFFIO_B19p				93	K9	AA13			DQ5B			DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B19n				94	L9	AB13			DQ5B			DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B20p					M9	AA14						DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B20n				95	N9	AB14				DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N1	VCCIO4			56		96										
B4	VREFB4N1	IO							V12								
B4	VREFB4N1	GND			57		97										
B4	VREFB4N1	IO	DIFFIO_B21p		58	R9	98	R10	W13	DQ1B	DQ1B	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B21n				99	T10	Y13			DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4
B4	VREFB4N1	IO	DIFFIO_B22p		59	N8	100	R11	AA15	DQ1B	DQ1B	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B22n		60	P9	101	T11	AB15	DQ1B	DQ1B				DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B23p		61	N10	102	R12	U12				DQ5B	DQ5B	DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B23n				103		T12			DQ5B					
B4	VREFB4N1	IO	DIFFIO_B24p					T12	AA16				DQ5B	DQ5B	DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0
B4	VREFB4N1	IO	DIFFIO_B24n					K10	AB16						DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B25p						AA17								
B4	VREFB4N1	VCCIO4			62		104										
B4	VREFB4N1	IO	DIFFIO_B25n						AB17								
B4	VREFB4N1	GND			63		105										
B4	VREFB4N1	IO						L10	R13								

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B4	VREFB4N1	IO			64	P10	106	P9	V13			DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5
B4	VREFB4N1	IO	VREFB4N1		65	R10	107	N12	W14								
B4	VREFB4N0	IO	DIFFIO_B26p			N11	108	R13	U13								
B4	VREFB4N0	IO	DIFFIO_B26n			P11	109	T13	V14				DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B27p						V15						DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B27n						W15						DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B28p						T14								
B4	VREFB4N0	IO	DIFFIO_B28n						T15						DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO							AB18						DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO					110		AA18								
B4	VREFB4N0	IO	RUP2		66	N12	111	M10	AA19	DQ1B	DQ1B						
B4	VREFB4N0	IO	RDN2		67	P12	112	N11	AB19	DQ1B	DQ1B						
B4	VREFB4N0	IO	DIFFIO_B29p					T14	W17				DQ5B	DQ5B	DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B29n		68	R11	113	T15	Y17	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3
B4	VREFB4N0	IO	VREFB4N0		69	R12	114	P11	V16								
B4	VREFB4N0	VCCINT			70		115										
B4	VREFB4N0	IO	DIFFIO_B30p						AA20							DQ5B	DQ5B
B4	VREFB4N0	GND					116										
B4	VREFB4N0	IO	DIFFIO_B30n						AB20						DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	PLL4_CLKOUTp		71	R14	117	P14	T16								
B4	VREFB4N0	IO	PLL4_CLKOUTn		72	R13	118	R14	R16								
B4	VREFB4N0	IO	DIFFIO_B31p				119	L11	U15								
B4	VREFB4N0	IO	DIFFIO_B31n				120	M11	U14								
B4	VREFB4N0	IO	DIFFIO_B32p						R14								
B4	VREFB4N0	IO	DIFFIO_B32n						R15								
B5	VREFB5N1	VCCD_PLL4			73	P14	121	N13	V17								
B5	VREFB5N1	GNDA4			74	P15	122	M12	V18								
B5	VREFB5N1	VCCA4			75	R15	123	L12	U18								
B5	VREFB5N1	IO	DIFFIO_R35n						AA22								
B5	VREFB5N1	IO	DIFFIO_R35p					K12	AA21						DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3
B5	VREFB5N1	VCCIO5					124										
B5	VREFB5N1	IO							P14								
B5	VREFB5N1	GND					125										
B5	VREFB5N1	IO	RUP3		76	N15	126	N14	T17			DQ1R	DM1R/BWS#1R				
B5	VREFB5N1	IO	RDN3		77	M14	127	P15	T18			DQ1R	DQ1R				
B5	VREFB5N1	IO	DIFFIO_R34n				128	P16	W20			DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4
B5	VREFB5N1	IO	DIFFIO_R34p					R16	W19				DQ1R				
B5	VREFB5N1	IO	DIFFIO_R33n						Y22						DQ3R	DQ3R	DQ1R
B5	VREFB5N1	VCCINT			78		129										
B5	VREFB5N1	IO	DIFFIO_R33p						Y21								
B5	VREFB5N1	GND					130										
B5	VREFB5N1	IO	DIFFIO_R32n						U20						DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R32p						U19								
B5	VREFB5N1	IO							N14								
B5	VREFB5N1	IO	DIFFIO_R31n		79	M15	131	N16	W22			DQ1R	DQ1R		DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R31p			L14	132	N15	W21			DQ1R	DQ1R		DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R30n						P15								
B5	VREFB5N1	IO	DIFFIO_R30p						P16								
B5	VREFB5N1	IO	VREFB5N1		80	L15	133	L14	R17								
B5	VREFB5N1	IO	DIFFIO_R29n						M15								
B5	VREFB5N1	IO	DIFFIO_R29p						N15								
B5	VREFB5N1	IO							P17								
B5	VREFB5N1	IO	DIFFIO_R28n						V22						DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R28p						V21						DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO							R20						DQ3R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R27n						U22						DQ3R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R27p				134		U21			DQ1R			DQ3R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R26n				135	L13	R18			DQ1R	DQ1R				
B5	VREFB5N0	VCCIO5			81		136										
B5	VREFB5N0	IO	DIFFIO_R26p				137	L16	R19			DQ1R	DQ1R		DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2
B5	VREFB5N0	GND			82		138										
B5	VREFB5N0	IO							N16								

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B5	VREFB5N0	IO	DIFFIO_R25n						R22						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R25p						R21						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	VREFB5N0		83	K13	139	L15	P20								
B5	VREFB5N0	VCCINT			84		140										
B5	VREFB5N0	IO	DIFFIO_R24n						P22						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	GND					141										
B5	VREFB5N0	IO	DIFFIO_R24p						P21						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R23n						N20						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R23p						N19								
B5	VREFB5N0	IO	DIFFIO_R22n				142	K16	N17				DQ1R				
B5	VREFB5N0	IO	DIFFIO_R22p		85	K14	143	K15	N18	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6
B5	VREFB5N0	IO	DIFFIO_R21n	DEV_OE	86	K15	144	J16	N22								
B5	VREFB5N0	IO	DIFFIO_R21p	DEV_CLRn	87	J13	145	J15	N21								
B5	VREFB5N0	IO	DIFFIO_R20n						M22						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R20p						M21						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R19n				146	J14	M20				DQ1R		DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R19p				147	J12	M19						DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO					148	J13	M16				DQ1R				
B5	VREFB5N0	CLK7	DIFFCLK_3n		88	J15	149	M16	T22								
B5	VREFB5N0	CLK6	DIFFCLK_3p		89	J14	150	M15	T21								
B6	VREFB6N1	CLK5	DIFFCLK_2n		90	H15	151	E16	G22								
B6	VREFB6N1	CLK4	DIFFCLK_2p		91	H14	152	E15	G21								
B6	VREFB6N1	CONF_DONE		CONF_DONE	92	H13	153	H14	M18								
B6	VREFB6N1	VCCIO6			93		154										
B6	VREFB6N1	MSEL0		MSEL0	94	G13	155	H13	M17								
B6	VREFB6N1	GND			95		156										
B6	VREFB6N1	MSEL1		MSEL1	96	G14	157	H12	L18								
B6	VREFB6N1	MSEL2		MSEL2	97	G15	158	G12	L17								
B6	VREFB6N1	MSEL3		MSEL3 (3)					K20								
B6	VREFB6N1	IO	DIFFIO_R18n					H16	L16								
B6	VREFB6N1	IO	DIFFIO_R18p					H15	L15								
B6	VREFB6N1	IO	DIFFIO_R17n	INIT_DONE	98	F13	159	G16	L22								
B6	VREFB6N1	IO	DIFFIO_R17p	CRC_ERROR	99	F14	160	G15	L21								
B6	VREFB6N1	IO							K15								
B6	VREFB6N1	IO	VREFB6N1		100	F15	161	F13	K19								
B6	VREFB6N1	IO							J15								
B6	VREFB6N1	IO	DIFFIO_R16n	nCEO	101	E14	162	F16	K22								
B6	VREFB6N1	VCCINT			102		163										
B6	VREFB6N1	IO	DIFFIO_R16p	CLKUSR	103	E15	164	F15	K21								
B6	VREFB6N1	GND					165										
B6	VREFB6N1	IO	DIFFIO_R15n		104	D14	166	B16	J22	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7
B6	VREFB6N1	IO	DIFFIO_R15p						J21						DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1
B6	VREFB6N1	IO	DIFFIO_R14n						J16								
B6	VREFB6N1	IO	DIFFIO_R14p						K16								
B6	VREFB6N1	IO	DIFFIO_R13n						H22						DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R13p						H21						DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R12n						K17								
B6	VREFB6N1	IO	DIFFIO_R12p						K18						DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO							J18								
B6	VREFB6N1	IO	DIFFIO_R11n						F22						DQ0R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R11p						F21						DQ0R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R10n						H20						DQ0R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R10p						H19						DQ0R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R9n	nWE			167		E22						DQ0R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R9p	nOE			168		E21							DQ1R	DQ1R
B6	VREFB6N0	IO	VREFB6N0		105	D15	169	F14	H18								
B6	VREFB6N0	IO	DIFFIO_R8n						J17								
B6	VREFB6N0	IO	DIFFIO_R8p						H16								
B6	VREFB6N0	VCCIO6					170										
B6	VREFB6N0	IO	DIFFIO_R7n				171	D16	D22			DQ1R			DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0
B6	VREFB6N0	GND					172										
B6	VREFB6N0	IO	DIFFIO_R7p				173	D15	D21							DQ1R	DQ1R

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B6	VREFB6N0	IO	DIFFIO_R6n	nAVD			174		F20						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R6p				175		F19						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R5n	PADD23					G18						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R5p						H17								
B6	VREFB6N0	IO	DIFFIO_R4n						C22						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R4p						C21						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R3n	PADD22					B22						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R3p	PADD21				G11	B21						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R2n	PADD20	106	C15	176	C16	C20			DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5
B6	VREFB6N0	IO	DIFFIO_R2p				177	C15	D20								
B6	VREFB6N0	IO	DIFFIO_R1n						F17						DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R1p						G17								
B6	VREFB6N0	VCCA2			107	A15	178	F12	F18								
B6	VREFB6N0	GNDA2			108	B15	179	E12	E18								
B6	VREFB6N0	VCCD_PLL2			109	B14	180	D13	E17								
B7	VREFB7N0	IO	DIFFIO_T32n					C14	F16								
B7	VREFB7N0	IO	DIFFIO_T32p				181	D14	E16				DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T31n						F15						DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T31p						G16								
B7	VREFB7N0	IO	DIFFIO_T30n			B13	182	D11	G15								
B7	VREFB7N0	IO	DIFFIO_T30p		110	A14	183	D12	F14	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6
B7	VREFB7N0	IO							G14								
B7	VREFB7N0	IO	VREFB7N0		111	A13	184	C11	D17								
B7	VREFB7N0	IO	DIFFIO_T29n					B13	C19				DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T29p						D19						DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	PLL2_CLKOUTn		112	B12	185	A14	A20								
B7	VREFB7N0	IO	PLL2_CLKOUTp		113	A12	186	B14	B20								
B7	VREFB7N0	IO							C17						DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T28n						H15								
B7	VREFB7N0	IO	DIFFIO_T28p						H14								
B7	VREFB7N0	IO	RUP4		114	B11	187	E11	B19	DQ1T	DQ1T						
B7	VREFB7N0	IO	RDN4		115	A11	188	E10	A19	DQ1T	DQ1T						
B7	VREFB7N0	IO	DIFFIO_T27n				189		A18						DQ2T	DQ5T	DQ5T
B7	VREFB7N0	VCCINT			116		190										
B7	VREFB7N0	IO	DIFFIO_T27p	PADD0				A12	B18				DQ5T	DQ5T			
B7	VREFB7N0	GND					191										
B7	VREFB7N0	IO	DIFFIO_T26n					B12	D15				DQ5T	DQ5T			
B7	VREFB7N0	IO	DIFFIO_T26p						E15						DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO							G13								
B7	VREFB7N1	VCCIO7			117		192										
B7	VREFB7N1	IO	DIFFIO_T25n	PADD1				A11	A17				DQ5T	DQ5T	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	GND			118		193										
B7	VREFB7N1	IO	DIFFIO_T25p	PADD2			194	B11	B17			DQ5T	DQ5T	DQ5T		DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T24n						A16						DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0
B7	VREFB7N1	IO	DIFFIO_T24p						B16						DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	VREFB7N1		119	B10	195	A13	C15								
B7	VREFB7N1	IO	DIFFIO_T23n	PADD3	120	A10	196	A15	E14	DQ1T	DQ1T				DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T23p				197		F12			DQ5T					
B7	VREFB7N1	IO	DIFFIO_T22n				198		H13								
B7	VREFB7N1	IO	DIFFIO_T22p				199		H12								
B7	VREFB7N1	IO	DIFFIO_T21n						G12								
B7	VREFB7N1	IO	DIFFIO_T21p	PADD4	121	C9	200	F9	F13			DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8
B7	VREFB7N1	IO	DIFFIO_T20n	PADD5				A10	A15				DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T20p	PADD6			201	B10	B15			DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	VCCIO7			122												
B7	VREFB7N1	IO	DIFFIO_T19n	PADD7			202	C9	C13			DQ5T	DQ5T	DQ5T			
B7	VREFB7N1	GND			123												
B7	VREFB7N1	IO	DIFFIO_T19p	PADD8			203	D9	D13				DM5T/BWS#5T	DM5T0/BWS#5T0	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	VCCINT			124		204										
B7	VREFB7N1	IO							E13								
B7	VREFB7N1	GND					205										
B7	VREFB7N1	IO	DIFFIO_T18n	PADD9					A14						DQ4T	DQ5T	DQ5T

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
B7	VREFB7N1	IO	DIFFIO_T18p	PADD10					B14						DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T17n	PADD11					A13						DQ4T	DQ5T	DQ5T
B7	VREFB7N1	VCCIO7					206										
B7	VREFB7N1	IO	DIFFIO_T17p	PADD12	125	A9	207	E9	B13			DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9
B7	VREFB7N1	GND					208										
B7	VREFB7N1	IO							E12							DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T16n	PADD13					E11								
B7	VREFB7N1	IO	DIFFIO_T16p	PADD14					F11						DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1
B7	VREFB7N1	CLK8	DIFFCLK_5n		126	B9	209	A9	A12								
B7	VREFB7N1	CLK9	DIFFCLK_5p		127	A8	210	B9	B12								
B8	VREFB8N0	CLK10	DIFFCLK_4n		128	B8	211	A8	A11								
B8	VREFB8N0	CLK11	DIFFCLK_4p		129	A7	212	B8	B11								
B8	VREFB8N0	IO							H11								
B8	VREFB8N0	IO	DIFFIO_T15n						D10						DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T15p						E10								
B8	VREFB8N0	IO	DIFFIO_T14n						A10						DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T14p	PADD15					B10								
B8	VREFB8N0	IO	DIFFIO_T13n	PADD16					A9						DQ5T	DQ3T	DQ5T
B8	VREFB8N0	VCCIO8			130		213										
B8	VREFB8N0	IO	DIFFIO_T13p	PADD17			214	C8	B9			DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10
B8	VREFB8N0	GND			131		215										
B8	VREFB8N0	IO					216	D8	C10				DQ3T	DQ5T			
B8	VREFB8N0	IO					217		G11			DQ5T					
B8	VREFB8N0	IO	DIFFIO_T12n	DATA2	132	C7	218	E8	A8	DQ1T	DQ1T		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T12p	DATA3	133	B7	219	F8	B8	DQ1T	DQ1T	DQ5T			DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T11n	PADD18	134	B6	220	A7	A7				DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T11p	DATA4	135	A6	221	B7	B7	DQ1T	DQ1T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T10n	PADD19			222		A6						DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T10p	DATA15					B6						DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	VREFB8N0		136	C6	223	C6	E9								
B8	VREFB8N0	IO	DIFFIO_T9n	DATA14			224	A6	C8			DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11
B8	VREFB8N0	IO	DIFFIO_T9p	DATA13				B6	C7				DQ3T	DQ5T	DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2
B8	VREFB8N0	IO	DIFFIO_T8n						G10								
B8	VREFB8N0	IO	DIFFIO_T8p						G9								
B8	VREFB8N0	IO	DIFFIO_T7n						H10								
B8	VREFB8N0	IO	DIFFIO_T7p						H9								
B8	VREFB8N0	VCCIO8					225										
B8	VREFB8N0	IO		DATA5	137	A5	226	E7	A5	DQ1T	DQ1T	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N0	GND					227										
B8	VREFB8N1	IO							B5								
B8	VREFB8N1	VCCINT			138		228										
B8	VREFB8N1	GND					229										
B8	VREFB8N1	IO	DIFFIO_T6n				230		F9								
B8	VREFB8N1	IO	DIFFIO_T6p	DATA6		B4	231	E6	F10			DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO		DATA7		A4	232	A5	C6			DM5T/BWS#5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T5n						A4						DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T5p	DATA8				B5	B4				DQ3T	DQ5T	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T4n	DATA9			233	D6	F8						DQ3T	DQ3T	DQ5T
B8	VREFB8N1	VCCIO8			139												
B8	VREFB8N1	IO	DIFFIO_T4p						G8								
B8	VREFB8N1	GND			140												
B8	VREFB8N1	IO	DIFFIO_T3n	DATA10			234	A4	A3				DM3T/BWS#3T	DM5T1/BWS#5T1	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T3p	DATA11				B4	B3						DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	VREFB8N1		141	C4	235	A2	D6								
B8	VREFB8N1	IO						D5	E7								
B8	VREFB8N1	IO	DIFFIO_T2n					A3	C3						DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T2p	DATA12	142	A3	236	B3	C4	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7
B8	VREFB8N1	IO	DIFFIO_T1n				237		F7						DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3
B8	VREFB8N1	IO	DIFFIO_T1p				238		G7								
B8	VREFB8N1	IO	PLL3_CLKOUTn		143	A2	239	C3	E6	DQ1T	DQ1T						
B8	VREFB8N1	IO	PLL3_CLKOUTp		144	B3	240	D3	E5	DM1T	DM1T						

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
		VCCINT				D3		F7	J11								
		VCCINT				D6		F11	J12								
		VCCINT				N2		G6	L14								
		VCCINT				D10		G7	M14								
		VCCINT				F12		G8	P11								
		VCCINT				H12		G9	P12								
		VCCINT				M8		G10	L9								
		VCCINT				M11		H6	M9								
		VCCINT				D8		H11	J13								
		VCCINT				L3		J6	J14								
		VCCINT				P3		K7	K14								
		VCCINT				K12		K11	J10								
		VCCINT							K9								
		VCCINT							N9								
		VCCINT							P9								
		VCCINT							P10								
		VCCINT							P13								
		VCCINT							U16								
		VCCINT							U17								
		VCCINT							T13								
		VCCINT							J8								
		VCCIO1				F4		E3	D4								
		VCCIO1						G3	F4								
		VCCIO1							K4								
		VCCIO1							H4								
		VCCIO2				J4		K3	N4								
		VCCIO2						M3	U4								
		VCCIO2							W4								
		VCCIO2							R4								
		VCCIO3				M5		P4	AB2								
		VCCIO3				M6		P7	W5								
		VCCIO3						T1	W9								
		VCCIO3							W11								
		VCCIO3							AA6								
		VCCIO4				M9		P10	AB21								
		VCCIO4				N9		P13	W12								
		VCCIO4						T16	W16								
		VCCIO4							W18								
		VCCIO4							Y14								
		VCCIO5				L13		K14	P18								
		VCCIO5						M14	V19								
		VCCIO5							Y19								
		VCCIO5							T19								
		VCCIO6				D13		E14	E19								
		VCCIO6						G14	G19								
		VCCIO6							L19								
		VCCIO6							J20								
		VCCIO7				C10		A16	A21								
		VCCIO7				C11		C10	D12								
		VCCIO7						C13	D14								
		VCCIO7							D16								
		VCCIO7							D18								
		VCCIO8				B5		A1	A2								
		VCCIO8				C5		C4	D5								
		VCCIO8						C7	D9								
		VCCIO8							D11								
		VCCIO8							E8								
		GND				E3		H7	L10								
		GND				G12		H8	L11								
		GND				D7		H9	M10								
		GND				N14		H10	M11								
		GND				M7		J7	L12								
		GND				N1		J8	L13								
		GND				P13		J9	M12								

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Bank Number	VREFB Group	Pin Name/ Function	Optional Function(s)	Configuration Function	E144 (4)	M164	Q240	F256/ U256	F484/ U484	DQS for X8/X9 in E144	DQS for X8/X9 in M164	DQS for X8/X9 in Q240	DQS for X8/X9 in F256/U256	DQS for X16/X18 in F256/U256	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484
		GND				P4		J10	M13								
		GND				D9		F6	N11								
		GND				M3		F10	K11								
		GND				R2		J11	N12								
		GND				J12		K8	K12								
		GND							K13								
		GND							N13								
		GND							N10								
		GND							K10								
		GND							J9								
		GND							D7								
		GND							J5								
		GND							H8								
		GND				K4		B2	A1								
		GND				N4		B15	C5								
		GND				G4		C5	C9								
		GND				D5		C12	C11								
		GND				C12		D7	C12								
		GND				D11		D10	C14								
		GND				C14		E4	C16								
		GND				M13		E13	A22								
		GND				M10		G4	E20								
		GND				C2		G13	G20								
		GND				C8		K4	L20								
		GND				E13		K13	P19								
		GND						M4	V20								
		GND						M13	Y20								
		GND						N7	AB22								
		GND						N10	Y18								
		GND						P5	Y16								
		GND						P12	Y12								
		GND						R2	Y11								
		GND						R15	Y9								
		GND							Y5								
		GND							AB1								
		GND							N3								
		GND							U3								
		GND							W3								
		GND							D3								
		GND							F3								
		GND							K3								
		GND							H3								
		GND							R3								
		GND							AB6								
		GND							Y15								
		GND							T20								
		GND							J19								
		GND							C18								
		GND							D8								

Notes:

(1) If the p pin or n pin is not available for the package, this means that the particular differential pair is not supported.
(2) DQS pins that do not have the associated DQ pins are not supported.
(3) E144, M164, Q240, and F256 in EP3C16 do not have the MSEL[3] pin and do not support the Active Parallel(AP) configuration mode.
(4) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity, and not for thermal purposes.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI and TDO) and the following configuration pins: nCONFIG, DCLK, DATA[15..0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank. If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA[1..4]	Power	Supply (analog) voltage for PLLs[1..4] and other analog circuits in the device.
VCCD_PLL[1..4]	Power	Supply (digital) voltage for PLLs[1..4].
RUP[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor Rup must be connected to the designated RUP pin within the same bank. If not required, this pin is a regular I/O pin.
RDN[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor Rdn must be connected to the designated RDN pin within the same bank. If not required, this pin is a regular I/O pin.
GNDA[1..4]	Ground	Ground for PLL[1..4]. You can connect these pins to GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
DATA0	Input (PS, FPP, AS) Bidirectional open drain (AP)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA0 is a dedicated bidirectional pin with optional user control.
MSEL[3..0]	Input	Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller devices or package options do not support the AP flash programming and do not have the MSEL[3] pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin.
	Clock and PLL Pins	
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
PLL[1..4]_CLKOUT[p,n]	I/O, Output	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.These pins can only use the differential I/O standard if it is being fed by a PLL output.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
		Optional/Dual-Purpose Configuration Pins
DCLK	Input (PS, FPP) I/O, Output (AS, AP)	Configuration clock pin. In PS and PP configuration modes, DCLK is used to clock configuration data from an external source into the Cyclone III device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. After AS or AP configuration, this pin is available as a user I/O pin with optional user control.
nCEO	I/O, Output	Output that drives low when device configuration is complete.
FLASH_nCE, nCSO	I/O, Output	This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active. nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.
DATA1, ASDO	Input (FPP) Output (AS) Bidirectional open-drain (AP)	This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control. ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.
DATA[7..2]	Input (FPP) Bidirectional open-drain (AP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings. After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control.
DATA[15..8]	Bidirectional open-drain (AP)	Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15..0]. In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15..8] are dedicated bidirectional pins with optional user control.
PADD[23..0]	I/O, Output (AP)	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.
nRESET	I/O, Output (AP)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.
nAVD	I/O, Output (AP)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus.
nOE	I/O, Output (AP)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0]).
nWE	I/O, Output (AP)	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.This pin can be set in Quartus ® II software to support open-drain output.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
		Dual-Purpose Differential and External Memory Interface Pins
DIFFIO_[L,R,T,B][0..61][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7]	I/O, DQS/CQ, CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][L,R,T,B]	I/O, DQ	Optional data signal for use in external memory interfaces.
DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.

Note:

(1) The pin definitions are prepared based on the device with the largest density, EP3C120. Refer to the pin list for the availability of pins in each density.

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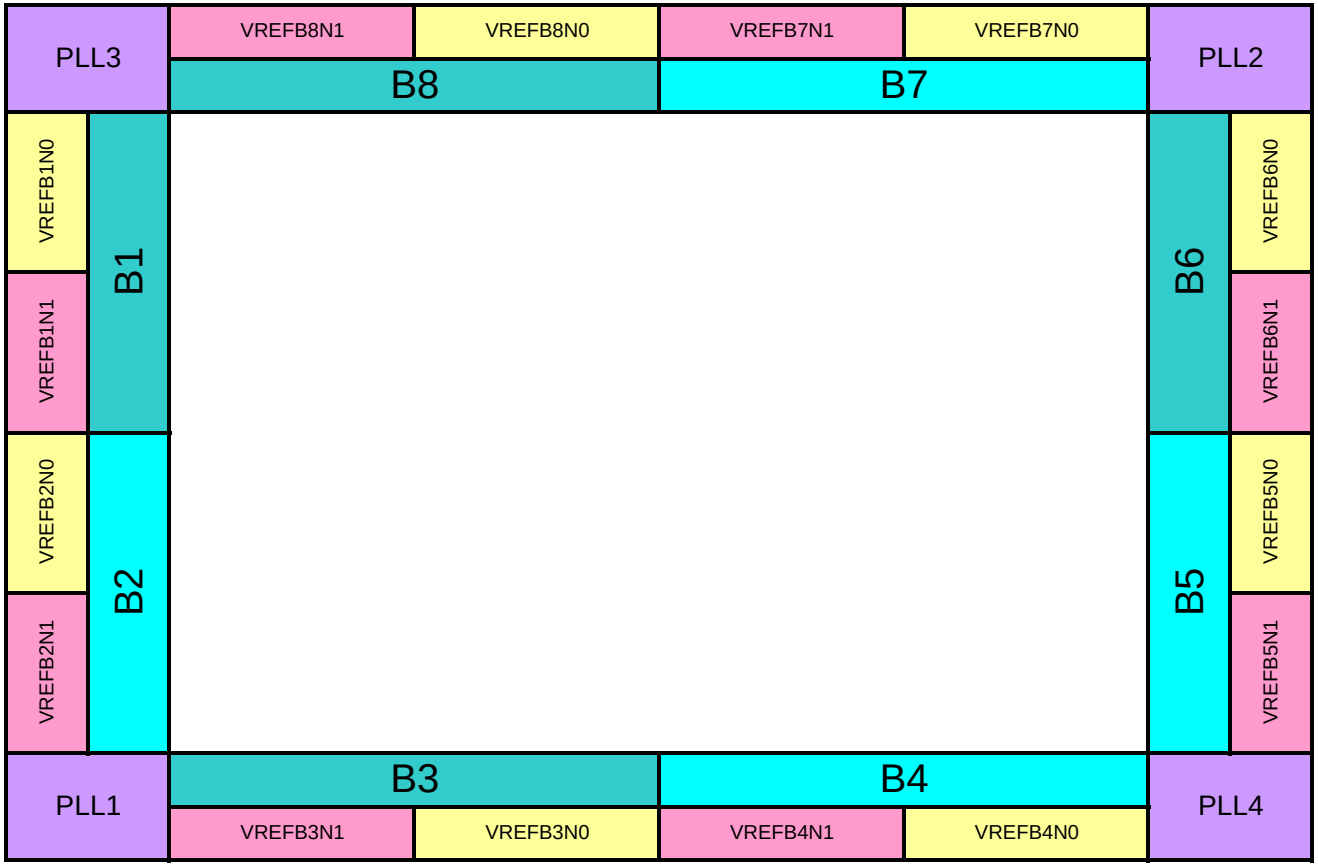

Notes:

(1) This is a top view of the silicon die.

(2) This is only a pictorial representation to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

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Version Number	Changes Made	Date
1.0	Initial release	8/17/2007
1.1	Added support for M164 package	11/23/2007
1.2	Updated pin function for CRC_ERROR pin	5/13/2008
	Updated DQ/DQS support for UBGA package	
	Updated pin function for PLL[1..4]_CLKOUT[p,n] pin	
	Remove RDY from pin list and pin definitions	
	Incorporated pin connection guideline into Pin Definitions worksheet	
	Incorporated VCCA and VCCD Decoupling recommendations	
1.3	Removed Pin Connection Guideline from Pin Definitions worksheet.	10/7/2009
	Removed VCCA and VCCD Decoupling recommendations.	
	Removed PKG notes from Pin List Worksheet.	
	Updated pin function for DCLK pin.	

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