SAM3U Microcontroller Series
Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's SAM3U series of ARM® Cortex™-M3, Thumb®2-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the SAM3U Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

11006A–ATARM–13-Oct-09

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the SAM3U Series Microcontrollers on Atmel's Web site.

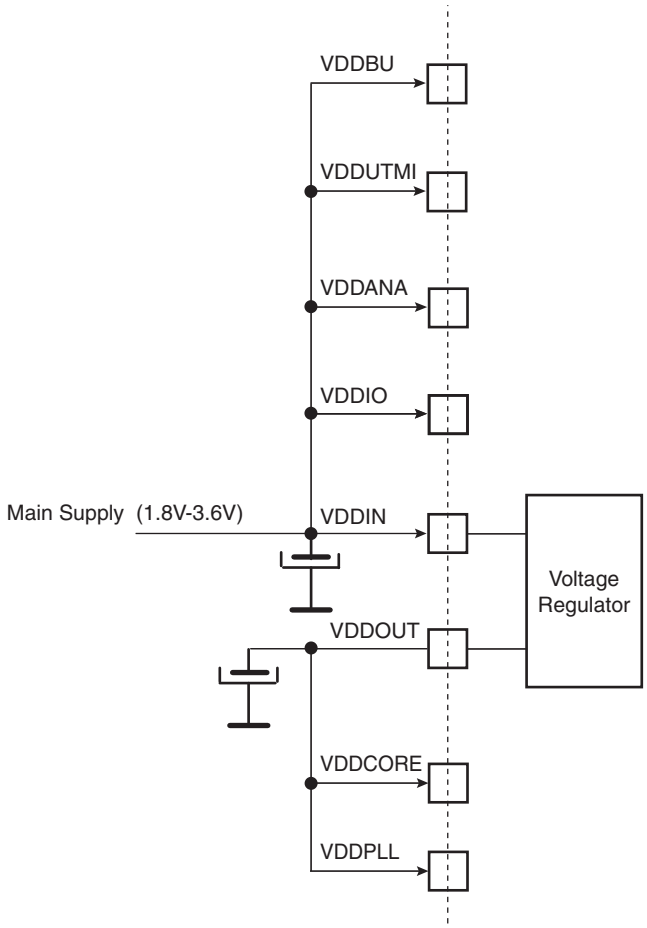
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	SAM3U Series Product Datasheet
Internal architecture of processor Thumb2 instruction sets Embedded in-circuit-emulator	Cortex-M3 Technical Reference Manual (available from ARM Ltd.)
Evaluation Kit User Guide	SAM3U-EK Evaluation Board User Guide

3. Schematic Check List

Single Power Supply Strategy



Single Power Supply Schematic Example:

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	1.8V to 3.6V Decoupling/Filtering capacitor (100 nF)[1][2]	Powers the voltage regulator.
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7µF)[1][2]	Powers the peripheral I/Os Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 4.7µF)[1][2]	Output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling capacitor (100 nF)[1][2]	Core, embedded memories and peripherals power supply.
	VDDUTMI	3.0V to 3.6V Decoupling/Filtering RLC circuit (1R resistor and 4.7µF capacitor in parallel with a 100 nF capacitor, 10 µH inductor)[1][2][8]	Powers the UTMI+ interface.
	VDDPLL	1.62V to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers PLLA, UPLL and 3-20 MHz oscillator.
	VDDANA	2.0V to 3.6V Decoupling/Filtering RLC circuit (1R resistor and 4.7µF capacitor in parallel with a 100 nF capacitor, 10 µH inductor)[1][2][8]	ADC power supply
	VDDBU	1.62V to 3.6V **VDDBU must be supplied before or at the same time as VDDIO and VDDCORE**	Powers the Slow Clock oscillator and a part of the System Controller.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE.
	GNDBU	Backup unit ground	GNDBU pin is provided for VDDBU pin.
	GNDANA	ADC ground	GNDANA pin is provided for VDDANA pin.
	GNDPLL	PLL ground	GNDPLL pin is provided for VDDPLL pin.
	GNDUTMI	UTMI+ ground	GNDUTMI pin is provided for VDDUTMI pin.

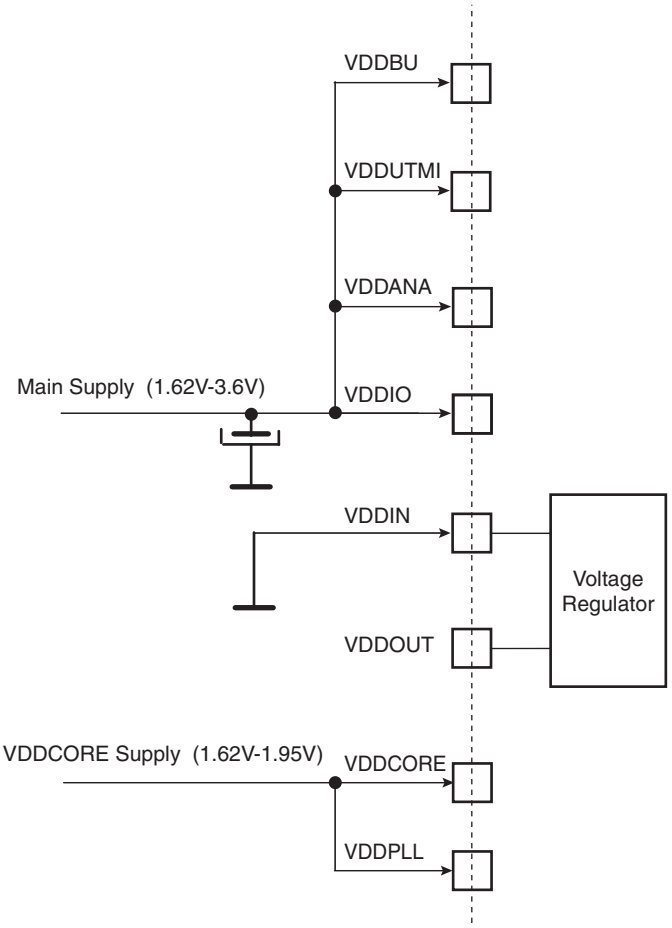
Note: Restrictions

With Main Supply < 2V, USB and ADC are not usable.

With Main Supply ≥ 2V and < 3V, USB is not usable.

With Main Supply ≥ 3V, all peripherals are usable.

Core externally supplied.



Core externally supplied Schematic Example:
Main Supply on VDDIO, VDDUTMI, VDDBU and VDDANA (1.62V to 3.6V).
VDDCORE Supply is between 1.62V and 1.95V.
Voltage regulator is OFF by connecting VDDIN to ground.

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	Connected to GND	The voltage regulator is OFF.
	VDDIO	1.62V to 3.6V Connected to Main Supply Decoupling/Filtering capacitors (100 nF and 4.7 µF)(1)(2)	Powers the peripheral I/Os. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Unconnected	Output of the main voltage regulator. Voltage regulator is OFF.
	VDDCORE	1.65V to 1.95V Connected to VDDCORE Supply Decoupling capacitor (100 nF)(1)(2)	Core, embedded memories and peripherals power supply
	VDDUTMI	3.0V to 3.6V Connected to Main Supply Decoupling/Filtering RLC circuit (1R resistor and 4.7µF capacitor in parallel with a 100nF capacitor, 10 µH inductor)(1)(2)(8)	Powers the UTMI+ interface.
	VDDPLL	1.62V to 1.95V Connected to VDDCORE Supply Decoupling capacitor (100 nF)(1)(2)	Powers PLLA, UPLL and 3-20 MHz oscillator.
	VDDANA	2.0VV to 3.6V Connected to Main Supply Decoupling/Filtering RLC circuit (1R resistor and 4.7µF capacitor in parallel with a 100nF capacitor 10µH inductor)(1)(2)(8)	ADC power supply
	VDDBU	1.62V to 3.6V Connected to Main Supply **VDDBU must be supplied before or at the same time as VDDIO and VDDCORE.**	Powers the Slow Clock oscillator and a part of the System Controller.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE
	GNDBU	Backup unit ground	GNDBU pin is provided for VDDBU pin.
	GNDANA	ADC ground	GNDANA pin is provided for VDDANA pin.
	GNDPLL	PLL ground	GNDPLL pin is provided for VDDPLL pin.
	GNDUTMI	UTMI+ ground	GNDUTMI pin is provided for VDDUTMI pin.

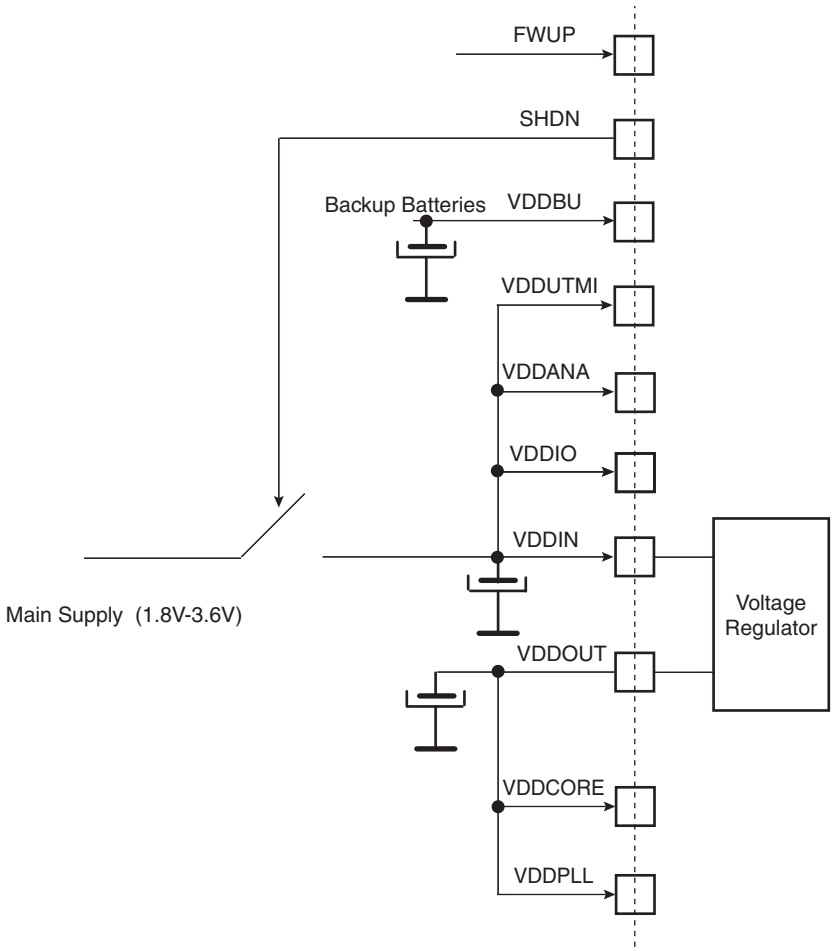
Note: Restrictions

With Main Supply < 2V, USB and ADC are not usable.

With Main Supply ≥ 2V and < 3V, USB is not usable.

With Main Supply ≥ 3V, all peripherals are usable.

Backup unit externally supplied



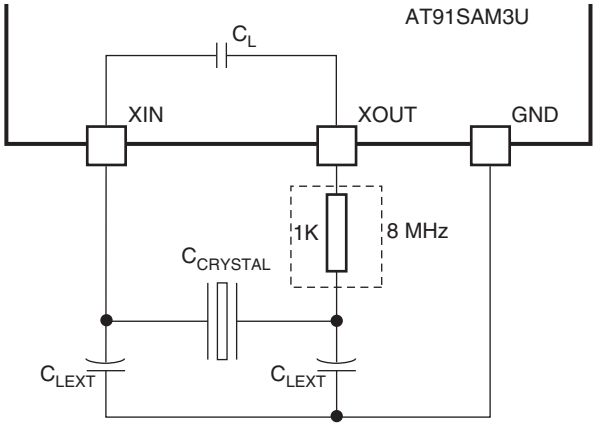
☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	1.8V to 3.6V Decoupling/Filtering capacitor (100 nF)[1][2]	Powers the voltage regulator.
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	Powers the peripheral I/Os. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 4.7µF)[1][2]	Output of the main voltage regulator. Voltage regulator is OFF
	VDDCORE	1.62V to 1.95V Decoupling capacitor (100 nF)[1][2]	Core, embedded memories and peripherals power supply
	VDDUTMI	3.0V to 3.6V Decoupling/Filtering RLC circuit (1R resistor and 4.7 µF capacitor in parallel with a 100 nF capacitor, 10 µH inductor)[1][2][8]	Powers the UTMI+ interface.
	VDDPLL	1.62V to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers PLLA, UPLL and 3-20 MHz oscillator.
	VDDANA	2.0V to 3.6V Decoupling/Filtering RLC circuit (1R resistor and 4.7µF capacitor in parallel with a 100 nF capacitor, 10 µH inductor)[1][2][8]	ADC power supply
	VDDBU	1.62V to 3.6V Connected to backup batteries. **VDDBU must be supplied before or at the same time as VDDIO and VDDCORE.**	Powers the Slow Clock oscillator and a part of the System Controller.
	FWUP	1.62V to 3.6V Connected to backup batteries	Force Wake-Up pin Allows to wake-up the device if the main supply is off.
	SHDN	Connected to the main supply control pin.	Shutdown pin Controls the main supply level.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE
	GNDBU	Backup unit ground	GNDBU pin is provided for VDDBU pin.
	GNDANA	ADC ground	GNDANA pin is provided for VDDANA pin.
	GNDPLL	PLL ground	GNDPLL pin is provided for VDDPLL pin.
	GNDUTMI	UTMI+ ground	GNDUTMI pin is provided for VDDUTMI pin.

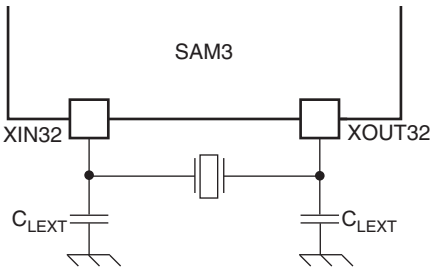
Note: Restrictions

With Main Supply < 2V, USB and ADC are not usable.

With Main Supply ≥ 2V and < 3V, USB is not usable.

With Main Supply ≥ 3V, all peripherals are usable.

☑	Signal Name	Recommended Pin Connection	Description
		Clock, Oscillator and PLL	
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz. A 12 MHz crystal is mandatory to use the High Speed USB.	Internal Equivalent Load Capacitance (C_L): C_L = 9.5 pF Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to validate.  The external load capacitance is calculated with the following formula: $C_{LEXT}=2*(C_{crystal}-C_L)$ Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM3U Series datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected. A 12 MHz clock is mandatory to use the High Speed USB.	1.8V Square wave signal (VDDPLL) External Clock Source up to 50 MHz Duty Cycle: 40 to 60%

☑	Signal Name	Recommended Pin Connection	Description
	XIN32 XOUT32 32 kHz Crystal used	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	No internal load capacitance Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to validate. .  Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM3U Series datasheet.
	XIN32 XOUT32 32 kHz Oscillator in bypass mode	XIN32: external clock source XOUT32: can be left unconnected.	1.8V to 3.3V Square wave signal (VDDBU) External Clock Source up to 44 kHz Duty Cycle: 40 to 60%

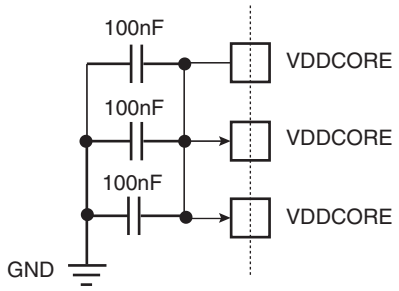
☑	Signal Name	Recommended Pin Connection	Description
Serial Wire and JTAG[3]			
	TCK/SWCLK	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TMS/SWDIO	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TDO/ TRACESWO	Floating	Output driven at up to V_{VDDIO}
	JTAGSEL	**In harsh[4] environments, it is strongly recommended to tie this pin to GNDBU if not used or to add an external low resistor value (such as 1 kOhm).** Must be tied to V_{VDDBU} to enter JTAG Boundary Scan.	Internal pull-down resistor (15 kOhm).
Flash Memory			
	ERASE	**In harsh[4] environments, it is strongly recommended to tie this pin to GNDBU if not used or to add an external low resistor value (such as 1 kOhm).**	Internal pull-down resistor (15 kOhm). Must be tied to V_{VDDBU} to erase the General Purpose NVM bits (GPNVMx), the whole Flash content and the security bit (SECURITY) Minimum debouncing time is 220 ms.
Reset/Test			
	NRST	Application dependant. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIO} (100 kOhm) is available for User Reset and External Reset control.
	NRSTB[5]	Application dependant. Can be connected to a push button for power-on reset. **In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDBU** To enter in FFPI mode NRSTB pin must be tied to $V_{VDDIO.}$	NRSTB is an asynchronous reset input always active. NRSTB pin integrates a permanent pull-up resistor (15 kOhm) and embeds an anti-glitch filter.
	TST[5]	**In harsh[4] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low resistor value (such as 1 kOhm).** To enter in FFPI mode TST pin must be tied to $V_{VDDIO.}$	Internal pull-down resistor (15 kOhm).

☑	Signal Name	Recommended Pin Connection	Description
	FWUP[5]	Add a pull-up resistor (100 kOhms) if OFF Mode or FWUP functionality is used. To enter in FFPI mode FWUP pin must be tied to $V_{VDDIO.}$ If unused, tie this pin to GND	Force wake-up input No internal pull-up resistor
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies.	This pin is a push-pull output. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).

☑	Signal Name	Recommended Pin Connection	Description
		PIO	
	PAx - PBx-PC[6]	Application Dependant (Pulled-up on V_{VDDIO})	At 1st power-up, PAx, PBx and PCx are in an undefined state. At reset, all PIOs are configured as Schmitt trigger inputs with pull-up. To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled. *Note: PA14, PB9 to PB16, PB25 to PB31 and PC20 to PC27 are not Shmitt triggered.*
		10-bit ADC	
	ADVREF	2.4V to V_{DDANA}. Decoupling capacitor(s).	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used, connect ADVREF to GND.
	AD0 to AD7	0V to V_{ADVREF}	ADx pins are multiplexed with PIOs.
		12-bit ADC (ADC12B)	
	AD12BVREF	2.4V to V_{DDANA}. Decoupling capacitor(s).	AD12BVREF is a pure analog input. To reduce power consumption, if ADC is not used, connect AD12BVREF to GND.
	AD12B0 to AD12B7	0V to $V_{AD12BvREF}$	AD12Bx pins are multiplexed with PIOs.
		USB High Speed Device (UDPHS)	
	DFSDP	Application dependent[7] If USB Device is not used it can be left floating.	Internal pull-down resistor
	DFSDM	Application dependent[7] If USB Device is not used it can be left floating.	Internal pull-down resistor
	DHSDP	Application dependent[7] If USB Device is not used it can be left floating.	Internal pull-down resistor
	DHSDM	Application dependent[7] If USB Device is not used it can be left floating.	Internal pull-down resistor
	VBG	Application dependent[7]	If USB Device is not used it must be left unconnected.

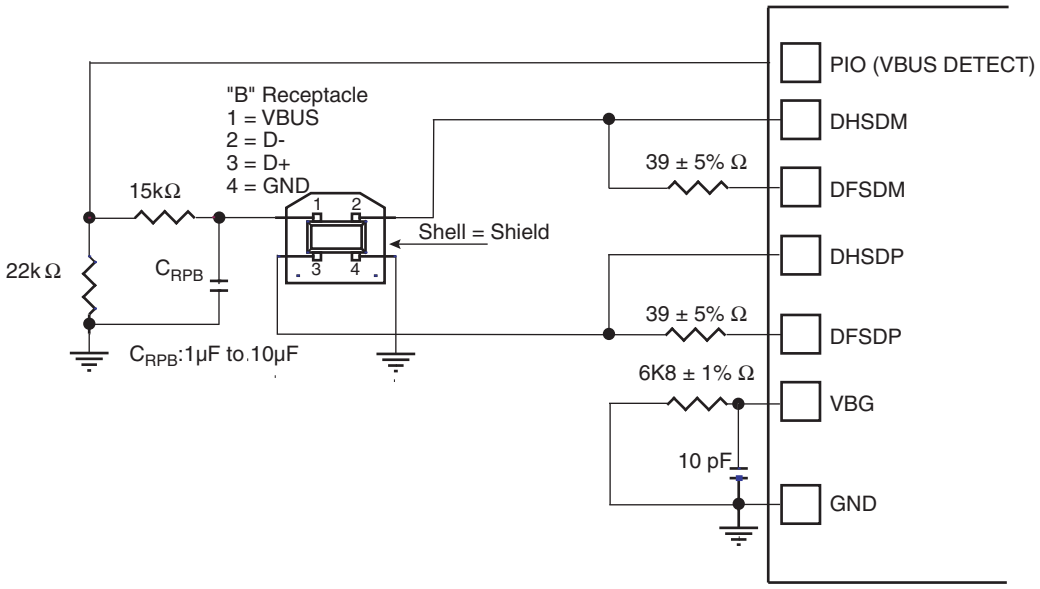
☑	Signal Name	Recommended Pin Connection	Description
Static Memory Controller (SMC)			
	D0-D15	Application dependent.	Data Bus (D0 to D15) *Note: Data bus lines are multiplexed with the PIOB controller. Their I/O line reset state is input with pull-up enabled.*
	A0-A23	Application dependent.	Address Bus (A0 to A23) *Note: Data bus lines are multiplexed with the PIOB & PIOC controllers. Their I/O line reset state is input with pull-up enabled.*
	NWAIT	Application dependent.	NWAIT pin is an active low input. *Note: NWAIT is multiplexed with PC18.*

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
5. See: Test Pin description in I/O Lines Considerations section of the SAM3U Series datasheet for more details on the different conditions to enter FFPI mode.
6. PB25 to PB31 and PCx is only available in 144-pin version

7. Typical USB High Speed Device connection: As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up. See: Typical Connection in USB High Speed Device Port section of the SAM3U Series datasheet for more details.



8. The filtering RLC circuit is given as an example. Depending on the application the user may only need a 100 nF decoupling capacitor.

4. SAM3U Boot Program Hardware Constraints

See AT91SAM Boot Program section of the SAM3U Series datasheet for more details on the boot program.

4.1 SAM-BA Boot

The SAM-BA® Boot Assistant supports serial communication via the UART or USB device port:

- UART Hardware Requirements: 3 to 8.9 MHz or 12 MHz or 19.7 to 20 MHz crystal.
  1 to 8.9 MHz or 12MHz or 19.7 to 50 MHz external clock.
- USB Device Hardware Requirements: 12 MHz Quartz or 12 MHz external clock on XIN.
  12 MHz must be ±500 ppm and 1.8V Square Wave Signal in bypass mode.

Table 4-1. Pins driven during SAM-BA Boot Program execution

Peripheral	Pin	PIO Line
UART	URXD	PA11
UART	UTXD	PA12

Revision History

Doc. Rev	Comments	Change Request Ref.
11006A	First issue	

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