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IF – Instruction Fetch

During this first stage of the pipeline we get the information at the program counters current location and store it into the instruction register.

ID – Instruction Decode

Break instruction register into three chunks and store them into the pipeline registers. Also stores information from other parts of the pipeline into the pipeline registers.

EX – Instruction execution

Preforms operations on the pipeline registers. Due to instruction conformity the pipeline does not need to know the instruction type and will therefore process most instructions very similarly.

Mem – Memory access/branch

Firstly the program counter is updated to the next instruction, this will always take place regards of what else happens. After this if the instruction was branch and it is true then we update the next program counter. In the case of a load or store, we read/write to memory using the ALU's output as an address.

WB – Write back

Information that was stored, loaded or operated on is written backwards into a pipeline register. This can allow it to be further operated upon. A notable feature of this pipeline section is that this stage is not required by a branch instruction.