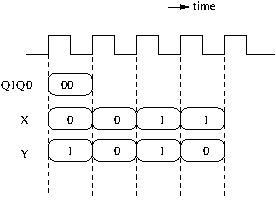
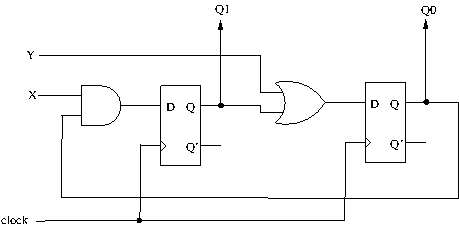
**長庚大學 資訊工程系 計算機組織 期中考試題 2019/11/11**

(1) 可翻閱參考書藉

(2) 考試時間：10:10AM – 12:00PM

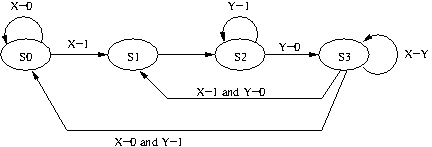
**General answering rules:**

1. You can use any components (such as AND-gate, adder, comparator, D flip flops, mod-N counter, etc.) that ever mentioned in this course and the digital circuit course without showing the detailed design of these components.
2. For a combinational circuit in part of your design, you just have to specify the Boolean equation or the truth table of this part. You don’t need to draw the detailed gate-level circuit diagram for a combinational circuit.
3. **(10 pts)** Given the circuit shown in the left-hand side of Figure 1, completes the waveform at the right-hand side to describe the behavior of the circuit.



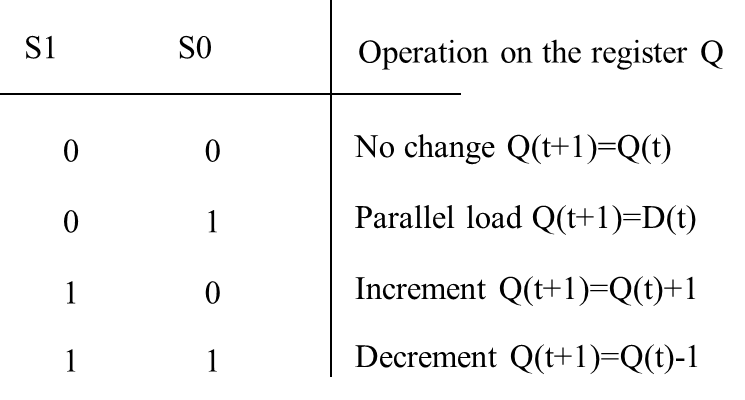
**Figure 1.**

1. **(15 pts)** Design a circuit with the behavior specified in the state-transition diagram shown in Figure 2. The circuit has four states and state-transitions are determined by two input signals X and Y (as annotated on edges)..



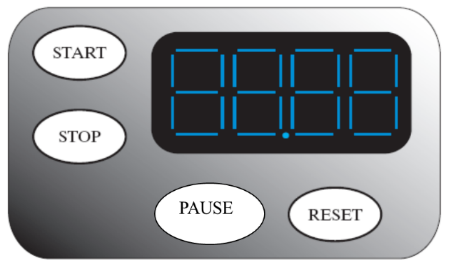
**Figure 2.**

1. **(15 pts)** Draw the **gate-level** circuit diagram of a 4-bit register Q with a 4-bit input D and mode selection S1 and S0. The register is to be operated according to the function table shown in Figure 3.



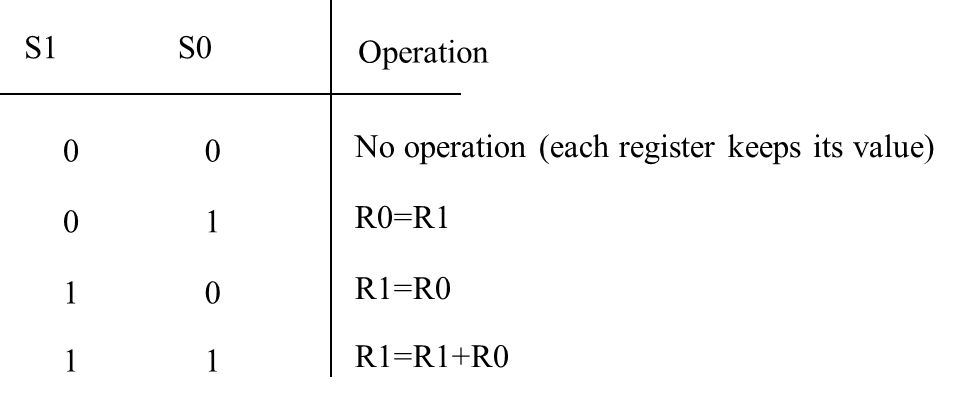
**Figure 3.**

1. **(20 pts)** Design a count-down timer with the following spec. The count-down timer looks like Figure 4. It has 4 digits to display the remaining time: 2 digits for minutes and 2 digits for seconds. After pressing the “START” button, the timer starts counting from 59:59 and down to 00:00, refreshing every 1 second. During the counting process, pressing “PAUSE” button will cause the timer to freeze at its current counting time. And press the “PAUSE” button again will cause the timer to resume counting from its current counting time. Answer the following questions regarding the count-down timer design:
2. Suppose the timer receives a clock signal with 100 Hz frequency. Explain how to generate a 1-cycle logic-1 pulse every second to trigger the counting.
3. Suppose the control unit has to deal with “START” and “PAUSE” button only. Draw the state-transition diagram to describe how the control unit controls the counting.
4. Continued from (b), draw the circuit diagram of the data path for keeping the time value.



**Figure 4.**

1. **(15 pts)** Draw the circuit diagram to realize the micro operations specified in Figure 5. The micro operations are concerned with two 8-bit registers R0 and R1 and controlled by two control signals S0 and S1.



**Figure 5.**

1. **(20 pts)** Design a circuit to compute arithmetic operations specified as follows. The signal interface is shown in Figure 6. The circuit receives input data A, B, C, and D. Each of the input data is of *n*-bit wide signed integer with 2’s complement encoding. Upon kicking the START signal, the circuit performs the following computation:

**if** (A+B>0)

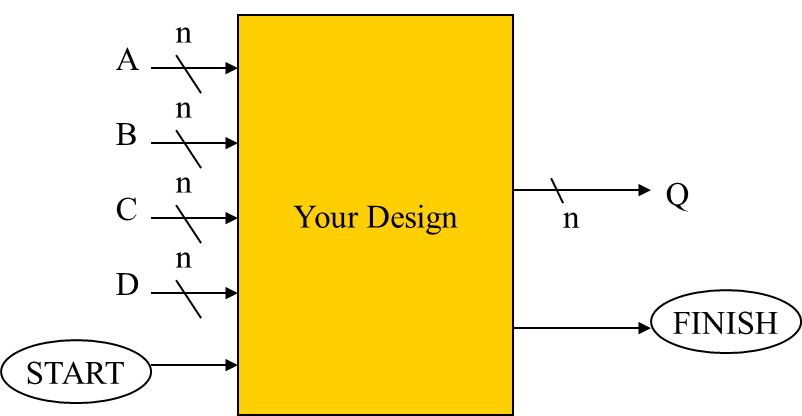
Q = C+D

**else**

Q = |C-D|

All input data will be kept fixed during the computation. You don’t need to deal with the case of overflow. You are asked to realize the computation with only one *n*-bit adder. Describe your design by answering the following questions:

1. Draw the data path to realize the computation.
2. Draw the state-transition diagram as the behavior description of the control unit to realize the computation.



**Figure 6.**

1. **(30 pts)**. You are asked to design the circuit of a data receiver of a serial bus protocol. The serial bus architecture is shown in Figure 7, which has one “master” and at most 16 “slaves” distinguished by a 4-bit slave ID. The master generates the clock signal MCLK that drives the operations of all slaves. And the master sends out its own data through the 1-bit data line MSO to some dedicated slave. Each slave has an 8-bit register Q to store the data sent from the master. Figure 8 shows the transmission protocol (as a timing waveform) of the serial bus. The data transmission follows the sequence:

(1) At initial, the system is idle and MSO=0.

(2) The master asserts logical 1 on MSO for one clock cycle to start a data transmission.

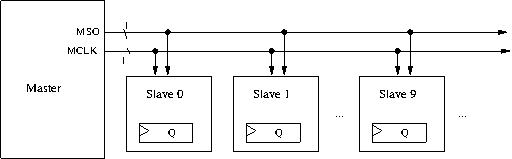
(3) The master sends out the 4-bit slave ID through MSO in 4 clock cycles to specify which slave is to receive the data. For example, the sequence “1001” will appear on MSO if the data is to send to Slave 9.

(4) The master sends out the 8-bit data through MSO in 8 clock cycles. After the transmission, the dedicated slave to receive the data should update its own register Q with the transmitted data. Other slaves should keep their contents in Q unchanged.

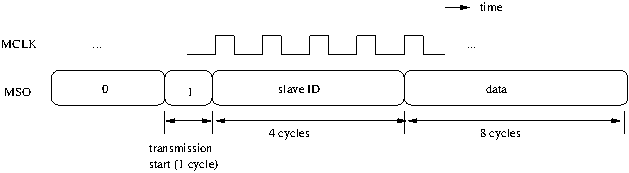
(5) The master asserts MSO=0 to go back to idle state.

You are asked to design the circuit of Slave 9 (with Slave ID “1001”). Describe your design by showing

1. The state-transition diagram of the control unit, and
2. Circuit diagram of the data path.



**Figure 7.**



**Figure 8.**