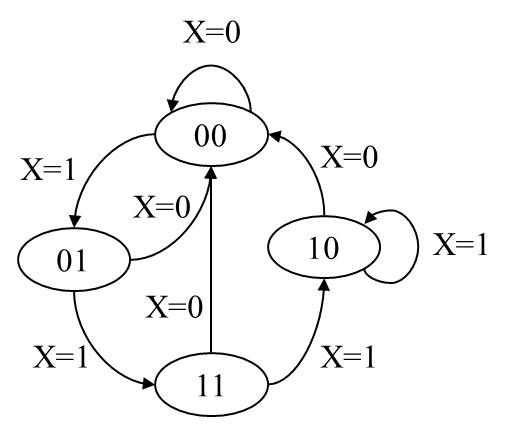
**長庚大學 資訊工程系 計算機組織 期末考試題 2018/01/15**

1. 可翻閱參考書籍

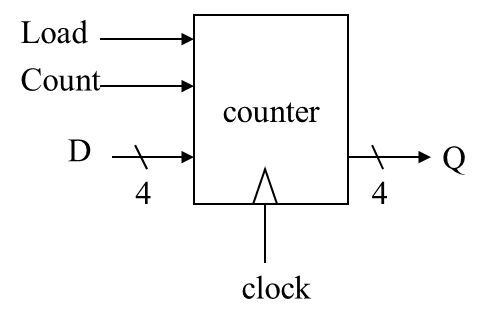
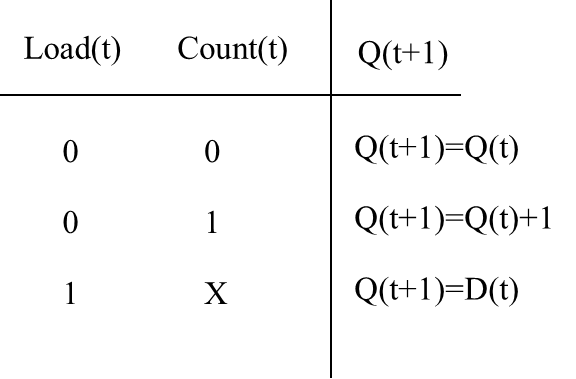
(2) 考試時間：10:10 – 12:00

1. **(15 pts)** Write the Verilog code to synthesize a circuit that realizes the state-transition diagram in Figure 1. The circuit has two flip-flops to establish four states and state transitions are based on the input signal *X*.



**Figure 1.**

2. **(15 pts)** Implement a 4-bit synchronous binary counter with synthesizable RTL coding. The spec is shown in Figure 2. The counter has 4-bit input D to set the content and the content is shown in the 4-bit output Q. Functionality of the counter is controlled by 2-bit control signal Load and Count as shown in Figure 2(b). Write the Verilog code to synthesize the counter.

1. (b)

**Figure 2.**

3. **(20 pts)** For each of the instructions listed below, write down the control signal value (in the format of Figure 3) to show how these instructions are realized by the CPU data path (in Figure 4).

(a) SUB R7, R2, R5 //R7=R2-R5

(b) DEC R1 //R1=R1+1

(c) LD R3, R6 //R3=mem[R6]

(d) BRN R4, -5 //if (R4<0) goto current\_position-5

(e) JMP R4 //goto position@R4



**Figure 3.**



**Figure 4.**

4. **(20pts)** Write down the machine code encoding for each instruction listed in Problem 3. (See appendix for the machine code format and assembly instruction table.)

5. **(25 pts)** Use the data path of the single-cycle CPU to perform the computation:

R0=|R1|+|R2|

The design concept is shown in Figure 5. You are asked to design additional control unit to command the data path to realize the required computation. You can modify any un-used register as needed. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 3) for each state.
3. the Verilog code that synthesizes the circuit of the control unit.



**Figure 5.**

6. **(30 pts)** You are asked to modify the single-cycle CPU with the addition of a new instruction BRGT (short for branch if greater than). The instruction takes two source operands Rs1 and Rs2 from registers and branch to the specified location if Rs1> Rs2. The target location is specified as an offset to current position and recorded in the instruction as an immediate. For example, the instruction

BRGT -5, R1, R2

means that “goto current\_position-5 if R1>R2”. Describe how you modify the CPU circuit by answering the following questions:

1. the machine code format to encode the new instruction
2. the modified control signal list for the modification
3. value of the modified control signal to perform “BRGT -5, R1, R2”
4. the modified data path circuit of the CPU
5. the modified branch control unit of the CPU.

