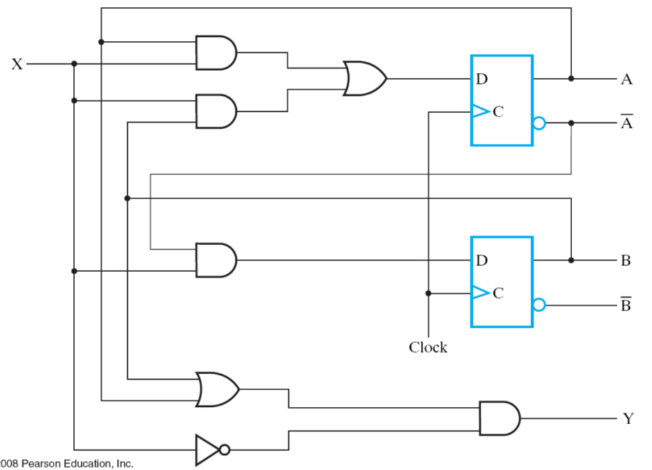
**長庚大學 資訊工程系 計算機組織 期末考試題 2019/01/07**

1. 可翻閱參考書籍

(2) 考試時間：10:10 – 12:00

1. **(6 pts)** Write the Verilog code to synthesize a circuit with equivalent function to Figure 1.



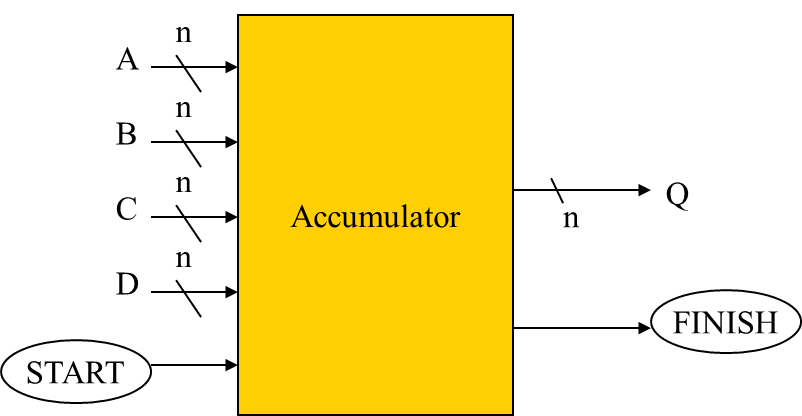
**Figure 1.**

2. Write the synthesizable Verilog code to complete our first example of RTL design: computing Q=A+B+C+D with only one adder. The input/output spec is shown in Figure 2(a): The circuit receives four 8-bit unsigned integer inputs (n=8) and generates an 8-bit output Q. The computing starts after receiving a one-cycle pulse with input START=1 and generates an output FINISH=1 upon finish. The behavior descriptions of the control unit and the data path are shown in Figure 2(b).

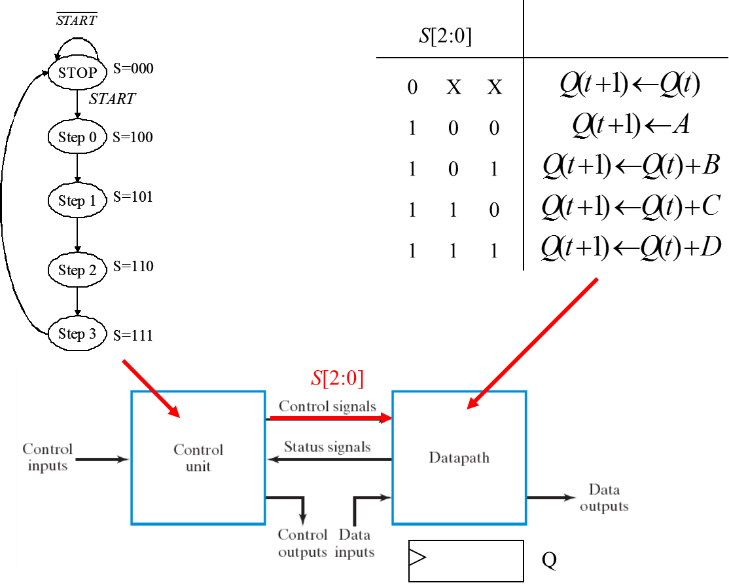
(a) **(8 pts)** Write the Verilog code to synthesize the control unit as an individual module with its behavior description given in Figure 2(b).

(b) **(8 pts)** Write the Verilog code to synthesize the data path as an individual module with its behavior description given in Figure 2(b). You have to ensure that only one adder is synthesized.

(c) **(8 pts)** Write the Verilog code of a top module that connects the control unit and the data path.







(b)

**Figure 2.**

3. **(20 pts)** For each of the instructions listed below, write down the control signal value (in the format of Figure 3) to show how these instructions are realized by the CPU data path (in Figure 4).

(a) ADD R6, R2, R3 //R6=R2+R3

(b) ADI R1, R2, 3 //R1=R2+3

(c) LD R3, R6 //R3=mem[R6]

(d) BRZ R2, -5 //if (R2==0) goto current\_position-5

(e) LDI R1, 3 //R1=3



**Figure 3.**



**Figure 4.**

4. **(20pts)** Write down the machine code encoding for each instruction listed in Problem 3. (See appendix for the machine code format and assembly instruction table.)

5. **(10 pts)** Write the assembly program of our simple demonstrative CPU to compute R0=|R1-R2|. You can modify any un-used registers.

6. **(25 pts)** Use the data path of the single-cycle CPU to perform the computation:

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That is, calculate the average value for registers {R0, R1, R2, R3} and store the result in R4 with fractional part been rounded off. The design concept is shown in Figure 5. You are asked to design additional control unit to command the data path to realize the required computation. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 3) for each state.
3. the Verilog code that synthesizes the circuit of the control unit.



**Figure 5.**

7. **(30 pts)** You are asked to modify the single-cycle CPU with the addition of a new instruction BRGT (short for branch if greater than). The instruction takes two source operands Rs1 and Rs2 from registers and branch to the specified location if Rs1> Rs2. The target location is specified as an offset to current position and recorded in the instruction as an immediate. For example, the instruction

BRGT -2, R1, R2

means that “goto current\_position-2 if R1>R2”. Describe how you modify the CPU circuit by answering the following questions:

1. the machine code format to encode the new instruction
2. the modified control signal list for the modification
3. value of the modified control signal to perform “BRGT -2, R1, R2”
4. the modified data path circuit of the CPU
5. the modified branch control unit of the CPU.

