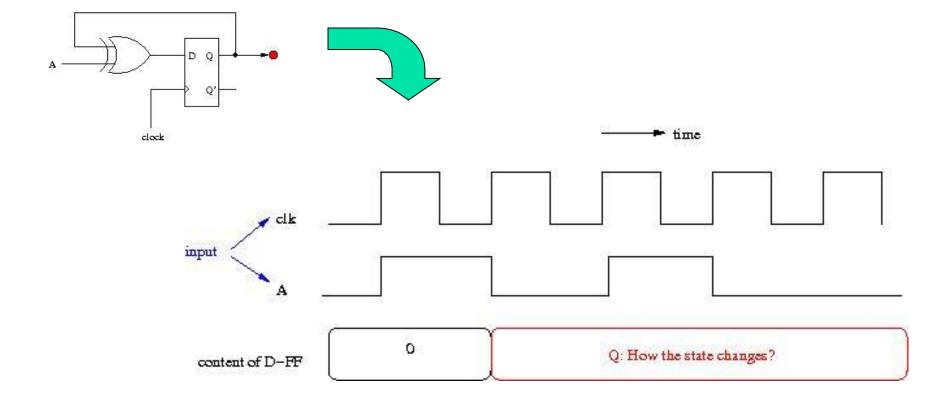
Lecture 01 (A)

Sequential Circuit Analysis

Draw the timing diagram from the circuit Section 5.4

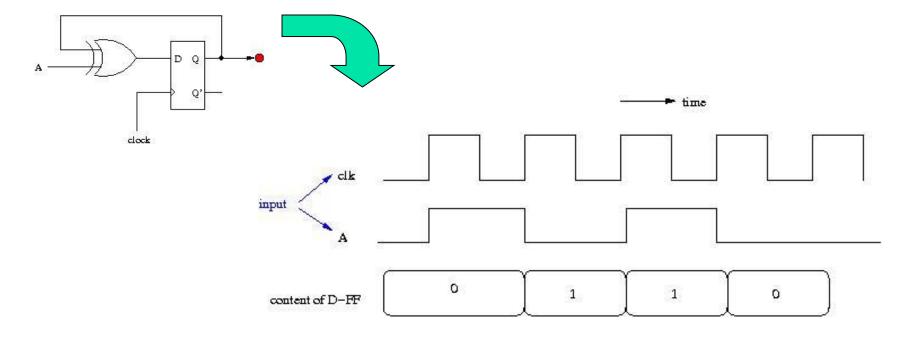
Today's Goal

- establish the ability to imagine how a circuit works
 - draw the timing waveform from a circuit diagram



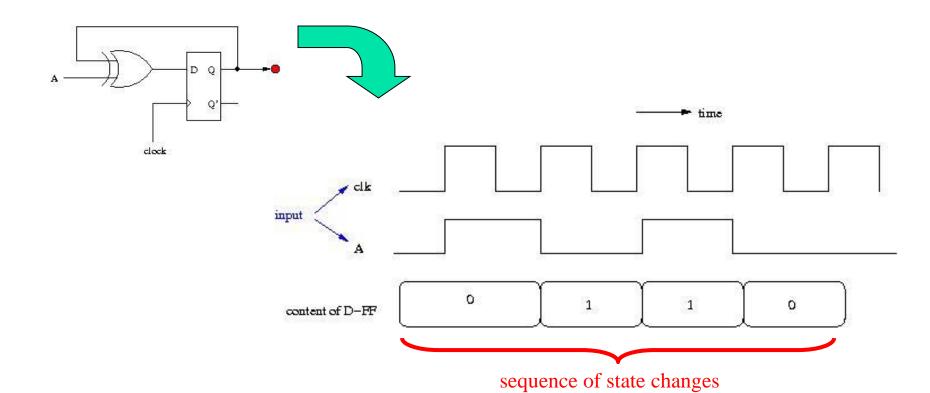
Today's Goal

- establish the ability to imagine how a circuit works
 - draw the timing waveform from a circuit diagram



Today's Goal

■ That's why we call it sequential circuit



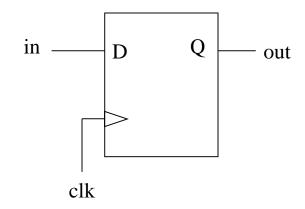
Materials coming from

Section 5.4

Preliminary: timing of logic elements (1)

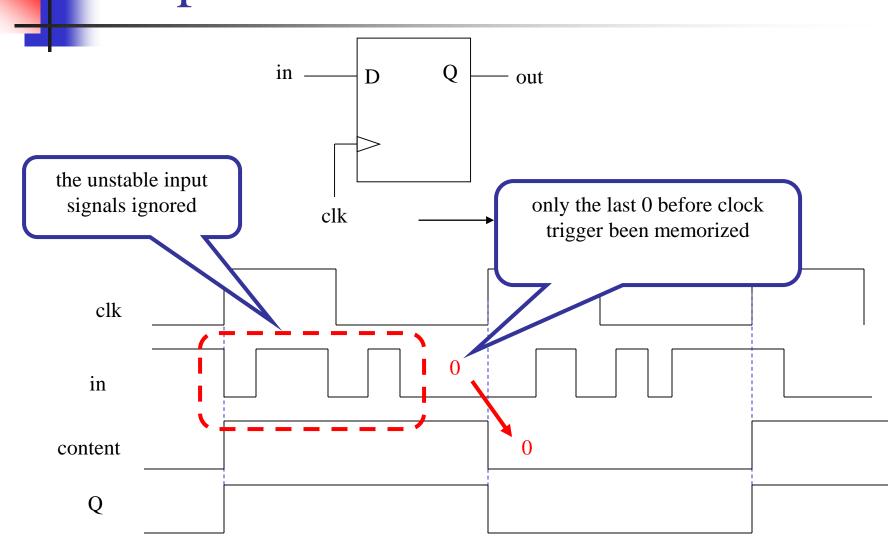
storage element: the D flip-flop

The D Flip-Flop

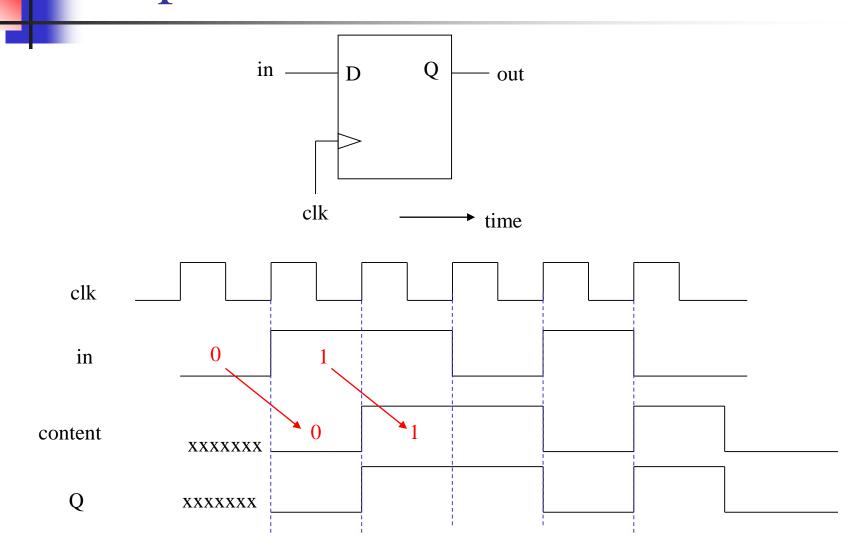


- Imagine that a D flip-flop is a box of 1-bit memory
- When the D flip-flop memorize the input?
 - at (positive) edge trigger of the clock (clk) signal
 - like a snapshot of a camera!

Timing Waveform of the D Flip-Flop



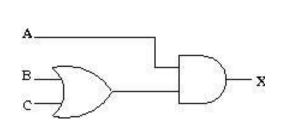
Timing Waveform of the D Flip-Flop

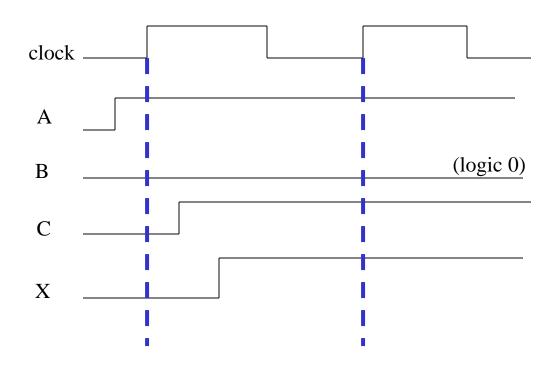


Preliminary: timing of logic elements (2)

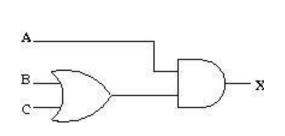
elements for combinational circuit

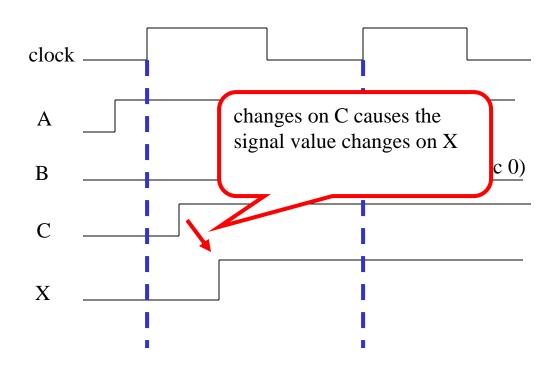
signal value changes immediately without waiting for the clock trigger



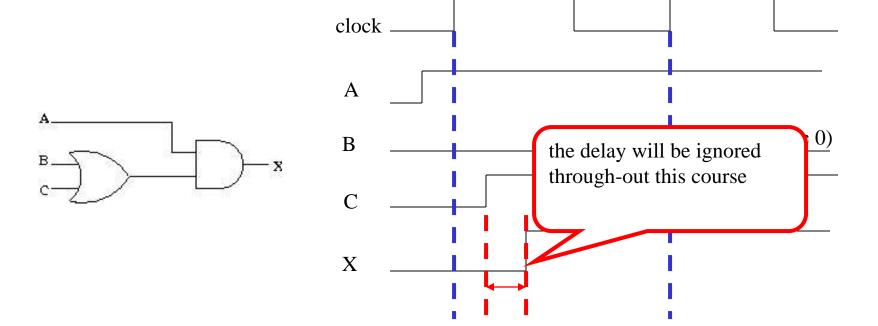


signal value changes immediately without waiting for the clock trigger

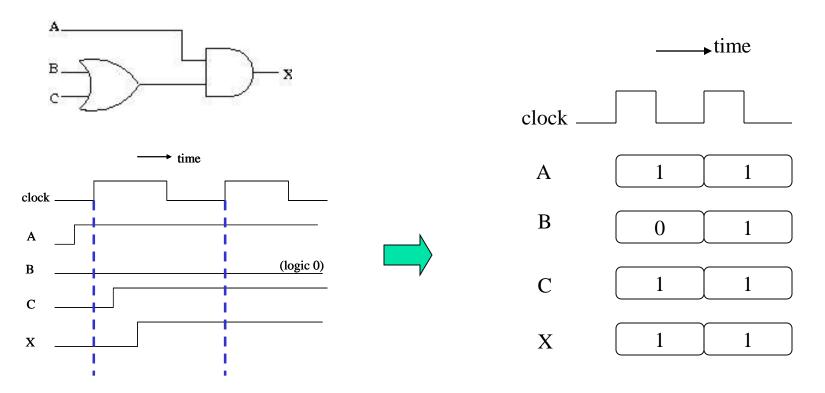




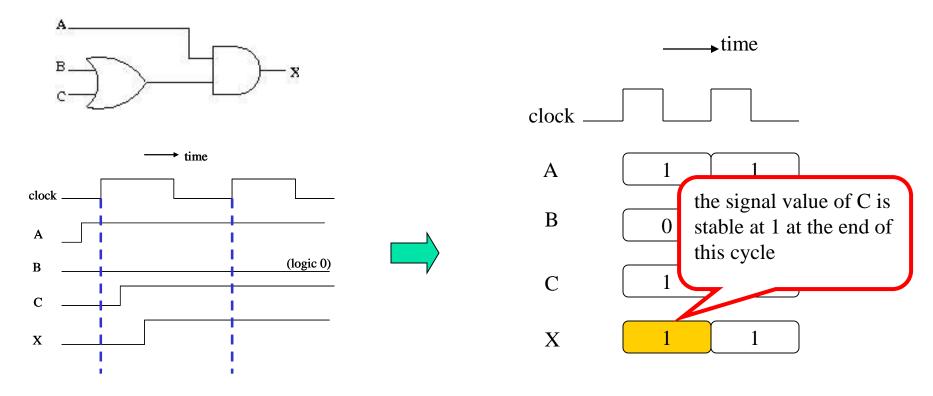
signal value changes immediately without waiting for the clock trigger



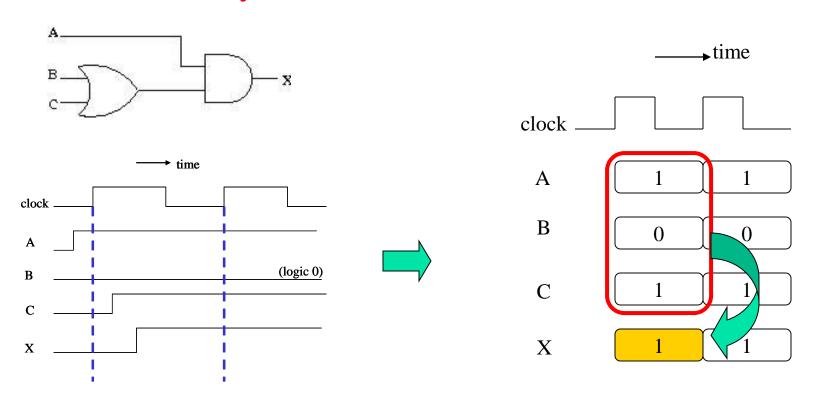
 we simply express the timing waveform cycle by cycle



 we simply express the timing waveform cycle by cycle



combinational circuit always gets the output at the same cycle!

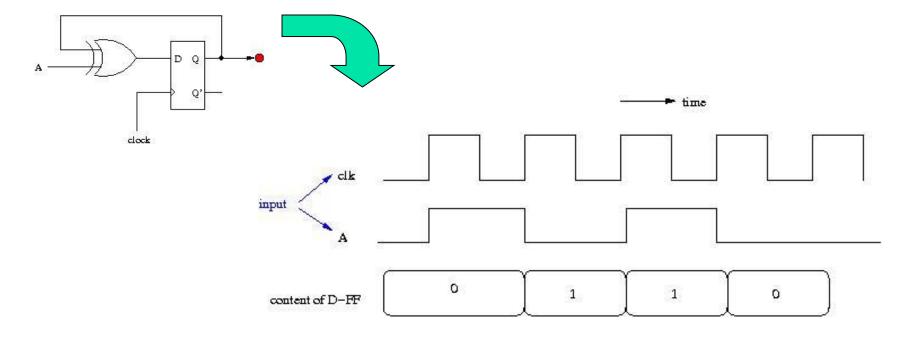


Now we begin

to draw the timing diagram from a sequential circuit

Recall your goal

- establish the ability to imagine how a circuit works
 - draw the timing waveform from a circuit diagram



Method to analyze a sequential circuit

- Step 1: derive input equations to D flip-flops
- Step 2: derive the state table
- Step 3: draw the state-diagram

Then you can draw the timing waveform from a state-diagram

Input equations to storage elements

for D flip-flops only

Example Circuit

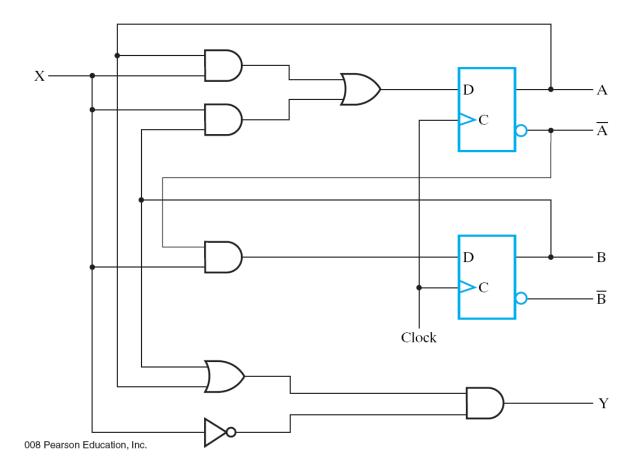
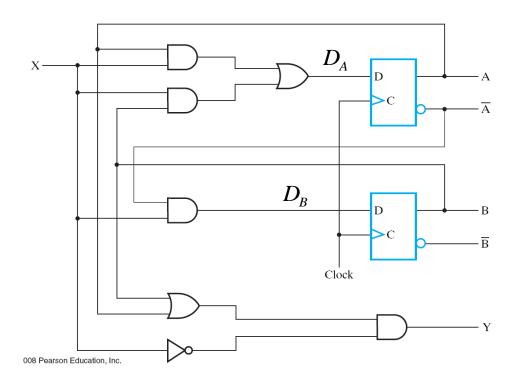


Figure 5-15 at page 241



- Boolean function to
 - determine the input to D-FFs
 - from current state (cycle t) and input signals



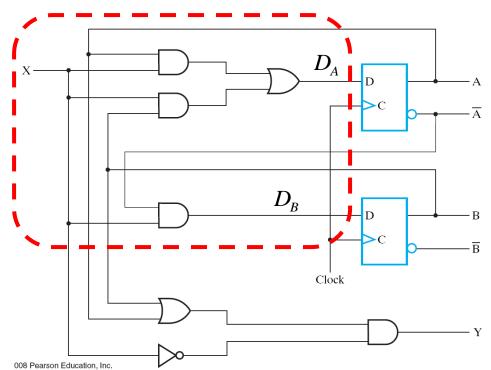
$$D_A = BoolFunc(A(t), B(t), X)$$

$$D_{\scriptscriptstyle B} = BoolFunc(A(t), B(t), X)$$



- ignore the D-FFs and consider the combinational circuit only
- simply write-down the Boolean equation of the combinational circuit





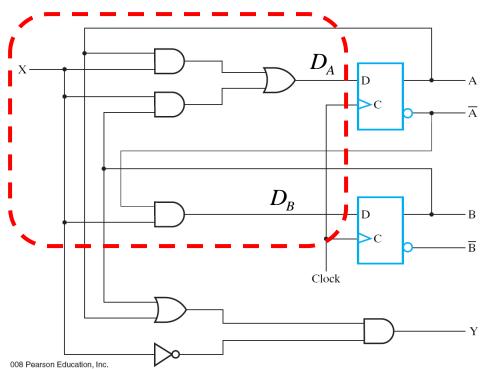
$$D_A = AX + BX$$

$$D_{\scriptscriptstyle R} = \overline{A}X$$



- ignore the D-FFs and consider the combinational circuit only
- simply write-down the Boolean equation of the combinational circuit





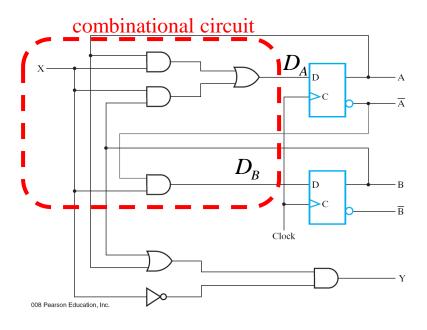
$$D_A = AX + BX$$

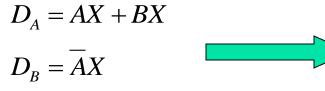
$$D_{B} = \overline{A}X$$

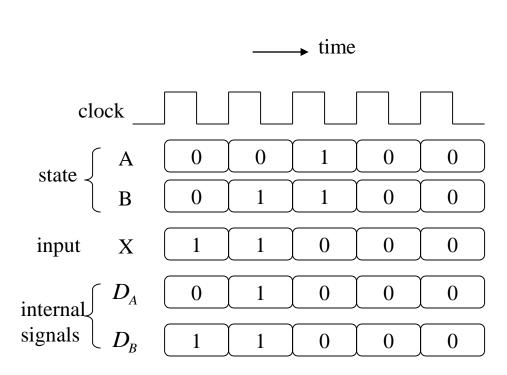
the input equation we want

Meaning of the input equations to D-FFs

Meaning of the input equations

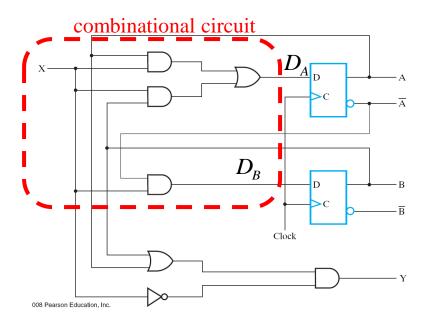




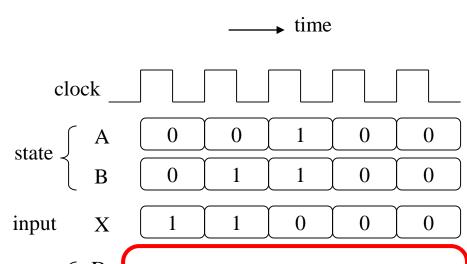


Meaning of the input equations

• the signal value at the end of the current cycle *t*



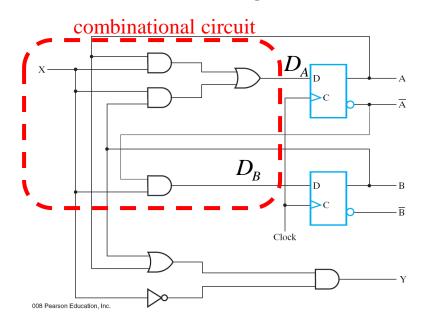




internal $\left\{egin{array}{l} D_A \ \\ D_B \end{array}
ight.$

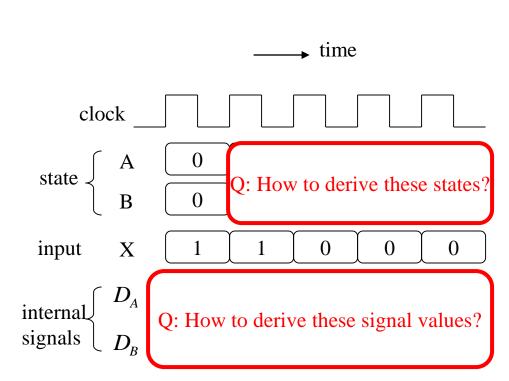
Q: How to derive these signal values?

Meaning of the input equations

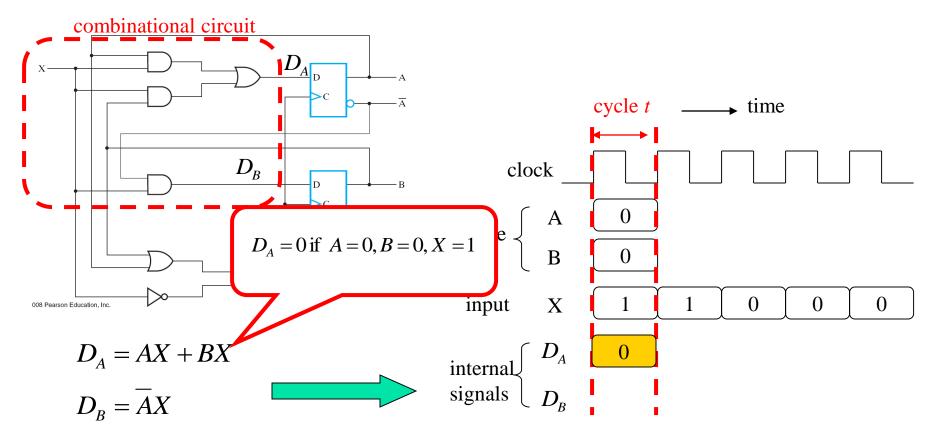


$$D_A = AX + BX$$

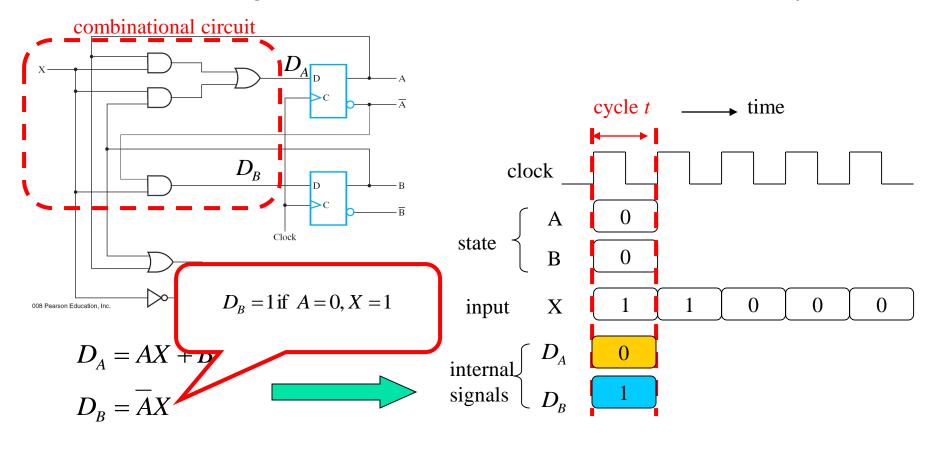
$$D_B = \overline{A}X$$



Meaning of the input equations

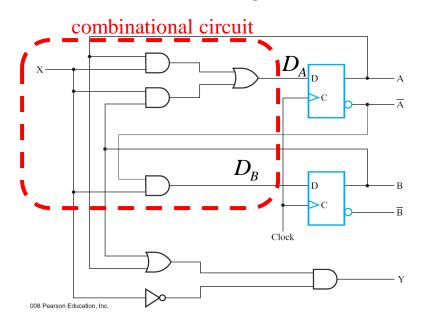


Meaning of the input equations



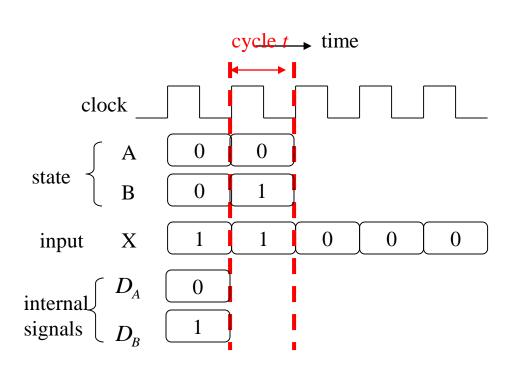


Meaning of the input equations

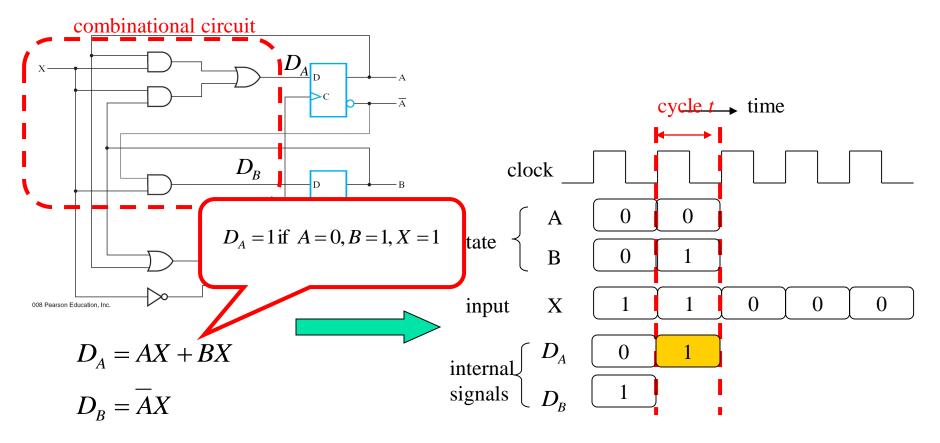


$$D_A = AX + BX$$

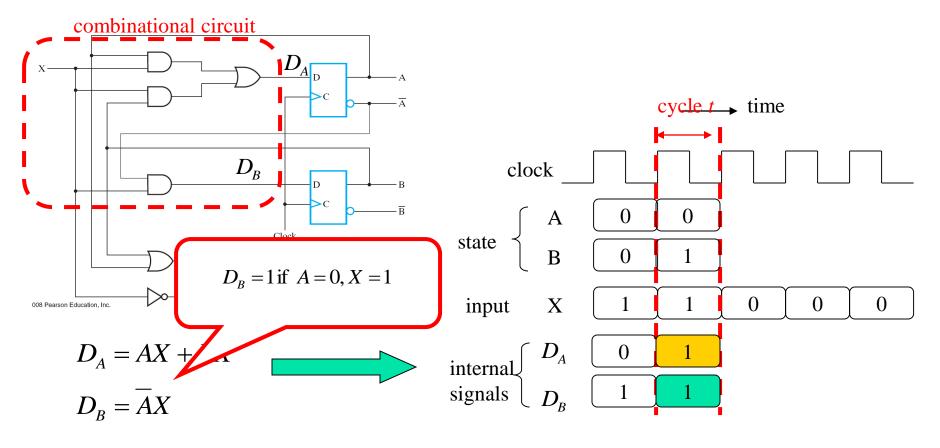
$$D_B = \overline{A}X$$



Meaning of the input equations



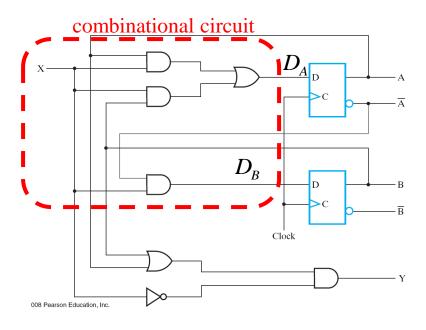
Meaning of the input equations



Meaning of the input equations

the signal value at the end of the current cycle t

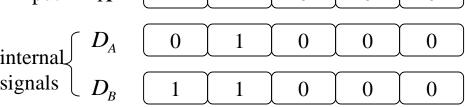
clock



$$D_A = AX + BX$$
$$D_B = \overline{A}X$$

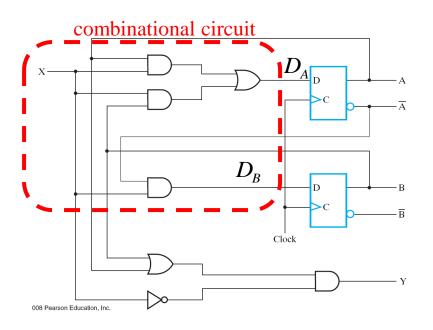
state $\begin{cases} A & 0 & 0 & 1 & 0 & 0 \\ B & 0 & 1 & 1 & 0 & 0 \\ input & X & 1 & 1 & 0 & 0 & 0 \\ \hline \begin{pmatrix} D & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ \end{pmatrix}$

Derive remaining part by yourself!



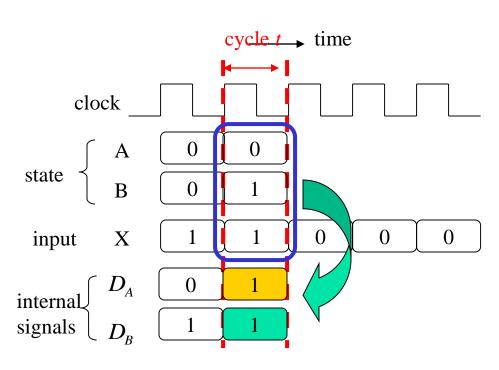
Rule of thumb

a combinational circuit always generates the outputs at the same cycle



$$D_A = AX + BX$$

$$D_B = \overline{A}X$$



State table of a sequential circuit

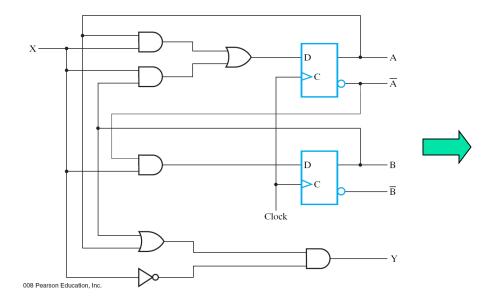
Method to analyze a sequential circuit

- Step 1: derive input equations to D flip-flops
- Step 2: derive the state table
- Step 3: draw the state-diagram

Then you can draw the timing waveform from a state-diagram



- like a truth table
- rules to determine the state at cycle t+1 from
 - (1) state at cycle t, and
 - (2) input signals at cycle *t*
- state: content of D-FFs



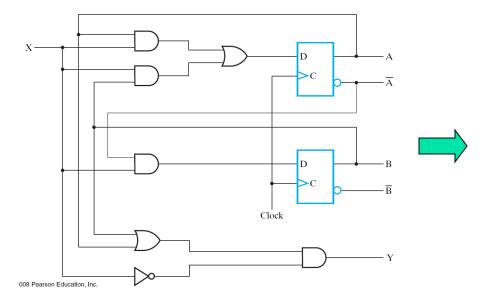
■ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Nex	Output	
Α	В	X	A	В	Υ
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0
	1	1	1	Ü	J



What is a state table?

- like a truth table
- rules to determine the state at cycle t+1 from
 - (1) state at cycle t, and
 - (2) input signals at cycle t
- state: content of D-FFs



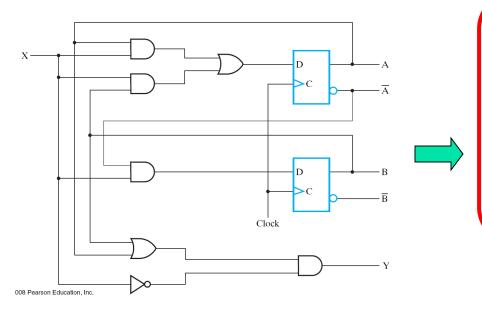
■ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Nex	Output	
Α	В	X	Α	В	Υ
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0
1	1	1	1	0	0

enumerate all possible conditions



- like a truth table
- rules to determine the state at cycle t+1 from
 - (1) state at cycle t, and
 - (2) input signals at cycle t
- state: content of D-FFs



state at cycle t state at cycle t+1

Prese	ent State	Input	!	Nex	t State	Output
Α	В	x	Ľ	Α	В	Υ
0	0	0	Γ.	0	0	0
0	0	1		0	1	0
0	1	0	ı	0	0	1
0	1	1	'	1	1	0
1	0	0		0	0	1
1	0	1	١.	1	0	0
1	1	0	ı	0	0	1
1	1	1		1	0	0

enumerate all possible conditions



- timing waveform can be drawn from the state table
- TABLE 5-1 State Table for Circuit of Figure 5-15

Prese	ent State	Input	Nex	t State	Outpu	t					
Α	В	X	A	В	Υ						
0	0	0	0	0	0						
0	0	1	0	1	0						
0	1	0	0	0	1				→ time	,	
0	1	1	1	1	0				— tillic		
1	0	0	0	0	1						
1	0	1	1	0	0		— 1				
1	1	0	0	0	1	clock					
1	1	1	1	0	0				J	J	J
						A	0			9	
						state B	0			•	
										~	~
						X	1	1	0	\downarrow 0	$\begin{bmatrix} 0 \end{bmatrix}$



timing waveform can be drawn from the state table

☐ TABLE 5-1 State Table for Circuit of Figure 5-15

Prese	ent State	Input	Nex	t State	Outpu	ıt					
Α	В	x	A	В	Y	_					
0	0	0	0	0	0						
0	0	1	0	1	0						
0	1	0	0	O	1				→ time	1	
0	1	1	1	1	0				— tillic	,	
1	0	0	0	0	1						
1	0	1	1	0	0						
1	1	0	0	0	1	clock					
1	1	1	1	0	0] []	J [
						A	0	0	1	0	0
						state B	0	$ \overline{1} $	1	0	0
						V	1	1	Ĭ o) o	Ϋ́ Λ

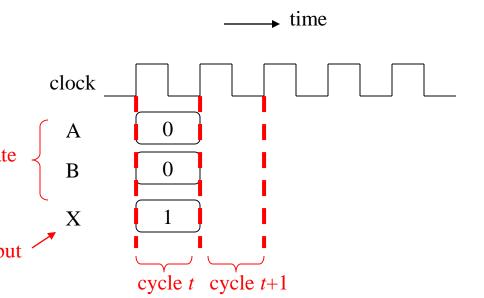


■ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input		Nex	Output	
A	В	x		A	В	Υ
0	0	0		0	0	0
0	0	1		0	1	0
0	1	0		0	0	1
0	1	1		1	1	0
1	0	0		0	0	1
1	0	1		1	0	0
1	1	0		0	0	1
1	1	1		1	0	0
			_		~	'
cycle t			cycle <i>t</i> +1			;

• rules to determine the state at cycle t+1 from

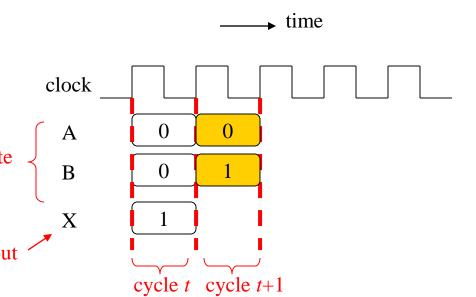
- state at cycle *t*, and
- input signals at cycle *t*



■ TABLE 5-1 State Table for Circuit of Figure 5-15

Prese	ent State	Input	Nex	t State	Output
A	В	x	A	В	Y
0	0	0	_0	0	0
0	0	1	0	1	0
U	1	0	0	U	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0
				~	,
	cycle t		cycl	e <i>t</i> +1	
	•				

- rules to determine the state at cycle t+1 from
 - state at cycle t, and
 - input signals at cycle *t*



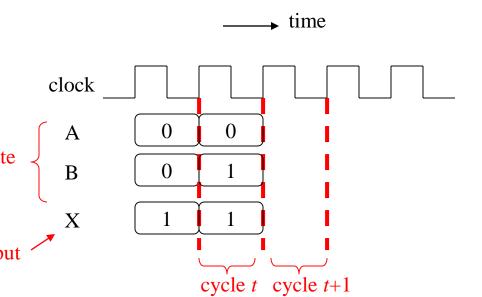


☐ TABLE 5-1 State Table for Circuit of F gure 5-15

Present State		Input	Nex	Next State		
Α	В	x	A	В	Y	
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	0	1	
0	1	1	1	1	0	
1	0	0	0	0	1	
1	0	1	1	0	0	
1	1	0	0	0	1	
1	1	1	1	0	0	
				~	,	
	cycle <i>t</i>		cycle	e <i>t</i> +1	:	



- rules to determine the state at cycle t+1from
 - state at cycle t, and
 - input signals at cycle t

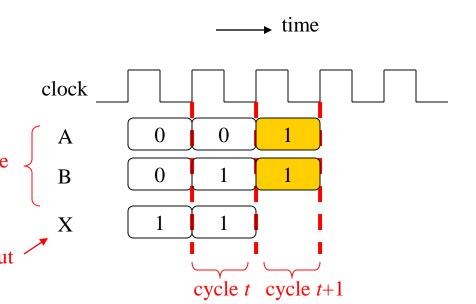




☐ TABLE 5-1 State Table for Circuit of Figure 5-15

	Input	Nex	Next State		
В	X	A	В	Y	
0	0	0	0	0	
0	1	0	1	0	
1	0		0	1	
1	1	1	1	0	
0	0	0	0	1	
0	1	1	0	0	
1	0	0	0	1	
1	1	1	0	0	
			~	ı	
cycle t		cycl	e <i>t</i> +1		
	0 0 1 1 0 0 1 1	0 0 0 1 1 0 1 1 0 0 0 0 1 1 0 1 1	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0	

- rules to determine the state at cycle t+1 from
 - state at cycle t, and
 - input signals at cycle t



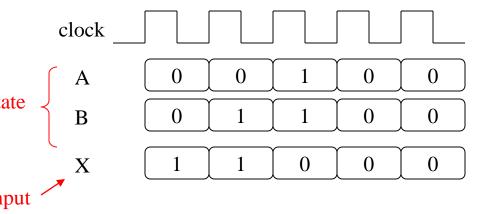


- timing waveform can be drawn from the state table
- TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Nex	Output	
A	В	X	A	В	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

complete the timing waveform by yourself!

time



How to derive the state table

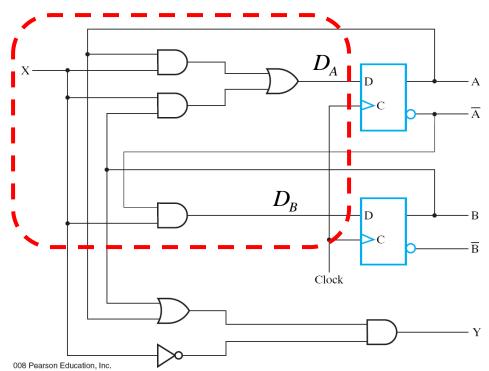
Method to analyze a sequential circuit

- Step 1: derive input equations to D flip-flops
- Step 2: derive the state table
- Step 3: draw the state-diagram

Then you can draw the timing waveform from a state-diagram



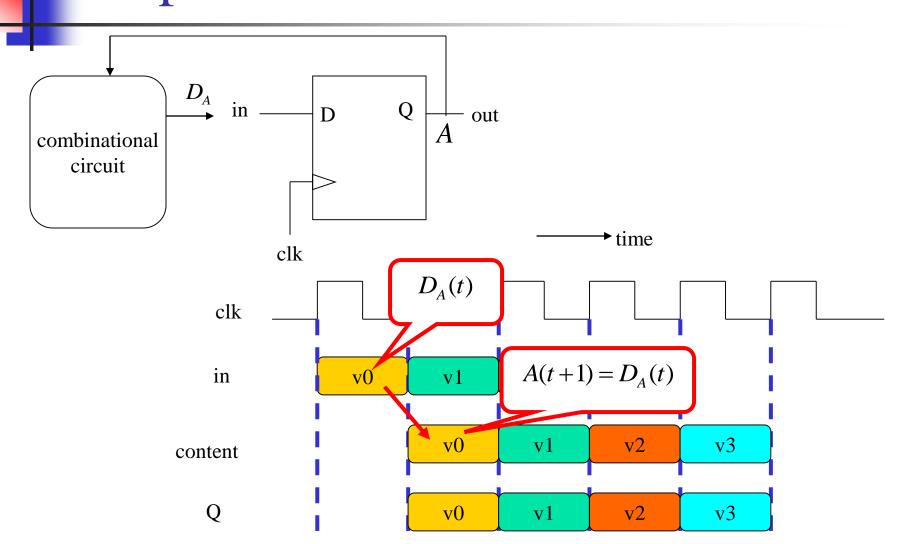
- Rule of thumb:
 - the input to a D-FF at cycle t equals the state of D-FF at cycle t+1



$$A(t+1) = D_A(t) = A(t)X(t) + B(t)X(t)$$

$$B(t+1) = D_B(t) = \overline{A(t)}X(t)$$

Timing Waveform of the D Flip-Flop



How to derive the state-table

check the rules and the state-table



 $D_A(t)=0$

$$D_{A}$$
 D_{A}
 D_{C}
 D_{B}
 D_{C}
 D_{C

$$A(t+1) = D_A(t) = A(t)X(t) + B(t)X(t)$$

$$B(t+1) = D_B(t) = \overline{A(t)}X(t)$$

$$D_B(t) = 1$$

state at cycle t

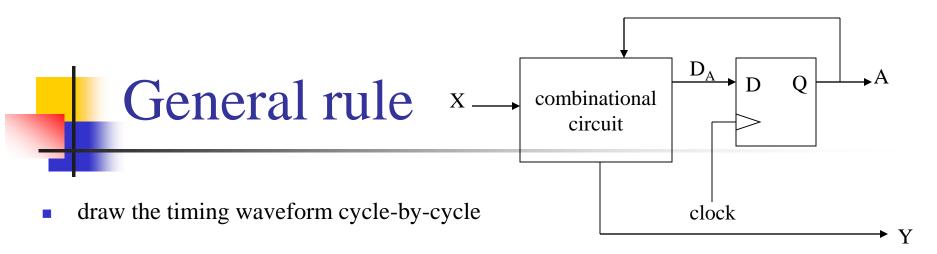
state at cycle t+1

State Table for Circuit of Figure 5-15

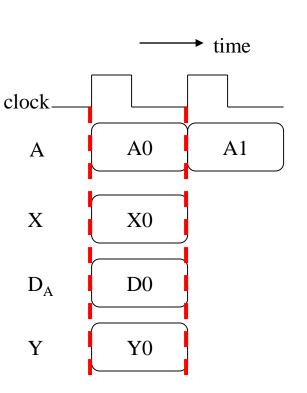
Present State		Input	Nex	Output	
A	В	x	A	В	Υ
0	0	0	-	0	0
0	0	1	0	1	0
Û	i	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0
1	1	1	1	U	U

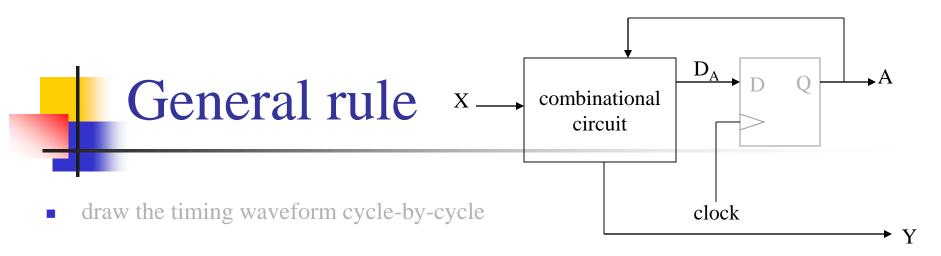
Put it all together

derive the state table and the timing waveform

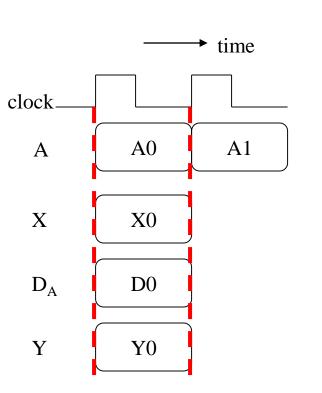


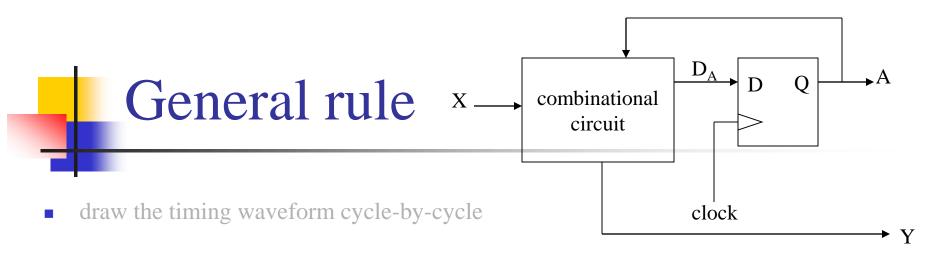
- Step 1: remove D-FFs and derive Boolean equations for the combinational circuit
 - state A is an input to the combinational circuit
- Step 2: derive outputs of the combinational circuit at the same cycle
 - inputs to D-FFs are outputs of the combinational circuit
 - the combinational circuit generates output at the same cycle
- Step 3: derive the next state of D-FFs
 - $\bullet A(t+1) = D_A(t)$



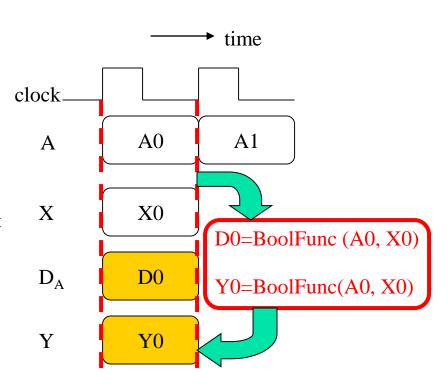


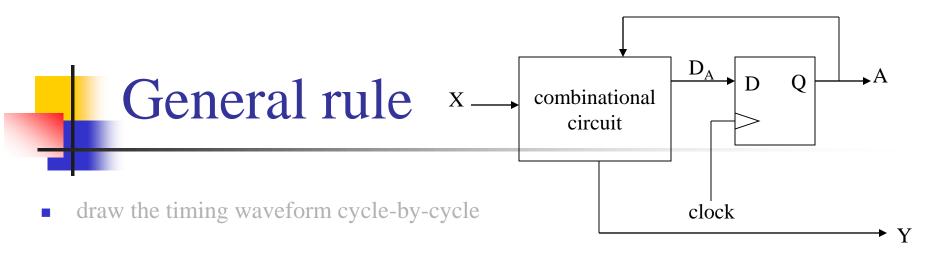
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- Step 3: derive the next state of D-FFs
 - $\bullet \quad A(t+1) = D_A(t)$



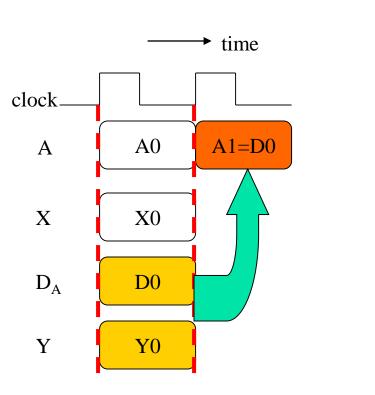


- Step 1: remove D-FFs and derive Boolean equations for the combinational circuit
 - state A is an input to the combinational circuit
- Step 2: derive outputs of the combinational circuit at the same cycle
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 - the combinational circuit generates output at the same cycle
- Step 3: derive the next state of D-FFs
 - $\bullet \quad A(t+1) = D_A(t)$





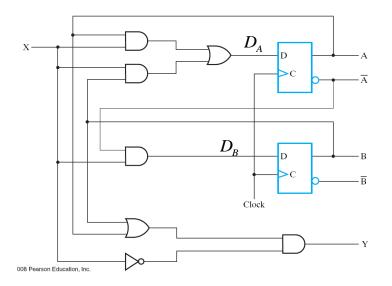
- Step 1: remove D-FFs and derive Boolean equations for the combinational circuit
 - state A is an input to the combinational circuit
- Step 2: derive outputs of the combinational circuit at the same cycle
 - inputs to D-FFs are outputs of the combinational circuit
 - the combinational circuit generates output at the same cycle
- Step 3: derive the next state of D-FFs
 - $\bullet \quad A(t+1) = D_A(t)$



Rule of Thumb

 Combinational Circuit: generate outputs at the same cycle to inputs

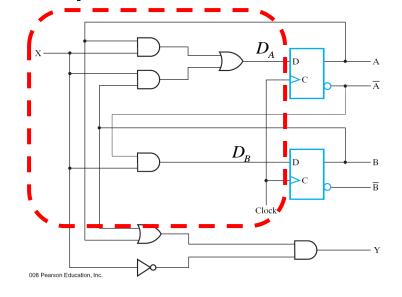
- D Flip-Flop: $A(t+1) = D_A(t)$
 - state changes at the next cycle



☐ TABLE 5-1 State Table for Circuit of Figure 5-15

SI	ate Table Io	or Circuit of F	Figure 5-15				
Pres	ent State	Input	Nex	t State	Output		
A	В	X	A	В	Υ		
0	0	0					
0	0	1					
0	1	0					
0	$\frac{1}{0}$	1		?			
1 1	0	0 1					
1	1	0					
1	1	1)		
clo	ock						
state {	A (B (0		?			
input	X	1 1	0	0	0		
nternal ignals	$egin{array}{c} D_A \ D_B \end{array}$?				

combinational circuit



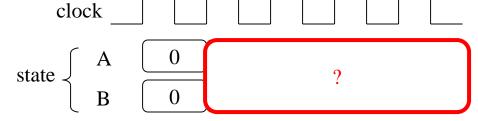
$$D_A = AX + BX$$

$$D_B = \overline{A}X$$

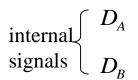
☐ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
Α	В	x	A	В	Y
0	0	0			
0	0	1			
0	1	0			
0	1	1		9	
1	0	0		?	
1	0	1			
1	1	0			
1	1	1			

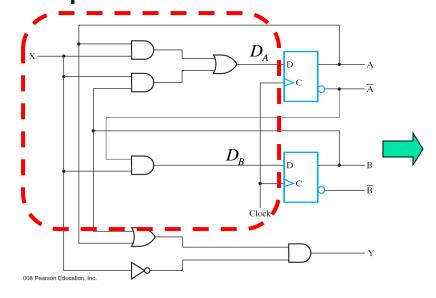




input X 1 1 0 0 0

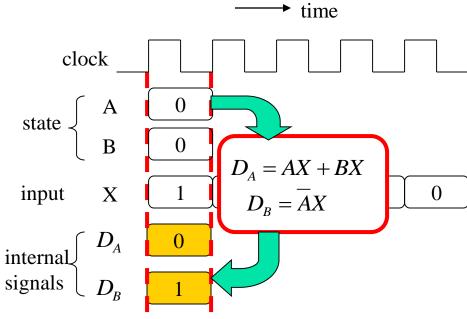


?

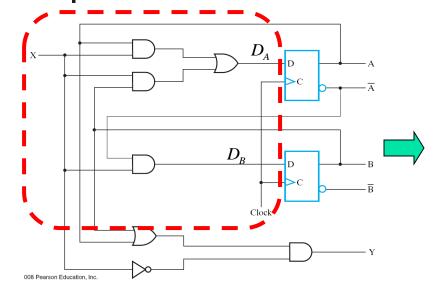


☐ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
A	В	X	A	В	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

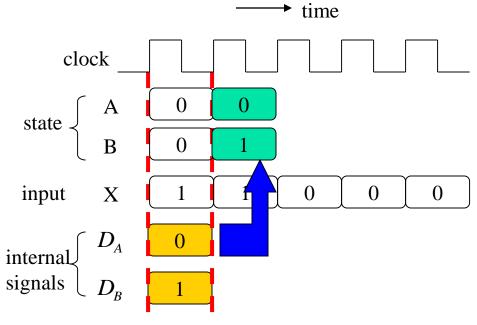


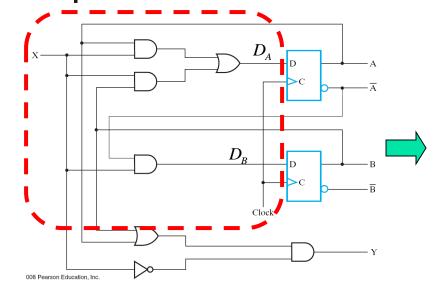




☐ TABLE 5-1 State Table for Circuit of Figure 5-15

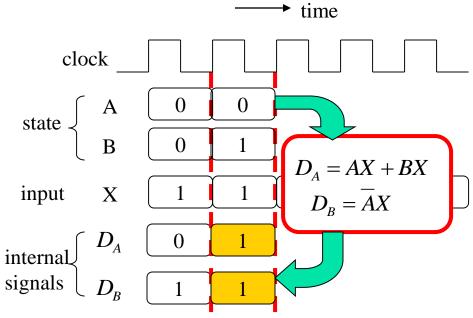
Present State		Input	Next State		Output	
A	В	x	A	В	Υ	
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	-0	1	
0	1	1	1	1	0	
1	0	0	0	0	1	
1	0	1	1	0	0	
1	1	0	0	0	1	
1	1	1	1	0	0	



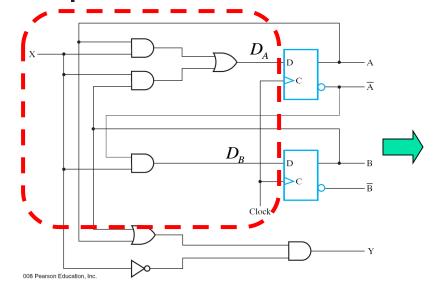


☐ TABLE 5-1
State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
A	В	X	A	В	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

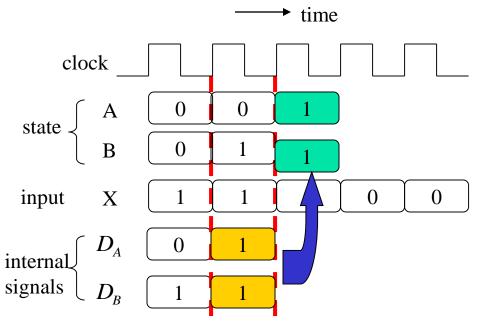


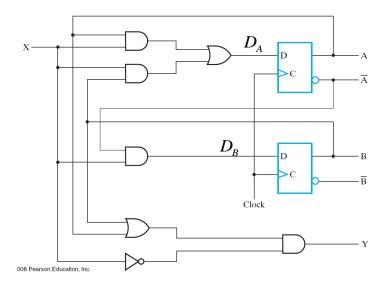
combinational circuit



☐ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
A	В	x	A	В	Υ
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
Ι	U	0	U	U	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0





Complete by yourself!

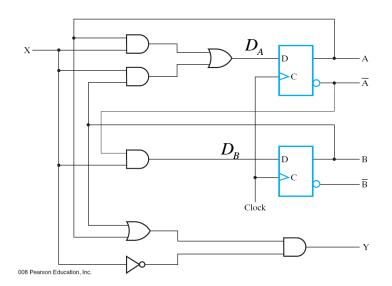
☐ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
Α	В	x	A	В	Υ
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

_____ time

clock

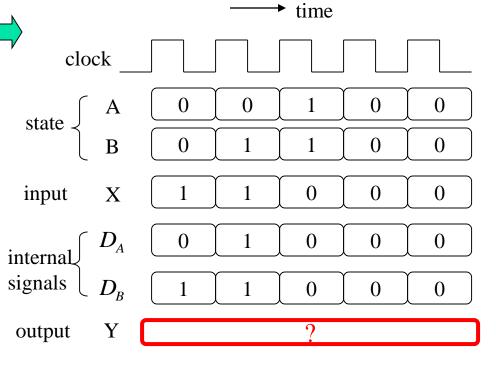
state \{	A	0	0	1	0	$\begin{bmatrix} 0 \end{bmatrix}$
state 3	В	0	1	1	0	0
input	X	1	1	0	0	0
internal	D_A	0	1	0	0	0
signals	D_n	1	1	0	0	0



Q: How about output Y?

☐ TABLE 5-1 State Table for Circuit of Figure 5-15

			Next State		Output
Α	В	X	A	В	Υ
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0



State diagram

finite-state machine model for digital circuit

Method to analyze a sequential circuit

- Step 1: derive input equations to D flip-flops
- Step 2: derive the state table
- Step 3: draw the state-diagram

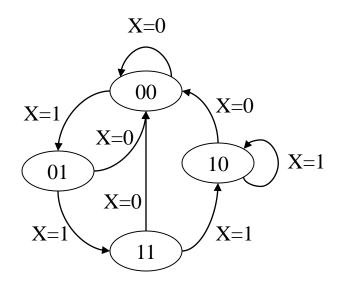
Then you can draw the timing waveform from a state-diagram

What is the state diagram?

a graphical way to represent the state table

TABLE 5-1	
State Table for Circuit of F	gure 5-15

Present State		Input	Next State		Output	
Α	В	x	A	В	Υ	
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	0	1	
0	1	1	1	1	0	
1	0	0	0	0	1	
1	0	1	1	0	0	
1	1	0	0	0	1	
1	1	1	1	0	0	

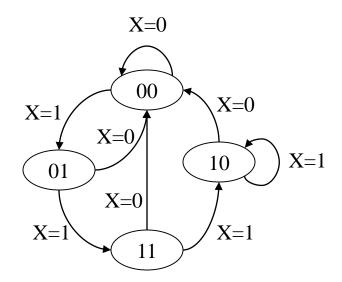




- node (state): content of the D-FFs
- edge: state transition upon receiving input signal value

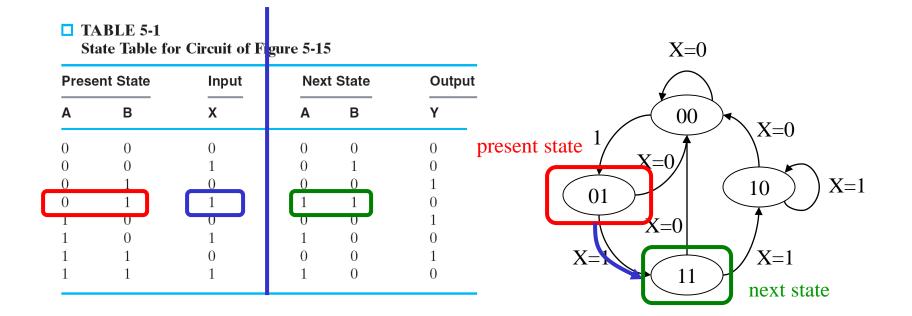
■ TABLE 5-1 State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output	
A	В	x	A	В	Y	
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	0	1	
0	1	1	1	1	0	
1	0	0	0	0	1	
1	0	1	1	0	0	
1	1	0	0	0	1	
1	1	1	1	0	0	



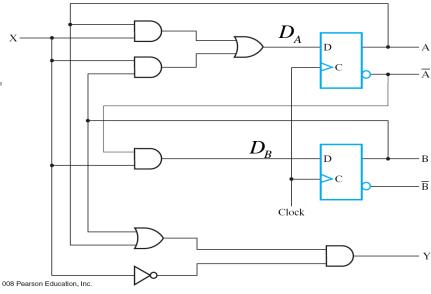


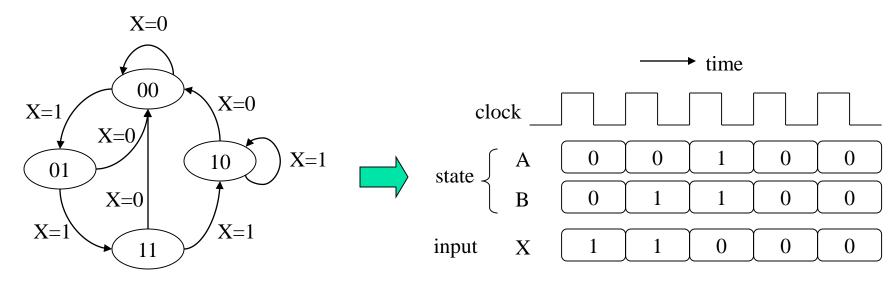
- node (state): content of the D-FFs
- edge: state transition upon receiving input signal value



Draw timing waveform from







Draw timing waveform from



