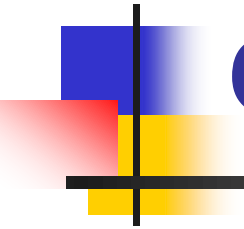
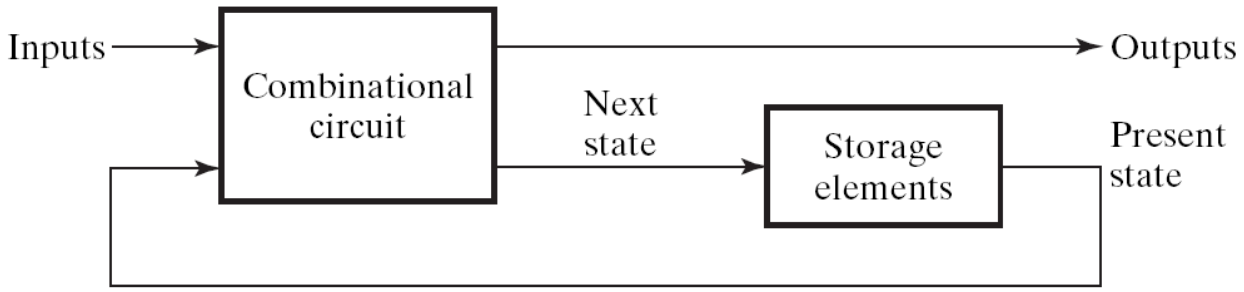
Lecture 01B

Timing Analysis of Sequential Circuit



What is a sequential circuit

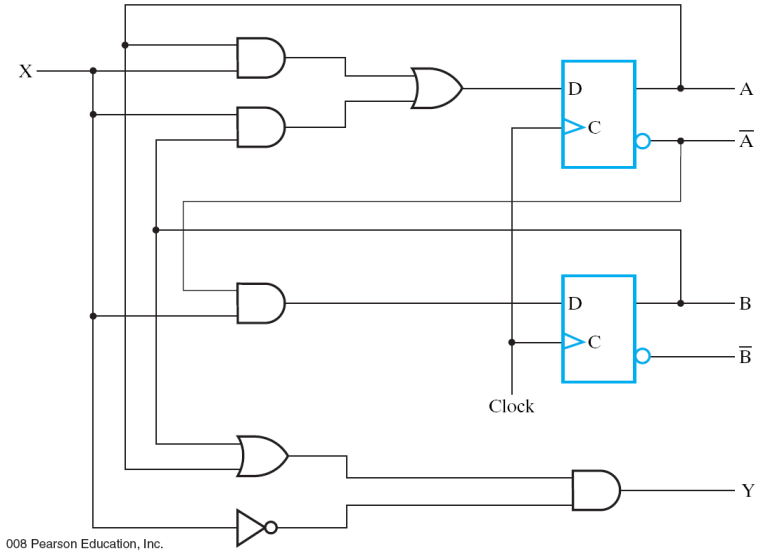
- Sequential Circuit:
  - a digital circuit with storage element to memorize current state
  - Figure 5-1:

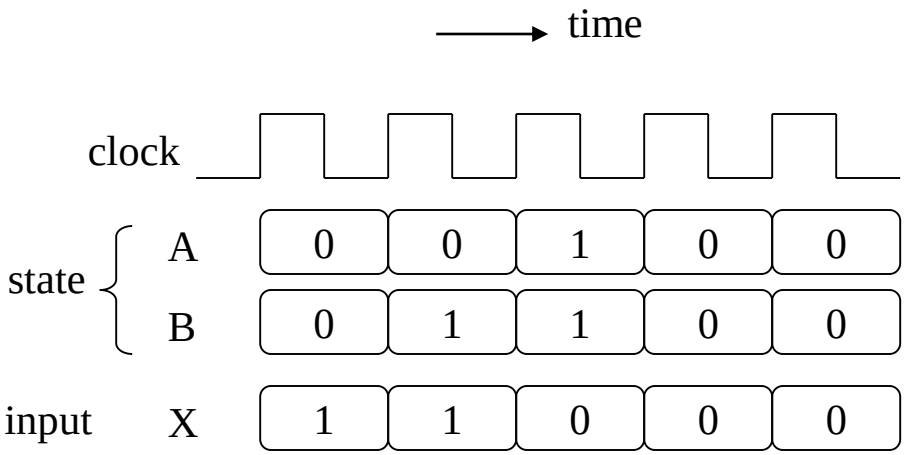


- the counter part -- Combinational Circuit
  - a digital circuit without storage element

The key to design hardware

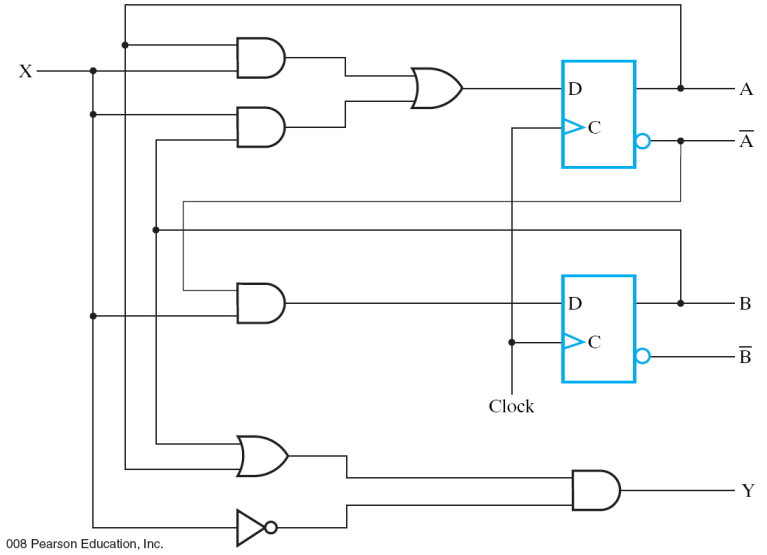
- imagine how a circuit works

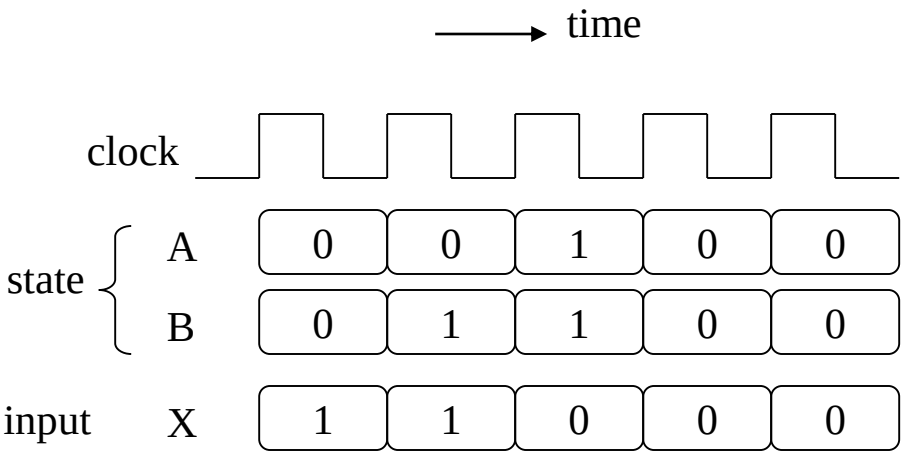




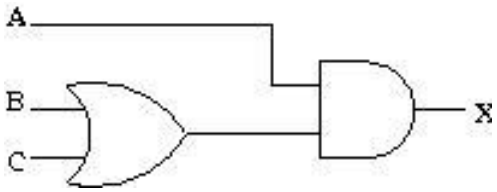
Note: we are talking about Synchronous Clocked Circuit

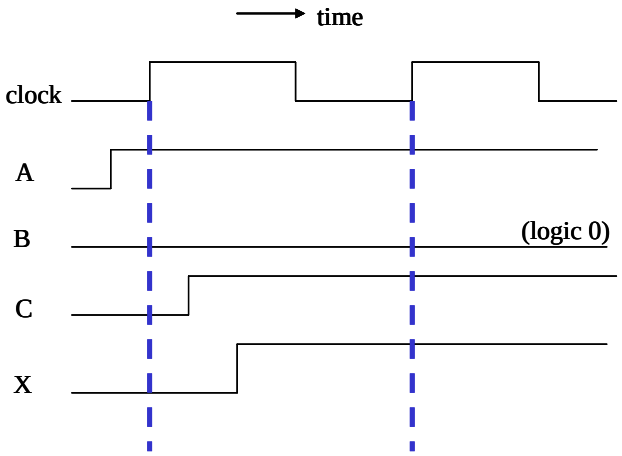
- All flip flops receive the same clock signal



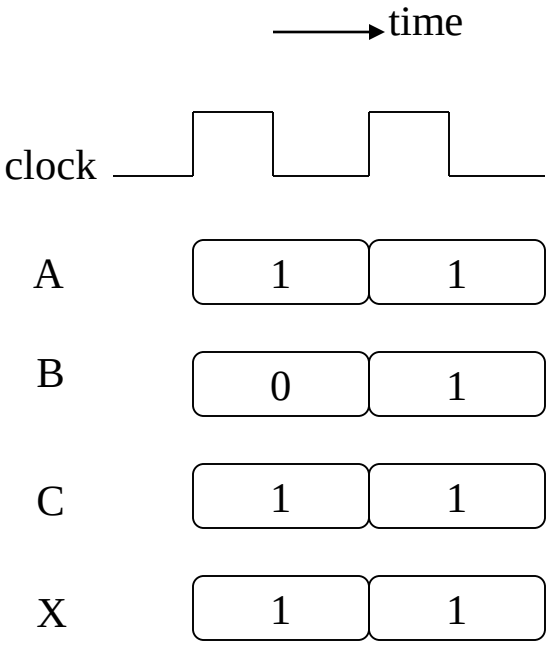


Cycle-based vs. Actual Timing

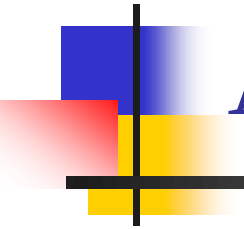




Actual Timing



Cycle-based reasosning

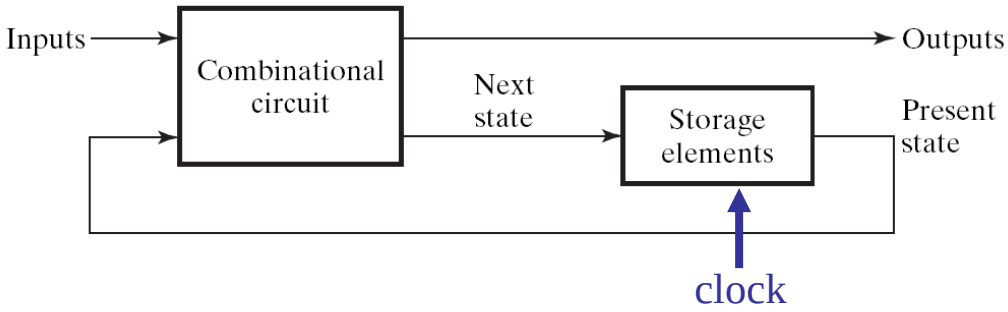


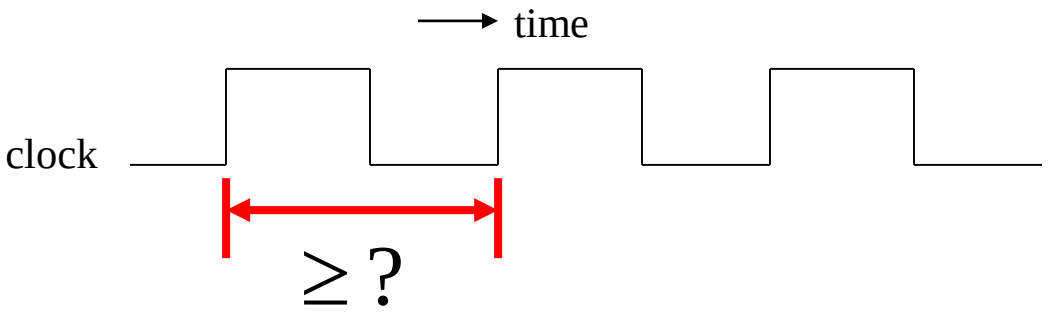
Analysis for actual timing

minimum clock period time

Core Question

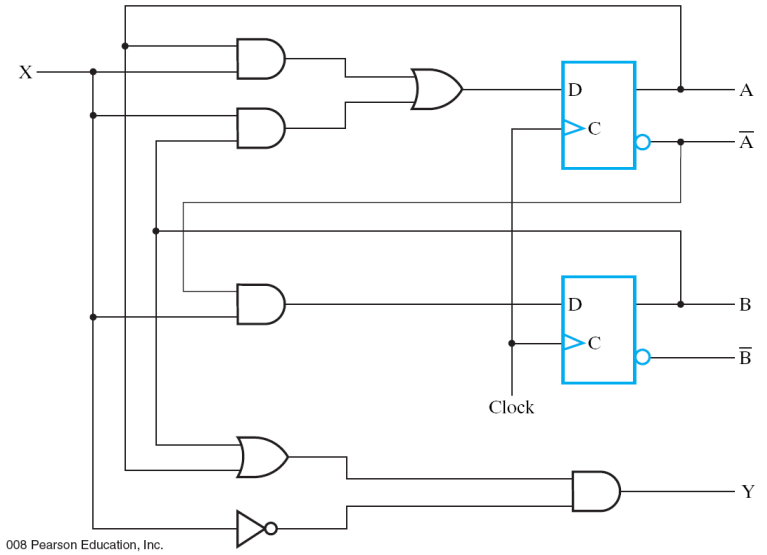
- What's the minimum clock period time to make the circuit works correctly?

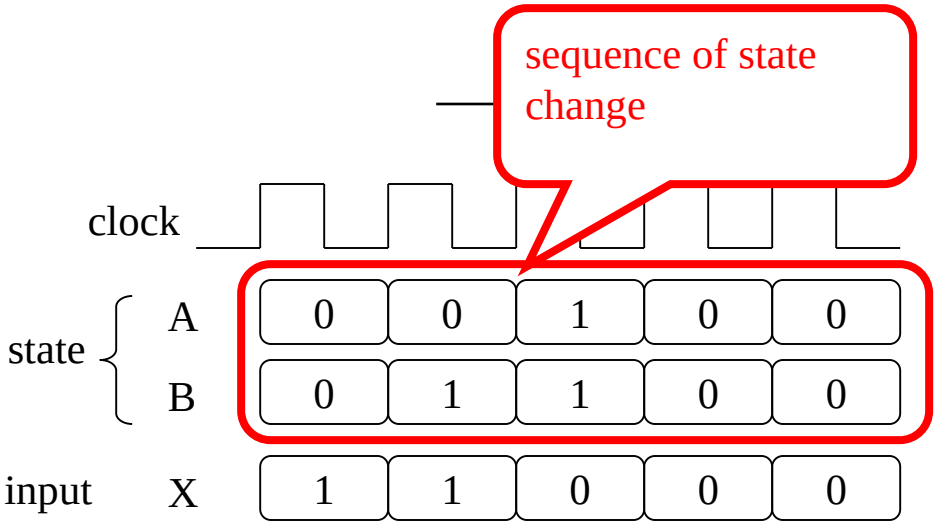




What's the clock for?

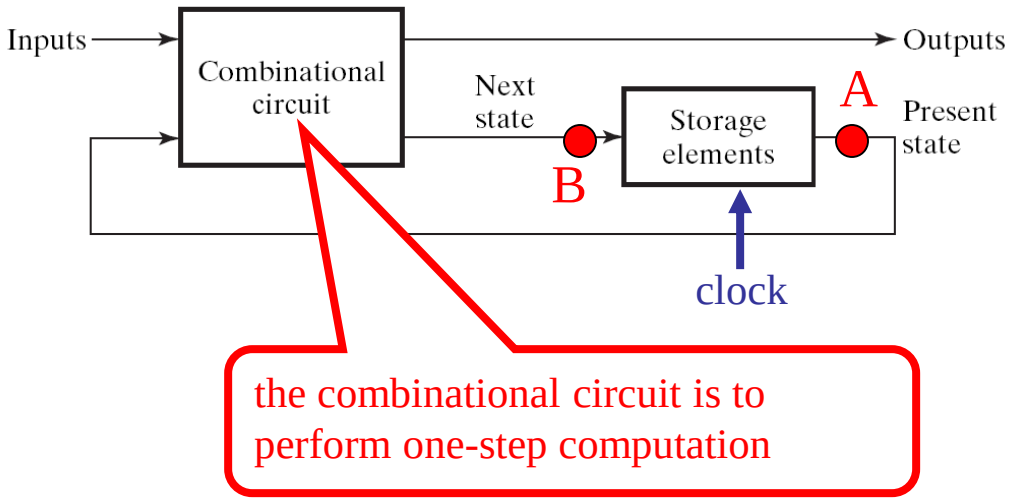
- Answer: to make the circuit doing step-by-step computation
  - clock signal is fed to all flip flops of the circuit
  - to let a sequential circuit performs its task in step-by-step manner
  - forms a sequence of state change on flip flops
    - imagine the flip flops as variables for programming





Core Question

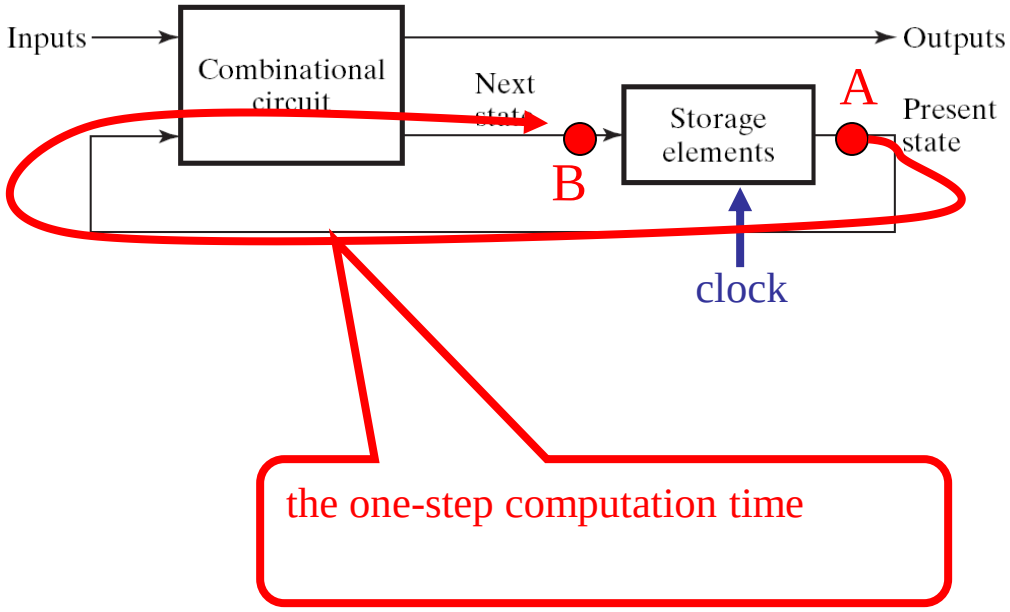
- What's the maximum one-step computation time?



$$delay(A, B) \leq ?$$

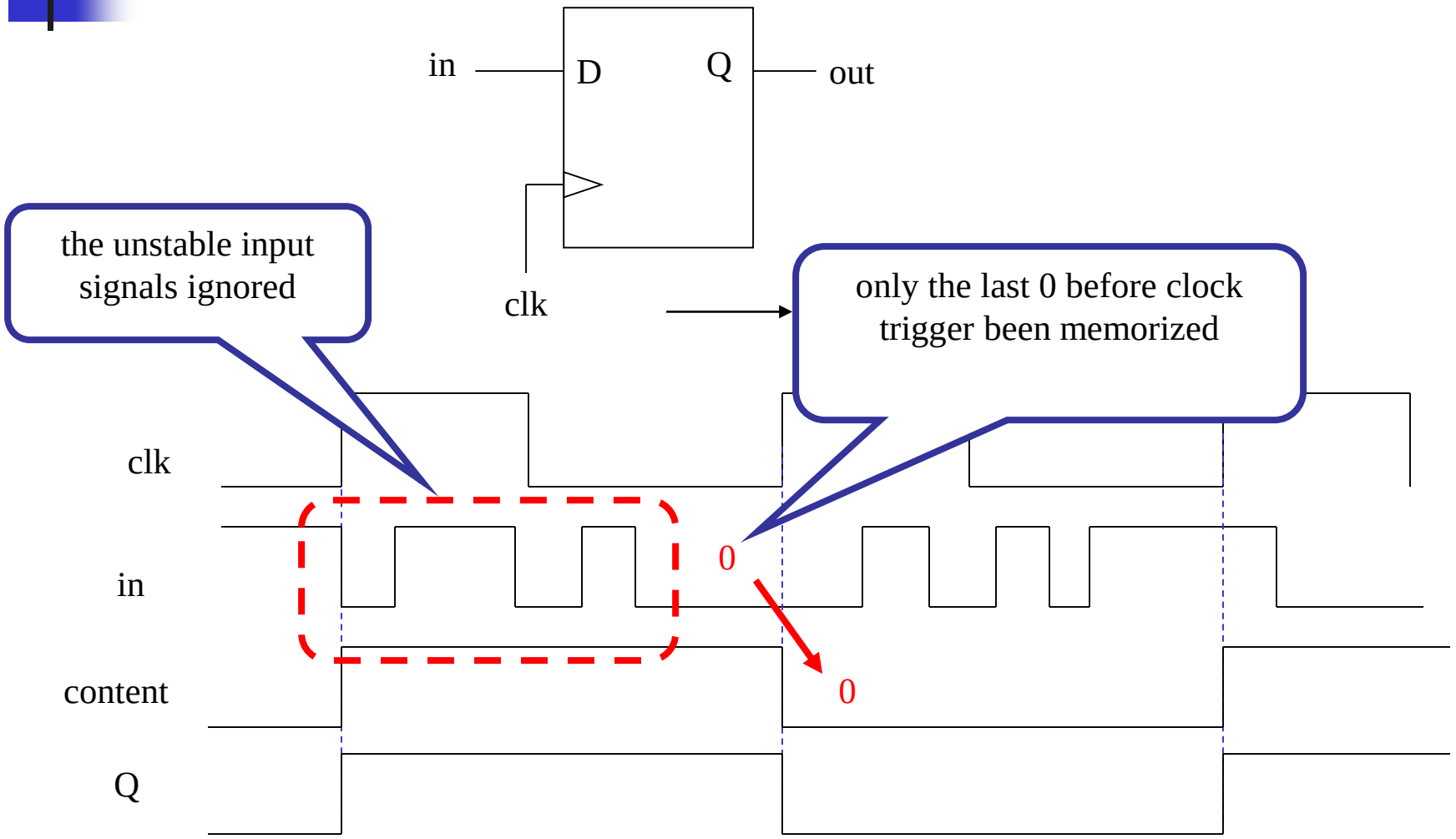
Core Question

- What's the maximum one-step computation time?



$$delay(A, B) \leq ?$$

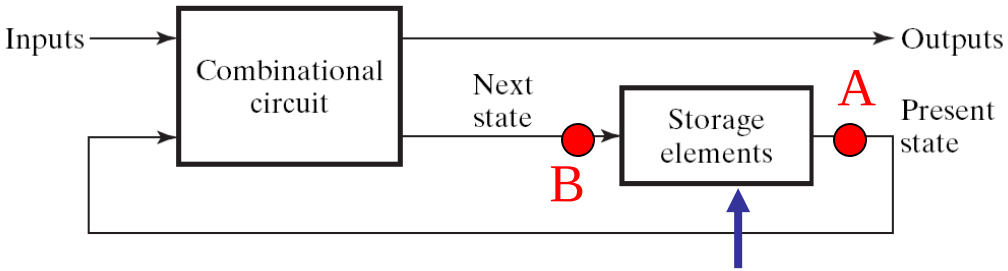
Recall: property of D flip-flop

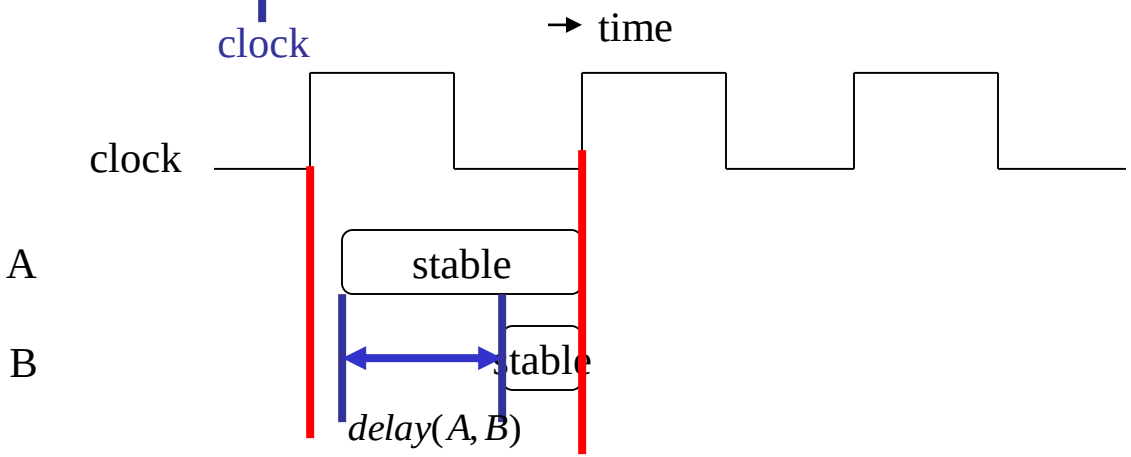


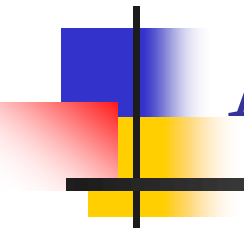
Core Question

- What's the maximum one-step computation time?

$$delay(A, B) \leq (\text{clock period time})$$



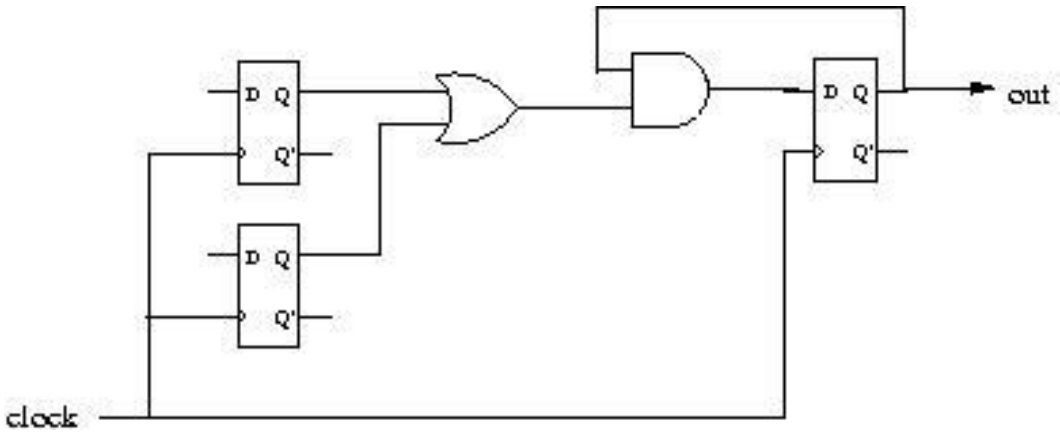




Analysis Example

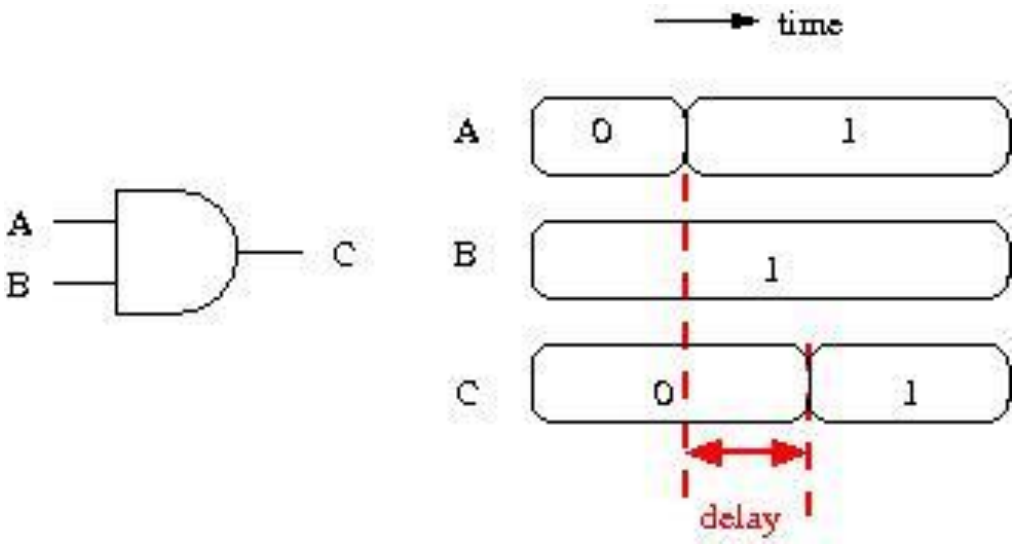
Problem Description

- find the maximum clock frequency (minimum clock period time) of the circuit

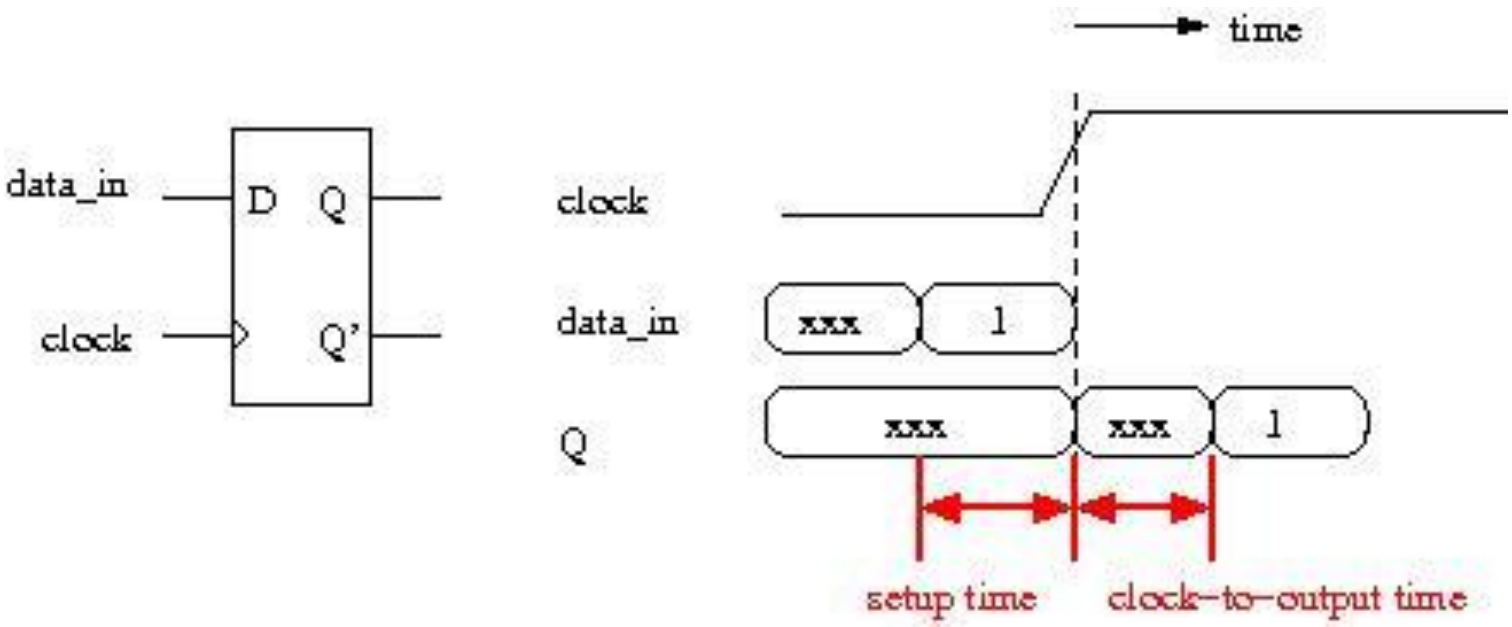


- delay of AND-gate: 3 ns
- delay of OR-gate: 4 ns
- setup time of D-FF: 2 ns
- clock-to-output time of D-FF: 1 ns

Delay of a gate



Delay for a flip-flop



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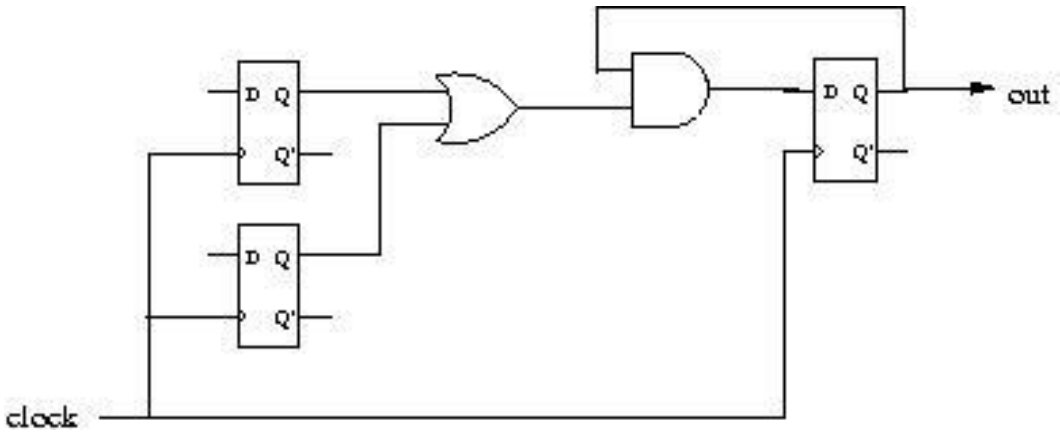

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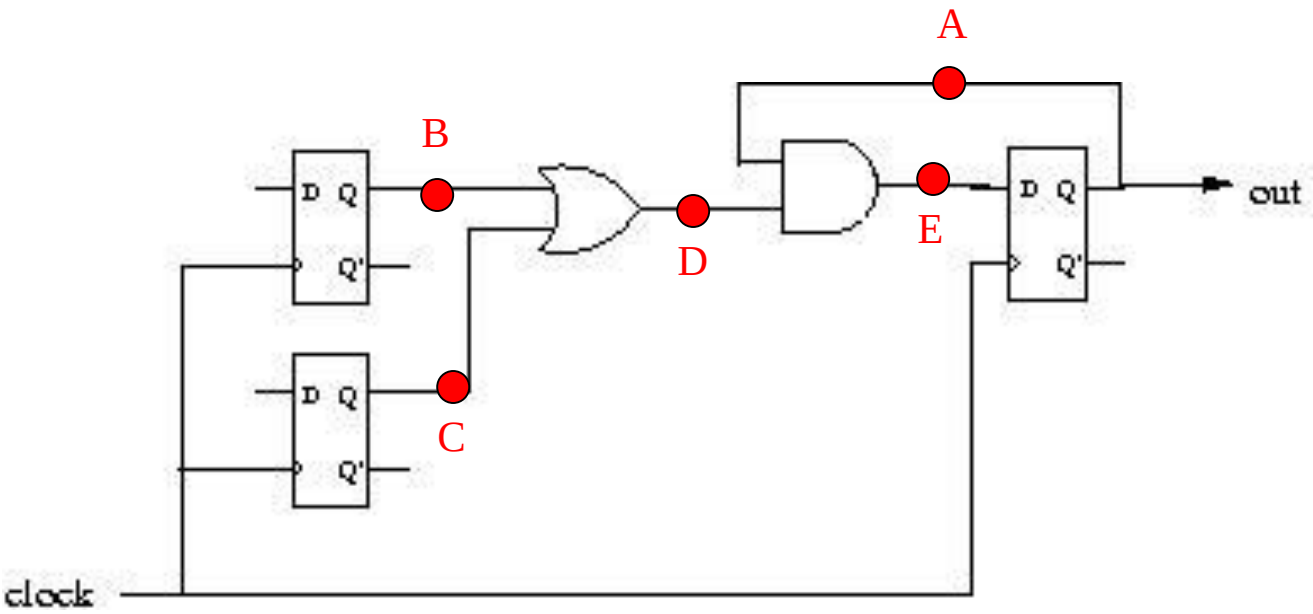
Analysis method

- start from the outputs of D-FFs
- mark critical points in the circuit
- find-out signal stable time for each point



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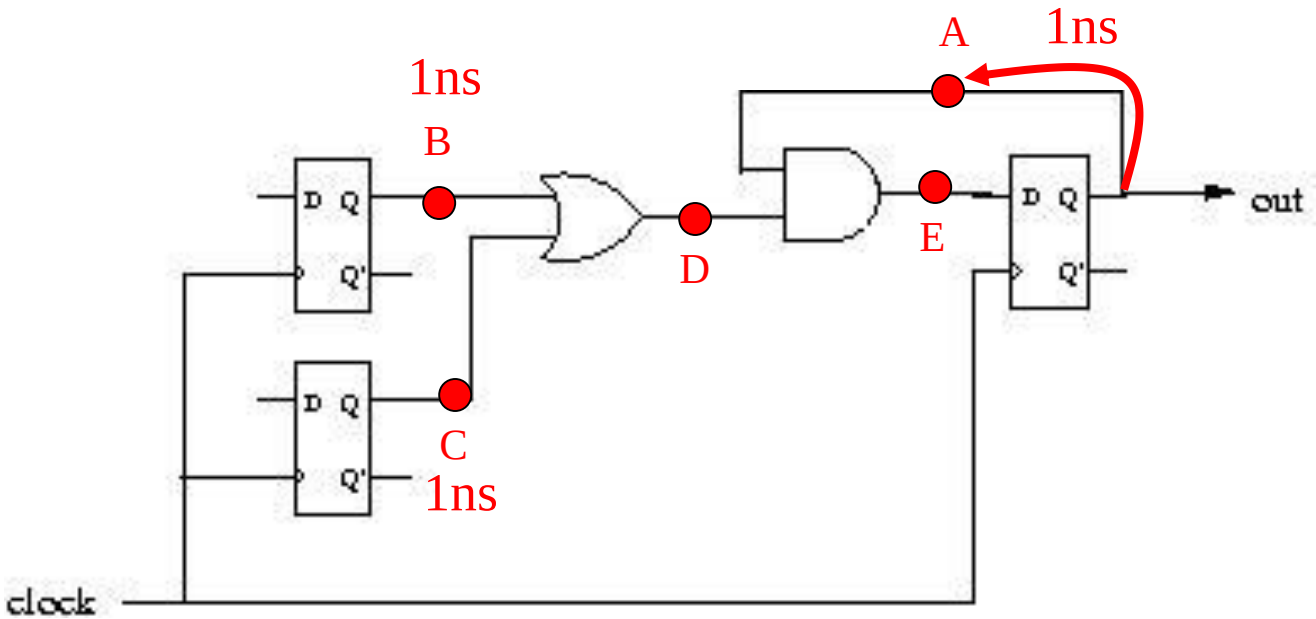

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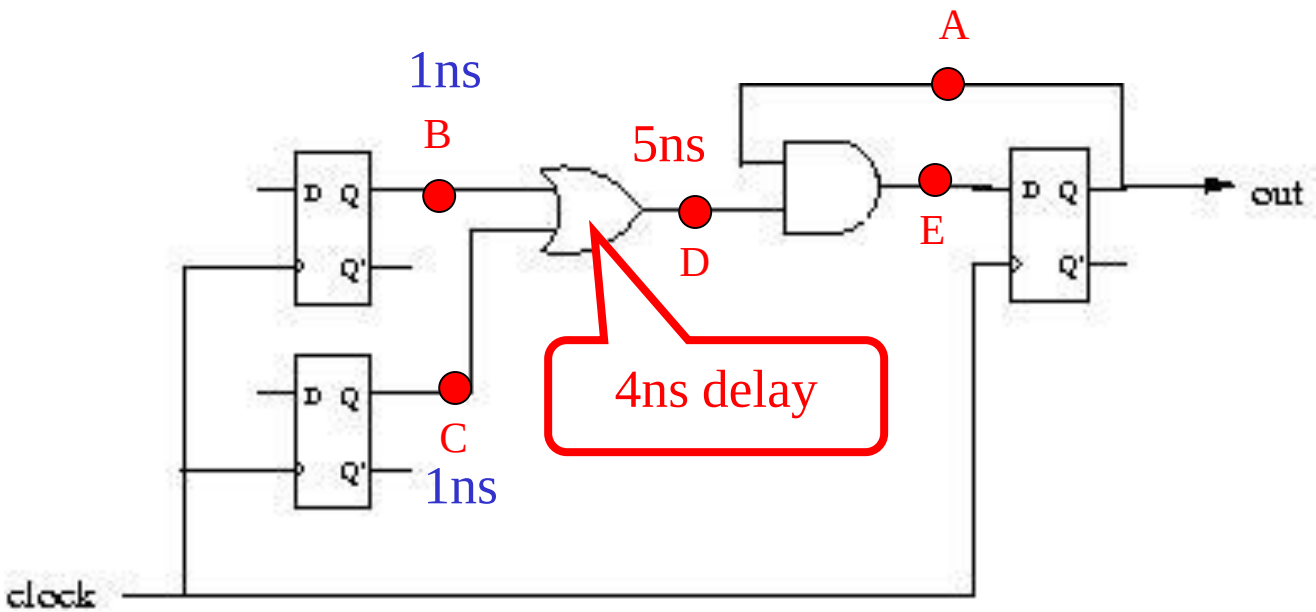

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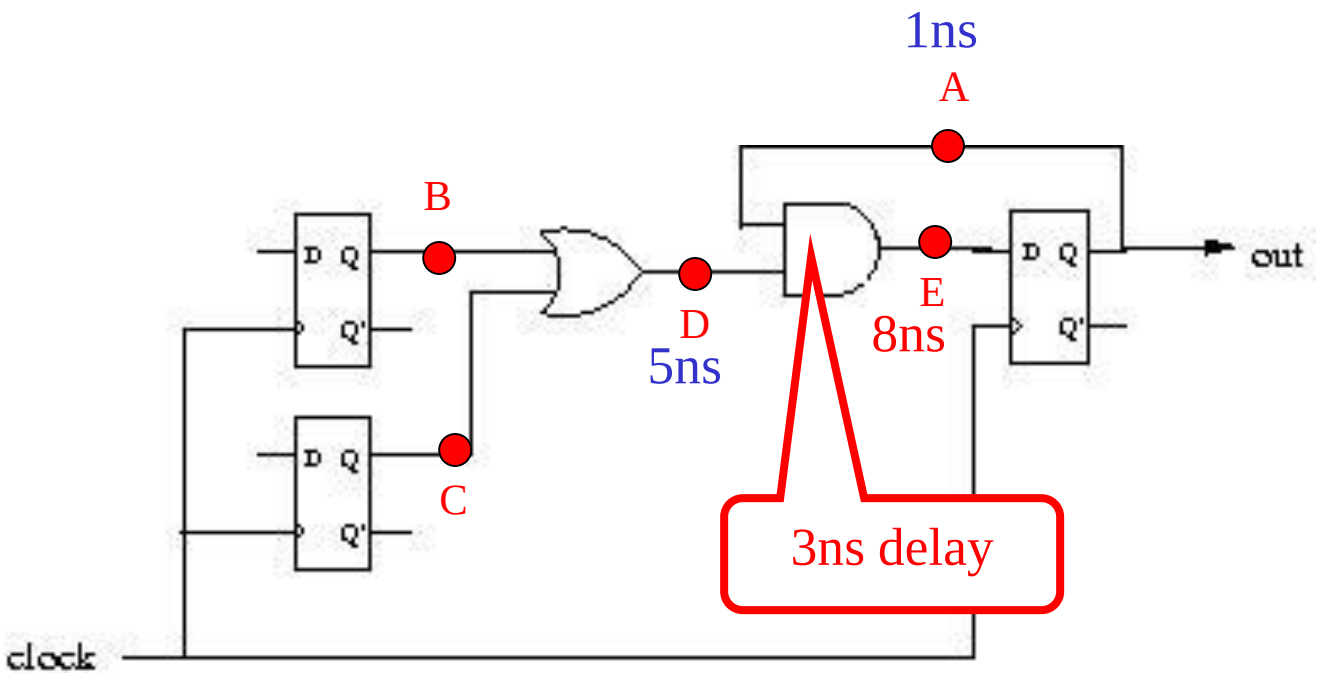

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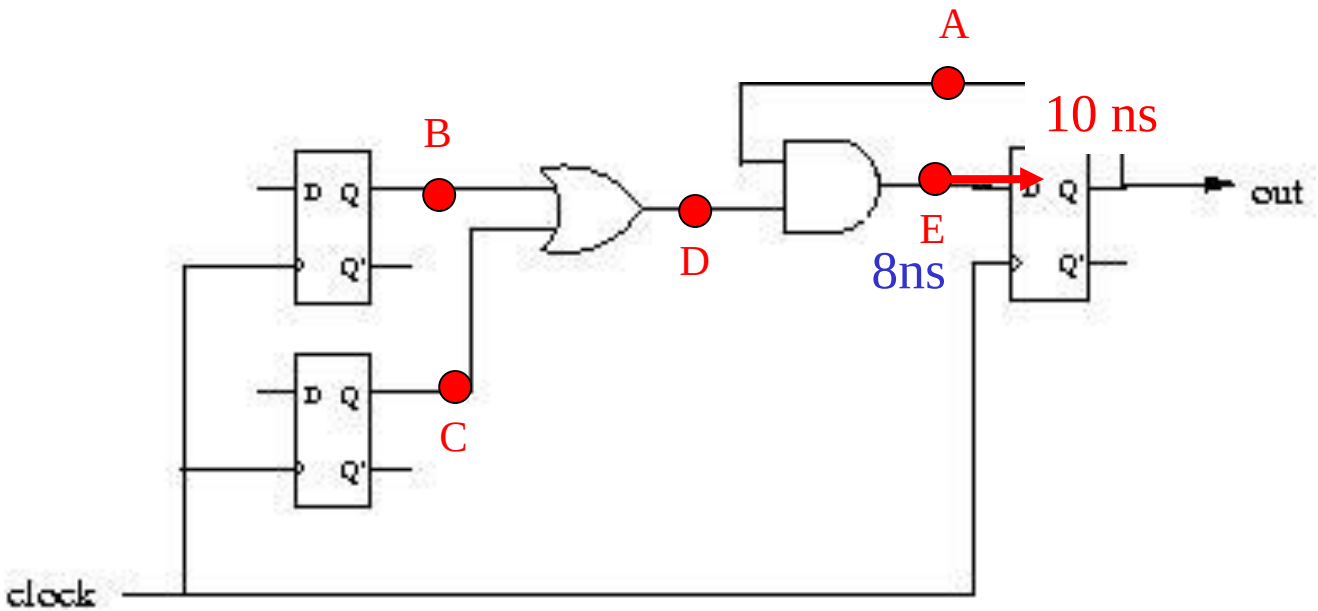
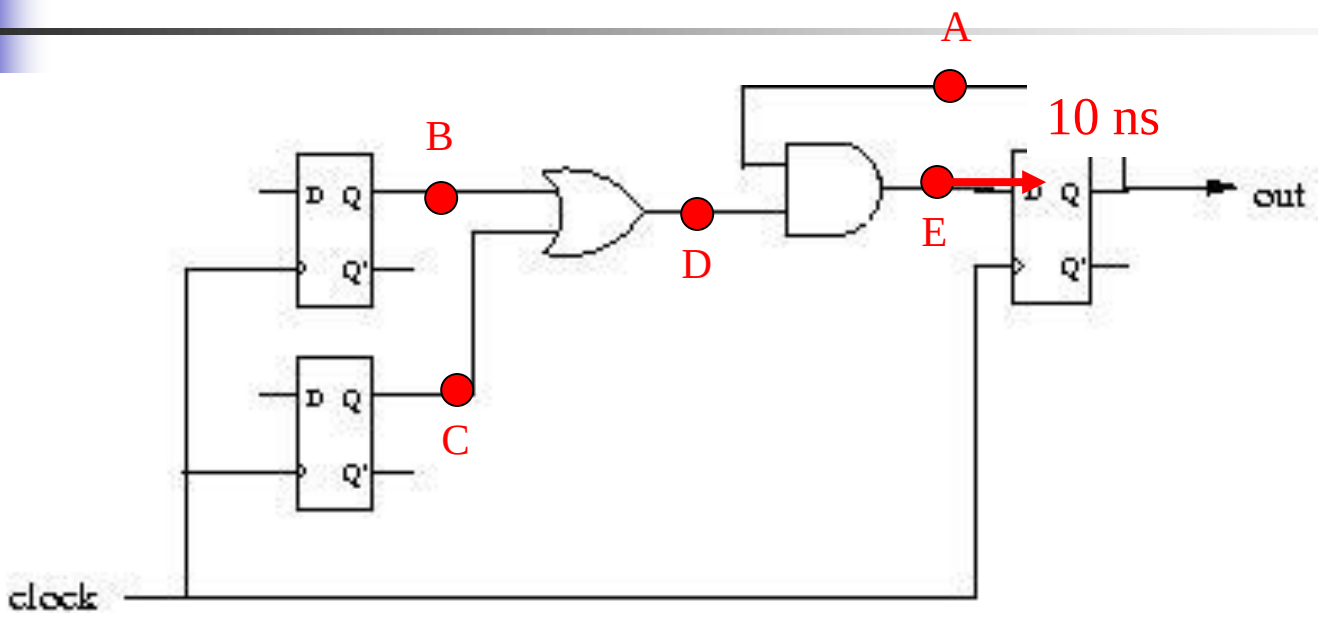
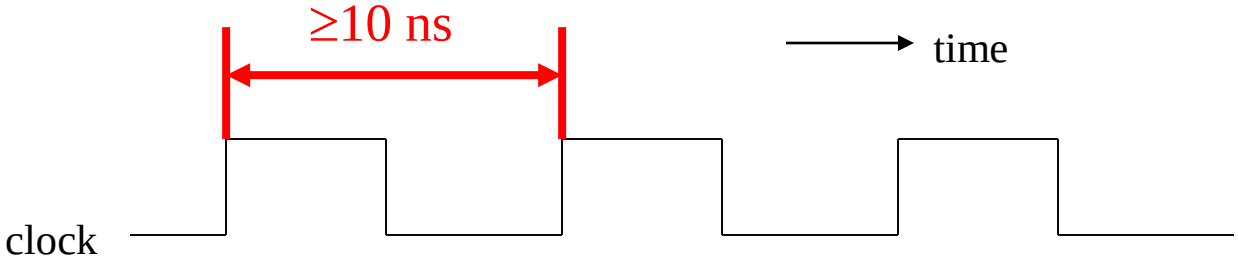
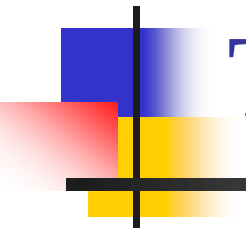


Clock period time and frequency



$$frequency \leq \frac{1}{10ns} = 100\text{MHz}$$

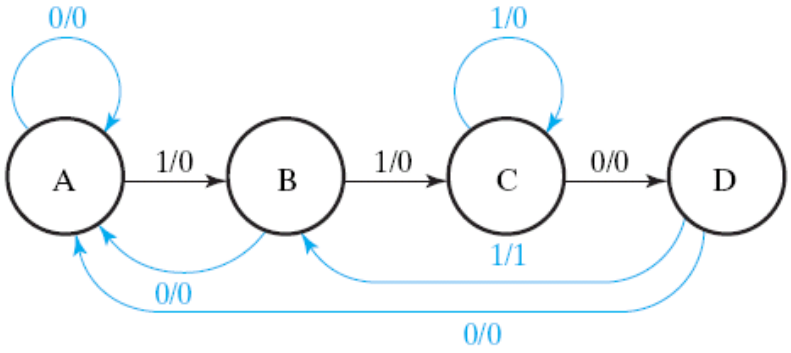


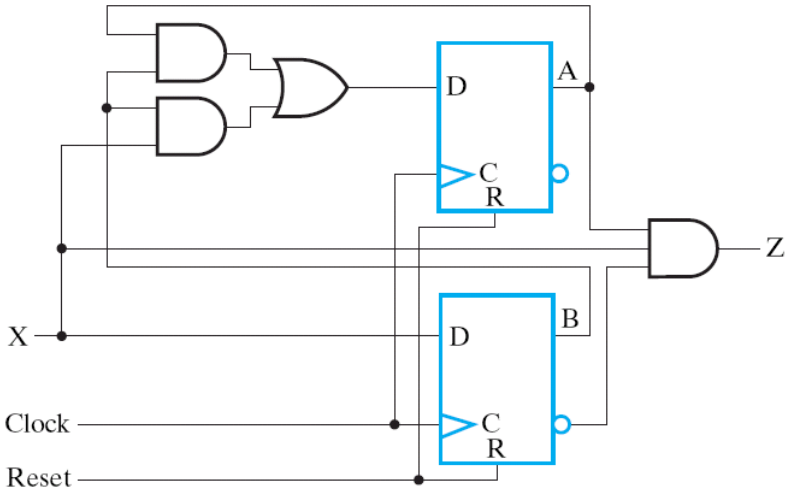


The next lecture

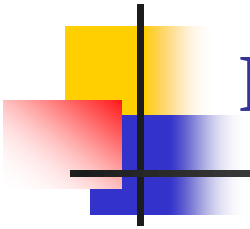
Next Lecture

- circuit design to realize a state-diagram
  - Section 5-5





Your work before the next meeting



- Preview the textbook: Section 5-5
- Review "digital circuit": combinational circuit design from the truth table
  - Chap. 2: Boolean algebra
  - Chap. 3: K-map simplification
- Review "discrete mathematics": finite automata
  - also named finite-state machine