**長庚大學 資訊工程系 計算機組織 期末考試題 2012/01/13**

1. 可翻閱參考書籍

(2) 考試時間：13:10 – 15:00

1. Design a hardware to compute



with only one *n*-bit adder. The inputs *A*, *B*, *C*, and output *X* are all *n*-bit unsigned integers. The spec is as follows (cf. Figure 1). The circuit starts computation upon receiving a one-cycle pulse “start=1”. The circuit generates the output X several cycles later and indicate by a one-cycle pulse “finish=1”. Your answer should include

1. Block diagram of the data path to perform the computation (with all data and control signals clearly named).
2. State-diagram of the control unit, with control signal values for each cycle clearly specified.



Figure 1

**(20%)**

1. Please translate the following assembly instructions of our simple processor to binary machine code.
2. ADD R6, R3, R1 //R6=R3+R1
3. LDI R4, 5 //R4= 5
4. ST R2, R3 //mem[R2]= R3
5. BRN R1, -5 //if (R1<0) goto PC-5

**(20%)**

1. For each of the instructions in Problem 2 (a)-(c), write down the control signal value (in the format of Figure 2) to show how these instructions are realized by the CPU data path (in Figure 3).

**(12%)**



Figure 2



Figure 3

1. Show how the branch instruction in Problem 2(d) is realized by the single-cycle CPU. Your answer should include
2. the control signal value in the format of Figure 2,
3. the circuit of the branch control unit to set PC (program counter) with each control signal clearly named, and
4. values of each control signal for each MUX selection in your answer (b).

**(8%)**

1. Disassemble each of the following binary machine code back to the assembly instruction.
2. 0000001 011 110 001
3. 0000101 101 101 010
4. 1000010 010 010 111
5. 1100000 111 010 101

**(20%)**

1. Use the data path of our single-cycle CPU to calculate amount of ones in a binary number. The design concept is shown in Figure 4. An additional control unit is added to realize the computation. At initial, the binary number to be calculated is stored in register R0 and R1 is 0. The calculation result will be stored in register R1. For example, the computation sets R1=3 if R0=(00100110)2. You may modify values of any registers as you wish. Your answer should include
2. the state-diagram of the control unit with operations of each state clearly specified,
3. the control signal value (in the format of Figure 2) for each state.

**(20%)**



Figure 4

1. You are asked to modify our single-cycle CPU with the inclusion of a new instruction MAX. The MAX instruction takes two register operands and stores the maximum value of the two operands in the destination register. For example, the instruction “MAX R3, R1, R2” means



Note that your modified design should also reserve all original instructions. Please show your design by writing down

1. the binary code format of the new instruction. (The format should be compatible to the original instruction set)
2. the modified CPU data path with each control signal clearly named, and
3. values of the control signal to perform “MAX R3, R1, R2”, in a modified format of Figure 2.

**(20%)**





