**長庚大學 資訊工程系 計算機組織 期末考試題 2013/01/11**

1. 可翻閱參考書籍

(2) 考試時間：13:10 – 15:00

1. Write an assembly program of our simple CPU to realize the following C program. (Assume that the size of an integer is 1 byte).

int i, A[10], B[10], S, N;

…

S = 0;

for (i=0;i<N;i++)

S = S + A[i] – B[i];

**(20%)**

1. Please translate the following assembly instructions of our simple processor to binary machine code.
2. SUB R2, R6, R5 //R2=R6-R5
3. ADI R4, R2, 5 //R4=R2+5
4. LD R2, R3 //R2=mem[R3]
5. BRZ R6, -9 //if (R6==0) goto PC-9

**(20%)**

1. For each of the instructions in Problem 2 (a)-(c), write down the control signal value (in the format of Figure 1) to show how these instructions are realized by the CPU data path (in Figure 2).

**(12%)**



Figure 1



Figure 2

1. Consider the assembly instruction “JMP R3”. Show how this instruction is realized by our single-cycle CPU by answering the following questions:
2. How the branch destination address is brought to the branch control unit?
3. The control signal value in the format of Figure 1,
4. The circuit of the branch control unit to set PC (program counter) with each control signal clearly named, and
5. Values of each control signal for each MUX selection in your answer (c).

**(8%)**

1. Disassemble each of the following binary machine code back to the assembly instruction.
2. 0000101 010 111 011
3. 1000010 101 101 010
4. 0001010 000 110 101
5. 1100001 110 011 101

**(20%)**

1. Use the data path of the single-cycle CPU to perform saturated addition of two unsigned integers. The semantics is as follows:



The design concept is shown in Figure 4. You are asked to design additional control unit to command the data path to realize the required computation. You may use any input port of the data path to send constants. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 1) for each state.

**(20%)**



Figure 4

1. You are asked to modify the single-cycle CPU to include a new instruction JAL (Jump and Link) for function calls. The JAL instruction serves as the call to a subroutine: jump to the beginning of a subroutine and store the return address (PC+1) in a register. The instruction has two register operands:

* The first operand specifies the register to store the return address,
* The second operand specifies the destination address to jump to (like the JMP instruction we already have).

For example, the instruction “JAL R1, R2” has the following semantics:

R1 = PC+1 //store the return address at R1

PC = R2 //goto the address stored in R2

Write down your design of the modified CPU. Your answer should address the following issues:

(a) The binary code format of the new instruction

(b) The modified data path of the CPU

(c) The modified control signals

(d) Value of the control signals to realize “JAL R1, R2”

**(25%)**





