**長庚大學 資訊工程系 計算機組織 期末考試題 2014/01/17**

1. 可翻閱參考書籍

(2) 考試時間：13:10 – 15:00

1. **(10 pts)** Draw the circuit synthesized from the following Verilog code.

**module** block\_p1 (a, b, c, d, e, clock);

**input** a, b, c;

**output** d, e;

**input** clock;

**reg** d, e;

**always** @(posedge clock) **begin**

d = a&b;

**end**

**always** @(a or b or c) **begin**

e = a|b|c;

**end**

**endmodule**

2. **(15 pts)** Write a Verilog code to synthesize a circuit that realizes the state-transition diagram in Figure 1. You may assign the value for each state (S0, S1, S2) as you want.



**Figure 1.**

3. **(15 pts)** Design a data path circuit to realize the following micro-operations.



The data path has three registers *R*0, *R*1, and *R*2. Register transfers are controlled by three input signals *CA*, *CB*, and *CC*. Contents of all registers remain un-changed if *CA*=*CB*=*CC*=0. Please draw the block diagram of this data path.

4. **(15 pts)** Write the Verilog code to synthesize the circuit in Problem 3.

5. **(20 pts)** Design a circuit to perform the arithmetic operation Q=A-B+C-D. Figure 2 shows the signal interface. The hardware has 4 *n*-bit inputs {A, B, C, D} and a control signal named start. After receiving one-cycle start signal, the circuit performs the required operation and generates the result Q several cycles later. You can use only one *n*-bit adder in your design. Your answer should include

(a) Block diagram of the data path, and

(b) The state-transition diagram of the control unit



**Figure 2.**

6. **(15 pts)** For each of the instructions listed below, write down the control signal value (in the format of Figure 3) to show how these instructions are realized by the CPU data path (in Figure 4).

(a) ADD R1, R2, R3 //R1=R2+R3

(b) ADI R1, R2, 3 //R1=R2+3

(c) ST R2, R1 //mem[R2]=R1



Figure 3



Figure 4

7. **(20 pts)** Use the data path of the single-cycle CPU to perform saturated addition of two unsigned integers. The semantics is as follows:



The design concept is shown in Figure 5. You are asked to design additional control unit to command the data path to realize the required computation. You may use any input port of the data path to send constants. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 3) for each state.



**Figure 5**

8. **(20 pts)** Consider the addition of two n-bit signed numbers encoded with 2’s complement. Figure 6 shows the circuit to generate the overflow flag *V*, where *Ci* stands for the carry sent from the full-adder at bit *i*-1 to bit *i*. Prove that the overflow occurs if and only if .



**Figure 6**





