**長庚大學 資訊工程系 計算機組織 期末考試題 2015/01/16**

1. 可翻閱參考書籍

(2) 考試時間：13:10 – 15:00

1. **(15 pts)** Draw the circuit synthesized from the following Verilog code.

**module** block\_p1 (a, b, c, d, e, clock);

**input** a, b, c;

**output** d, e;

**input** clock;

**reg** d, e;

**always** @(posedge clock) **begin**

d <= (e)? ~d: d;

**end**

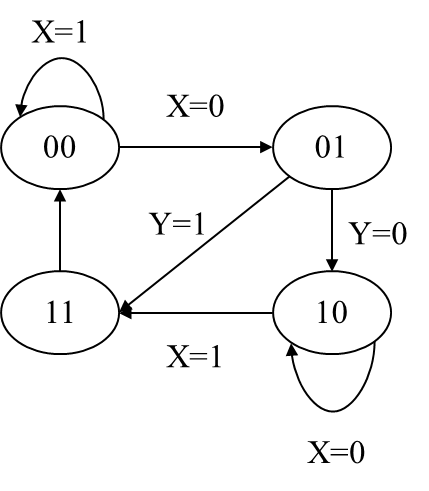
**always** @(a or b or c) **begin**

e = (a)? b: c;

**end**

**endmodule**

2. **(15 pts)** Write a Verilog code to synthesize a circuit that realizes the state-transition diagram in Figure 1. The circuit has two flip-flops to establish four states and state transitions are based on two input signals *X* and *Y*. Note that the state “11” transits to state “00” at the next cycle despite of input values on *X* and *Y*.



**Figure 1.**

3. You are asked to realize the data path circuit to of the following micro-operations.



The data path has three 32-bit registers *R*0, *R*1, and *R*2. Register transfers are controlled by three input signals *CA*, *CB*, and *CC*. At any time, at most one of *CA*, *CB*, and *CC* will be of value 1. Contents of all registers remain un-changed if *CA*=*CB*=*CC*=0. Your answer should include:

1. **(15 pts)** The block diagram of the circuit that realizes the micro-operations, and
2. **(15 pts)** The verilog code to synthesize the desired circuit.

4. **(25 pts)** For each of the instructions listed below, write down the control signal value (in the format of Figure 2) to show how these instructions are realized by the CPU data path (in Figure 3).

(a) SUB R5, R2, R4 //R5=R2-R4

(b) ADI R1, R2, 3 //R1=R2+3

(c) LD R6, R3 //R6=mem[R3]

(d) BRN R0, -5 //if (R0<0) goto current\_position-5

(e) JMP R2 //goto position@R2



Figure 2



Figure 3

5. **(20 pts)** Use the data path of the single-cycle CPU to perform addition with all operands in the memory. The semantics is as follows:



You can destroy the values stored in registers R4 to R7. The design concept is shown in Figure 4. You are asked to design additional control unit to command the data path to realize the required computation. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 2) for each state.



**Figure 4**

6. **(20 pts)** Consider the addition of two n-bit signed numbers encoded with 2’s complement. Figure 5 shows the circuit to generate the overflow flag *V*, where *Ci* stands for the carry sent from the full-adder at bit *i*-1 to bit *i*. Prove that the overflow occurs if and only if .



**Figure 5**

