**長庚大學 資訊工程系 計算機組織 期末考試題 2011/01/10**

1. 可翻閱參考書籍

(2) 考試時間：15:10 – 17:00

1. Design a hardware to compute



with only one *n*-bit adder. The inputs *A*, *B*, *C*, and output *X* are all *n*-bit unsigned integers. The spec is as follows (cf. Figure 1). The circuit starts computation upon receiving a one-cycle pulse “start=1”. The circuit generates the output X several cycles later and indicate by a one-cycle pulse “finish=1”. Your answer should include

1. Block diagram of the data path to perform the computation (with all data and control signals clearly named).
2. State-diagram of the control unit, with control signal values for each cycle clearly specified.



Figure 1

**(20%)**

1. Please translate the following assembly instructions of our simple processor to binary machine code.
2. SUB R3, R5, R2 //R3=R5-R2
3. ADI R4, R1, 5 //R4=R1+5
4. LD R2, R3 //R2=mem[R3]
5. BRZ R1, -11 //if (R1==0) goto PC-11

**(20%)**

1. For each of the instructions in Problem 2 (a)-(c), write down the control signal value (in the format of Figure 2) to show how these instructions are realized by the CPU data path (in Figure 3).

**(12%)**



Figure 2



Figure 3

1. Show how the branch instruction in Problem 2(d) is realized by the single-cycle CPU. Your answer should include
2. the control signal value in the format of Figure 2,
3. the circuit of the branch control unit to set PC (program counter) with each control signal clearly named, and
4. values of each control signal for each MUX selection in your answer (b).

**(8%)**

1. Disassemble each of the following binary machine code back to the assembly instruction.
2. 0000000 001 010 101
3. 0000101 100 101 000
4. 1000010 000 011 101
5. 1100001 111 110 101

**(20%)**

1. Design the control unit to perform the following computation with the data path of our single-cycle CPU.



The design concept is shown in Figure 4. Suppose:

1. The array size *n* is initially store in R1 and R1 will be set to zero after the computation finished.
2. The starting addresses of array *A* and *B* are initially stored in R1 and R2, respectively.

You may modify values of any registers as you wish. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 2) for each state.

**(20%)**



Figure 4

1. You are asked to modify our single-cycle CPU with the inclusion of a new instruction ABS. The ABS instruction takes one source register operand and store the absolute value of the source register in the destination register. For example, the instruction “ABS R1, R2” means “R1=|R2|”. Note that your modified design should also reserve all original instructions. Please show your design by writing down
2. the binary code format of the new instruction. (The format should be compatible to the original instruction set)
3. the modified CPU data path with each control signal clearly named, and
4. values of the control signal to perform R1=|R2|, in a modified format of Figure 2.

**(20%)**





