**長庚大學 資訊工程系 計算機組織 期中考試題 2012/11/16**

(1) 可翻閱參考書藉

(2) 考試時間：1:10PM – 3:00PM

1. **(15 pts)** Consider the circuit in Figure 1(a). Besides the clock signal, the circuit has two input signals *A*, *B* and two D flip-flops *D*1 and *D*0. Please complete the waveform in Figure 1(b) by filling states of *D*1 and *D*0 for each cycle.



1. the circuit (b) waveform to be completed

**Figure 1.**

1. **(15 pts)** Consider the state-transition diagram in Figure 2. The state diagram has four states triggered by two input signals *X* and *Y*. Please design a digital circuit to realize the state-transition diagram.



**Figure 2.**

1. **(15 pts)** You are asked to design a 4-bit **up/down counter** with parallel load. Figure 3 shows the specification. Please design the circuit with basic logical cells such as AND/OR/NOT/XOR/multiplexer/D flip-flops.



1. Input/output interface (b) Function specification

**Figure 3.**

1. Design a 4-digit timer specified in Figure 4. The timer refreshes every 0.01 seconds and counting starts from 00.00 second to 99.99 second. Please show the following components of the timer.
2. **(5 pts)** The circuit to generate 1-cycle pulse for every 0.01 seconds from the **10 KHz clock**.
3. **(5 pts)** The circuit of the data path for the 4-digit time counting from 00.00 second to 99.99 seconds.
4. **(5 pts)** The state-transition diagram of the control unit to send control signals to the 4-digit counting data path
5. **(5 pts)** The control circuit to show the counting time on the four 7-segment display.



**Figure 4.**

1. **(15 pts)** Design a data path circuit to realize the following micro-operations.



The data path has three registers *R*0, *R*1, and *R*2. Register transfers are controlled by three input signals *CA*, *CB*, and *CC*. Contents of all registers remain un-changed if *CA*=*CB*=*CC*=0. Please draw the block diagram of this data path.

1. **(20 pts)** Design the circuit for the equation evaluation:



The input/output interface is shown in Figure 5. Assume that the 4 input data--- A, B, C, D ---- are kept fixed during the computation. You can use **only one adder** and no comparator can be used in your design. Please show

1. the state diagram of the control unit, and
2. the circuit diagram of the data path.



**Figure 5**

1. **(20 pts)** You are asked to design the normalization circuit in a floating-point unit. Figure 6 shows the signal interface. The circuit receives an n-bit **signed** integer *A* and counts amount of leading sign bits in *A* as the output *X*. That is, *X* will be the number of leading 0’s if *A* is positive. On the other hand, the number of leading 1’s in *A* will appear on *X* if *A* is a negative integer. An example is as follows.



Please show the following parts in your design:

1. the state-transition diagram of the control unit of your design
2. the block diagram of the data path of your design.



**Figure 6**