**長庚大學資訊工程系 計算機組織隨堂練習 2014/09/26**

考試範圍：數位電路課程全部

考試時間：1:10 PM– 2:00PM

考試規則：可翻閱參考資料, 1:50PM 後開放討論

1. Draw the timing waveform for a given circuit. The circuit is shown in Figure 1. Please complete the waveform in Figure 2. (50%)



Figure 1



Figure 2

1. Design a frequency divider as specified in Figure 3. The circuit receives 100 MHz clock input ICLK and generates a clock signal OCLK with lower frequency. The frequency of OCLK is controlled by the 2-bit input signal *S*, as specified in the table in Figure 3. Your design has to be a **synchronous** circuit. Draw the circuit diagram of your design. (50%)

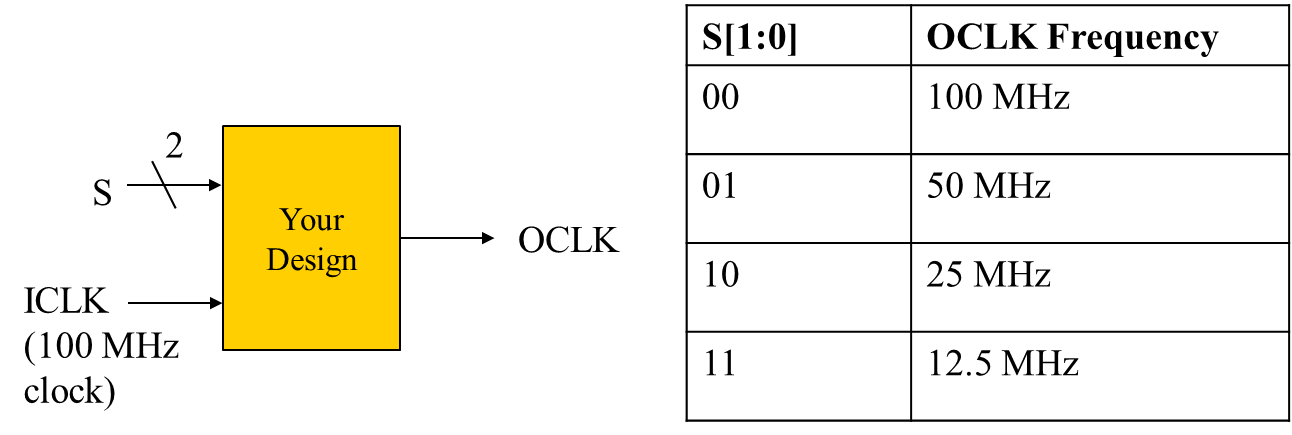


Figure 3.