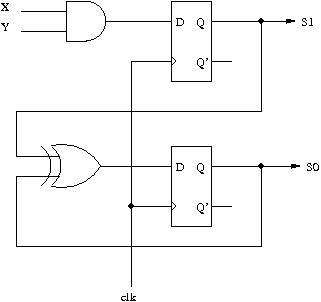
**長庚大學 資訊工程系 計算機組織 期中考試題 2011/11/18**

(1) 可翻閱參考書藉

(2) 考試時間：1:10PM – 3:00PM

1. **(15 pts)** Consider the circuit in Figure 1(a). Besides the clock signal clk, the circuit has two input signals X, Y and two D flip-flops S1 and S0. Please complete the waveform in Figure 1(b) by filling states of S1 and S0 for each cycle.

1. Circuit (b) Timing waveform

**Figure 1.**

1. **(15 pts)** Consider the state diagram in Figure 2. The state diagram has three states triggered by one input signal X. Please design a digital circuit to realize the state diagram.



**Figure 2.**

1. **(15 pts)** You are asked to design a 4-bit **down counter** with parallel load. Figure 3 shows the specification. The input/output interface is shown in Figure 3(a). The counting function, controlled by signals Count and Load, is specified in Figure 3(b). Please design the circuit with AND/OR/NOT gates and multiplexers.



1. Input/output interface (b) Function specification

**Figure 3.**

1. You are asked to design a 4-digit timer specified in Figure 4. The timer receives an 1 KHz clock signal and displays 4 decimal digits. The timer refreshes every 0.01 seconds and counting starts from 00.00 second to 99.99 second. Please show the following components of the timer.
2. **(6 pts)** The circuit to generate 1-cycle pulse for every 0.01 seconds from the 1 KHz clock.
3. **(9 pts)** The circuit for the 4-digit time counting from 00.00 second to 99.99 seconds.



**Figure 4.**

1. **(20 pts)** You are asked to design the circuit for an arithmetic computation. The input/output interface is shown in Figure 5. Assume that the 4 input data--- A, B, C, D ---- are kept fixed during the computation. You can use **only one adder** for the computation. The arithmetic operation to be realized is

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Your answer should include

1. the state diagram of the control unit, and
2. the circuit diagram of the data path.
3. **(20 pts)** Realize a series of computation with minimum amount of registers. The computation is as follows.

T1 = A+B

T2 = A-B

T3 = T1+T2

T4 = C-T3

T5 = D-A

T6 = T4-T5

A, B, C, D are input data kept fixed during the computation. Temporary variables T1-T6 are to be stored in registers and T6 is the final output. You can use **only one adder** to realize the computation. Please draw the data path that stores T1-T6 in **minimum amount of registers**. You should explain how you devise the circuit.

1. **(25 pts)** Design the circuit to find **greatest common divisor** (GCD) of two positive integers A and B. You can use only one adder. You answer should include
2. the state diagram of the control unit with control signals annotated, and
3. the circuit diagram of the data path.