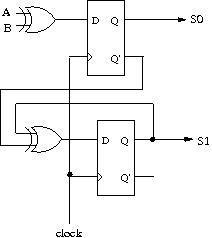
**長庚大學 資訊工程系 計算機組織 期中考試題 2013/11/15**

(1) 可翻閱參考書藉

(2) 考試時間：1:10PM – 3:00PM

1. **(10 pts)** Draw the state-transition diagram to explain the behavior of the circuit in Figure 1.



**Figure 1.**

1. **(15 pts)** Design a circuit with the behavior specified in the state-transition diagram shown in Figure 2. The circuit has three states and one input signal *X*.



**Figure 2.**

1. **(20 pts)** You are asked to design a circuit for counting votes in a Yes/No polling. The spec is shown in Figure 3. There are at most four people in a poll and each one hits a button in his seat to express “Yes” for the poll. Hitting a button twice or more won’t change the answer and one does not have to hold the button until the polling outcome appears. Each button is routed to a button control unit and a 1-cycle pulse is sent whenever the button is hit once. Your task is to design the circuit that counts amount of buttons hit and send out the result with a 3-bit bus named “count”.



**Figure 3.**

1. **(15 pts)** You are asked to analyze the performance of the circuit in Figure 4. Suppose:

(1) the delay of an AND gate is 3 ns.

(2) the delay of an OR gate is 4 ns.

(3) the setup time and clock-to-output time of a D flip-flop is 2 ns and 1 ns, respectively.

What is the maximum clock frequency that the circuit can work correctly?

sample_circuit

**Figure 4.**

1. **(15 pts)** You are asked to design a 4-bit **up/down counter** with parallel load. Figure 5 shows the specification. Please design the circuit with basic logical cells such as AND/OR/NOT/XOR/multiplexer/D flip-flops.



1. Input/output interface (b) Function specification

**Figure 5.**

1. **(20 pts)** Design a 4-digit count-down timer specified as follows. The timer refreshes every one second and counts down from 59:59 to 00:00. The count-down is driven by a clock signal with 1KHz frequency. Please show that how a set of counters can be connected to realize the count-down timer.
2. **(20 pts)** You are asked to design a frequency divider in responsible of generating a slower clock from a faster clock signal. The specification is shown in Figure 6. The frequency divider receives an input clock ICLK with 1GHz frequency and generates an output clock OCLK in 100MHz. Moreover, the generated clock has 30% duty-cycle: each cycle period has 3 ns in logic 1 and 7ns in logic 0. Please design the circuit of the frequency divider.



**Figure 6.**