長庚大學 資訊工程系碩士班 專業能力鑑定 計算機架構試題 2012/08/22

說明:

1. 可翻閱參考書籍
2. 滿分 120 分
3. Translate the following C program to MIPS or ARM assembly code. **(20 pts)**

int S, A[100], B[100];

S = 0;

i = 0;

j = 99;

while (i<100)

S = S + A[i++] \* B[j--];

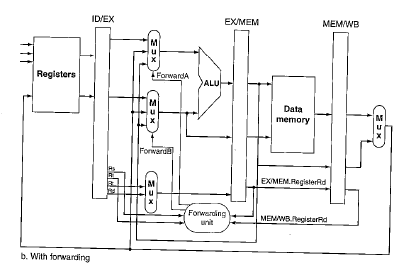
1. As an engineer, you are asked to write a program in some simple embedded processor that has no hardware multipliers and dividers. Moreover, you are facing stringent performance requirement to develop the software. Write a C program to compute

*A* = 3868\**B*,

where *A* and *B* are of integer type. Note that you can use only add, subtract, and shift operations in your program. No multiplications and divisions are allowed. Try to minimize amount of additions and subtractions for the computation. You will get all the score if you realize the computation with no more than four additions and subtractions. (You will get 10 pts if your answer is correct but not optimal.) **(15 pts)**

(Hints: (1) the binary representation of 3868 is 00111100011100, (2) think about the mathematical principle behind Booth encoding.)

1. Give an example to explain each of the following pipeline hazards. Your answer should include (i) a simple MIPS/ARM assembly program, and (ii) a figure of pipeline behavior to indicate where the stall is.
2. Data hazard **(10 pts)**
3. Control hazard **(10 pts)**
4. Consider the MIPS pipeline data path in Figure 1. Draw a hardware block diagram to show how the forwarding unit is implemented. That is, draw a **digital circuit diagram** to show how the two MUX selection signals *ForwardA* and *ForwardB* are generated. You can use any components (such as multiplexer, adder, comparator, counter, etc.) you learned in the digital circuit course. **(15 pts)**



**Figure 1**

1. Consider a 32Kbyte 4-way set associative cache. Each cache block is of 16 bytes. Write down the 32-bit address format, as in Figure 2, to access the cache. **(10 pts)**



**Figure 2**

1. You are asked to modify the MIPS processor pipeline (with forwarding) to include a new instruction, ADDM. The ADDM instruction performs addition on two operands and store the result in some destination register. The modification is that the second operand of ADDM is a memory operand with the address indicated by the register operand. For example, the instruction

addm $1, $2, $3

indicates the following computation:

R1 = R2 + mem[R3].

Answer the following questions about the modified processor.

1. Draw the modified data path of the MIPS processor pipeline. You should show clearly (i) the modified pipeline stages, and (ii) the additional forwarding path to send the result of an ADDM instruction to some depending instruction. **(20 pts)**
2. Draw the digital circuit diagram of the forwarding unit to show how to control the additional forwarding path. **(20 pts)**