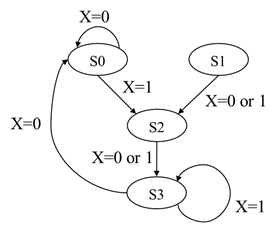
**長庚大學 資訊工程系 計算機組織 期末考試題 2016/01/15**

1. 可翻閱參考書籍

(2) 考試時間：13:10 – 15:00

1. **(15 pts)** Write a Verilog code to synthesize a circuit that realizes the state-transition diagram in Figure 1. The circuit has two flip-flops to establish four states and state transitions are based on the input signal *X*.



**Figure 1.**

2. You are asked to realize the data path circuit to of the following micro-operations.



The data path has three 32-bit registers *R*0, *R*1, and *R*2. Register transfers are controlled by three input signals *CA*, *CB*, and *CC*. At any time, at most one of *CA*, *CB*, and *CC* will be of value 1. Contents of all registers remain un-changed if *CA*=*CB*=*CC*=0. Your answer should include:

1. **(10 pts)** The block diagram of the circuit that realizes the micro-operations, and
2. **(10 pts)** The verilog code to synthesize the desired circuit.

3. **(20 pts)** You are asked to implement a frequency dividor using Verilog. The frequency dividor receive a clock signal with 1 KHz frequency and generates an output clock in 100 Hz with 50% duty cycle. Write a synthesizable Verilog code to realize the frequency dividor. Note that no adders and comparators are allowed in the synthesized circuit.

4. **(25 pts)** For each of the instructions listed below, write down the control signal value (in the format of Figure 2) to show how these instructions are realized by the CPU data path (in Figure 3).

(a) ADD R2, R4, R6 //R2=R4+R6

(b) INC R1 //R1=R1+1

(c) ST R6, R3 //mem[R6]=R3

(d) BRZ R0, -5 //if (R0=0) goto current\_position-5

(e) JMP R4 //goto position@R4



Figure 2



Figure 3

5. **(30 pts)** Use the data path of the single-cycle CPU to compute the sum of an array:

.

At initial, the array *A* is stored in the data memory, with the starting address stored in register *R*1 and the array size *N* stored in *R*2. After the computation, the result has to be stored in R0 and you can destroy values stored in other registers. The design concept is shown in Figure 4. You are asked to design additional control unit to command the data path to realize the required computation. Your answer should include

1. the state-diagram of the control unit with operations of each state clearly specified,
2. the control signal value (in the format of Figure 2) for each state.
3. the Verilog code that synthesizes the circuit of the control unit.



**Figure 4**

