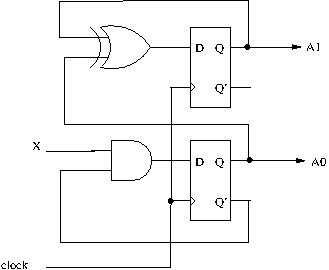
**長庚大學 資訊工程系 計算機組織 期中考試題 2015/11/20**

(1) 可翻閱參考書藉

(2) 考試時間：1:10PM – 3:00PM

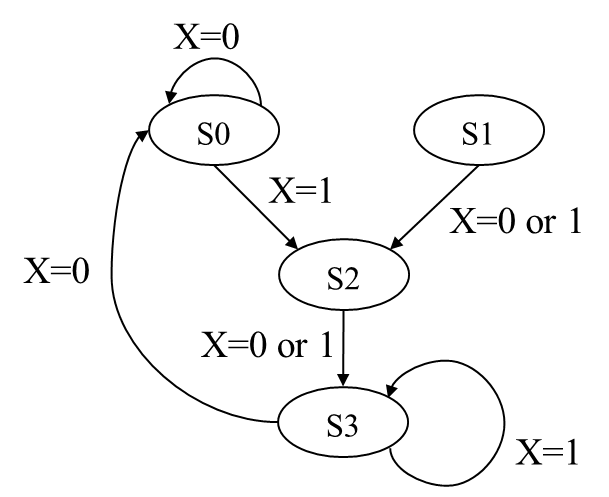
**General answering rules:**

1. You can use any components (such as AND-gate, adder, comparator, mod-N counter, etc.) that ever mentioned in this course and the digital circuit course without showing the detailed design of these components.
2. For a combinational circuit part in your design, you just have to specify the Boolean equation or the truth table of this part. You don’t need to draw the gate-level circuit diagram for a combinational circuit.
3. **(15 pts)** Draw the state-transition diagram to explain the behavior of the circuit in Figure 1.



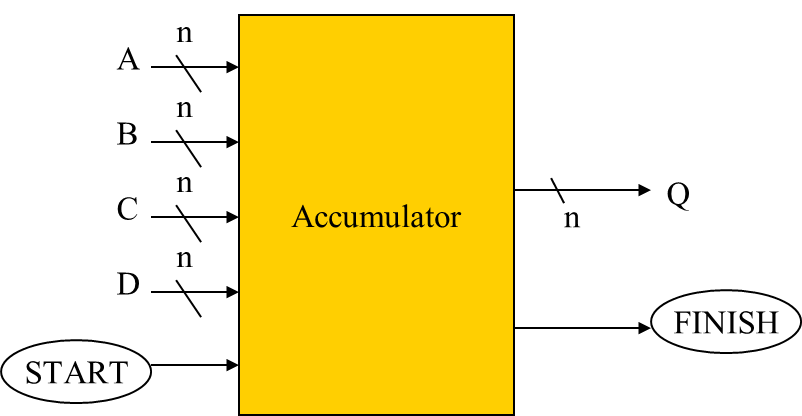
**Figure 1.**

1. **(15 pts)** Design a circuit with the behavior specified in the state-transition diagram shown in Figure 2. The circuit has four states and one input signal *X*.



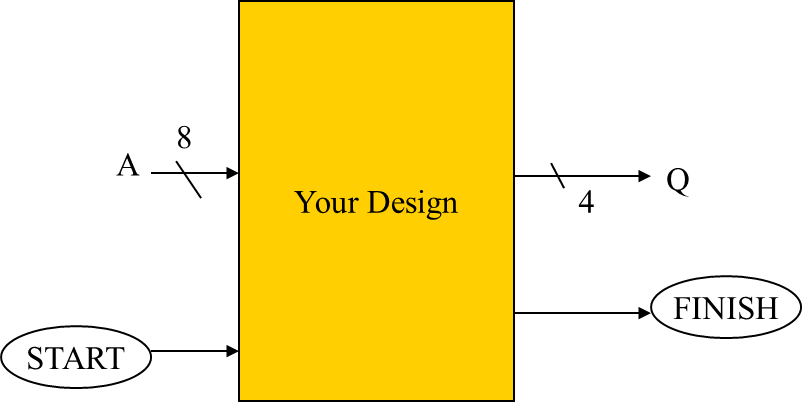
**Figure 2.**

1. **(20 pts)** Design a circuit to compute Q=(A+B)/2 + (C+D)/4. The signal interface is shown in Figure 3. The circuit receives a START signal with one cycle logic-1 pulse to start the computing. Each of the four inputs {*A*, *B*, *C*, *D*} is a *n*-bit unsigned integer number. To limit the chip area, you can use only one *n*-bit adder in the circuit. You may assume that all the four input numbers are fixed during computation and no overflow will occur in the computation. Draw the circuit diagram to show your design.



**Figure 3.**

1. **(20 pts)** Design the circuit to count amount of 1s in a given number. The signal interface is shown in Figure 4. The input *A* is an 8-bit number. After the input *A* is set, an one-cycle pulse “START” triggers the calculation. The output, amount of 1s in *A*, will be presented on *Q* and indicated by an one-cycle pulse “FINISH”. For example, if the input *A*=010011012, the circuit will generate an output *Q*=01002 when the computation is completed. Draw the circuit diagram of your design and explain how you devise the design.



**Figure 4.**

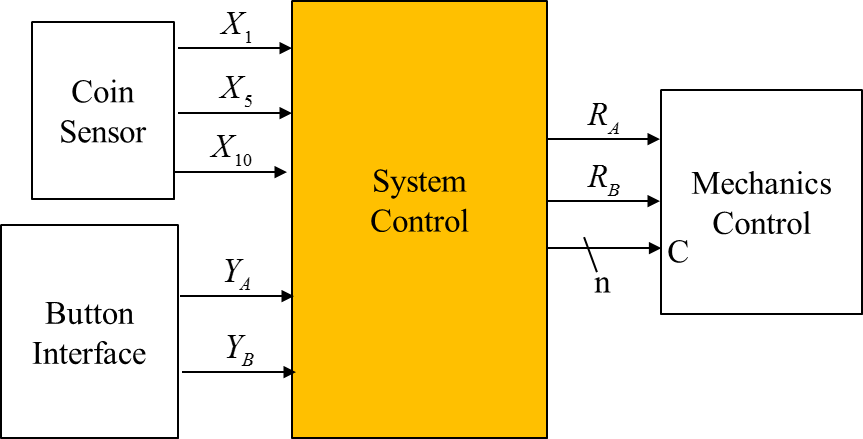
1. You are asked to design a 4-digit timer specified in Figure 4. The timer receives an 1 KHz clock signal and displays 4 decimal digits. The timer refreshes every 0.01 seconds and counting starts from 00.00 second to 99.99 second. Please show the following components of the timer.
2. **(8 pts)** The circuit to generate 1-cycle pulse for every 0.01 seconds from the 1 KHz clock.
3. **(12 pts)** The circuit for the 4-digit time counting from 00.00 second to 99.99 seconds.



**Figure 5.**

1. **(30 pts)** After graduation, you got an engineering position in a team to design a vending machine (自動販賣機). The system diagram is shown in Figure 6 and you are asked to design the “System Control” module of the vending machine. The machine receives $1, $5, and $10 coins and sales two products. Product A costs $15 and Product B costs $20. The system operates as follows.
2. Each time the user inserts a coin, the “Coin Sensor” module detects the type of the coin and generates a one-cycle logic-1 pulse on *X*1, *X*5, or *X*10, depending on the value of the coin.
3. When the user pushes a product selection button, a one-cycle logic-1 pulse is generated on either *YA* or *YB*, depending on the product selected.
4. If the coins inserted are sufficient to purchase the required product, the “System Control” module generates a 1-cycle pulse on *RA* or *RB* nets, depending on the selected product type, to inform the “Mechanics Control” module to release the required product. Amount of changes for returning to the user is also informed through the *n*-bit bus *C*. Note that the system state remains unchanged if not sufficient amount of cash inserted.
5. After the product is released and the change is returned to the user, the machine returns to an idle state and waiting for the next user to insert coins.

Draw the circuit diagram of the “System Control” module to show your design.

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**Figure 6.**