長 庚 大 學 資 訊 工 程 系 計 算 機 組 織 期 中 考 試 題 ２０１６／１１／１８

(1) 可翻閱參考書籍

(2) 考試時間：1:10PM – 3:00PM

General answering rules:

(i) You can use any components (such as AND-gate, adder, comparator, mod-N counter, etc.) that ever mentioned in this course and the digital circuit course without showing the detailed design of these components.

(ii) For a combinational circuit part in your design, you just have to specify the Boolean equation or the truth table of this part. You don't need to draw the gate-level circuit diagram for a combinational circuit.

1. **(15 pts)** Design a circuit with the behavior specified in the state-transition diagram shown in Figure 1. The circuit has four states and one input signal *X*.
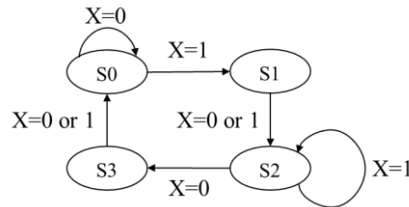

Figure 1.

2. **(10 pts)** Design a frequency divider. The spec is shown in Figure 2. The circuit receives a clock signal (CLK) with 1 KHz frequency as input and generates an output signal PCLK in 1 Hz with 50% duty cycle. Draw the block diagram of your design
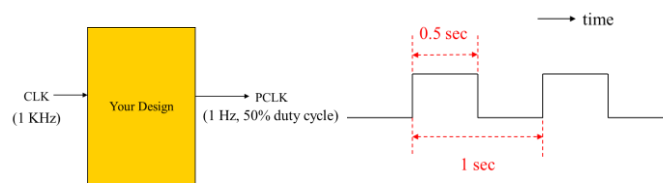

Figure 2.

3. **(10 pts)** You are asked to design a circuit to keep track of amount of cars currently stayed in parking space. (停車場). The parking space has two gates: one for entry and the other for exit. Sensors are embedded for each gate. At most 50 cars can stay in the parking space. Your task is to design a circuit meeting the spec shown in Figure 3. The sensor in the entrance sends a 1-cycle pulse SI=1 to your circuit. Similarly, the sensor in the exit gate sends a 1-cycle pulse SO=1 to your circuit. Your circuit sends out amount of cars currently in the parking space through bus Q. Draw the circuit diagram of your circuit to monitor amount of cars in the parking space.
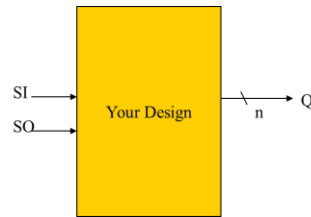
Figure 3.

4. **(15 pts)** Design a circuit that acts like a stack to send out input numbers in reverse order. The signal interface is shown in Figure 4 and the required behavior is shown in Figure 5. Upon receiving the "start" signal, two input numbers A and B will be send into the circuit in two consecutive cycles. In the coming two cycles after receiving the two input numbers, your design should send out the two numbers in reverse order. Present your design alone with how your design is devised (such as state-transition diagram for the control, micro-operations to be realized, etc.)
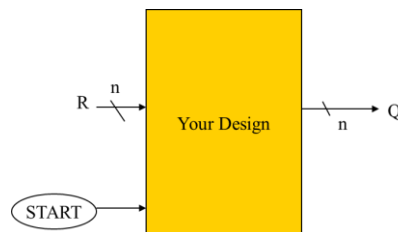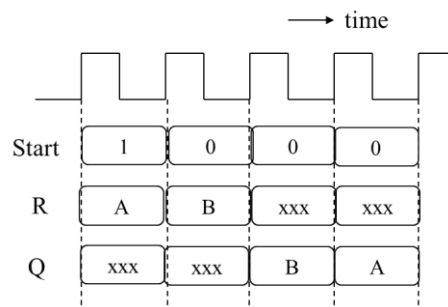

Figure 4.

Figure 5.

5. **(20 pts)** Design a circuit the select the maximum input number as the output. The signal interface is in Figure 4. The expected timing behavior is shown in Figure 6. Upon receiving the "start" signal, two numbers A and B will be given in two consecutive cycles. At the 3rd cycle, your circuit should send out the maximum number between A and B. Draw the circuit diagram alone with your design rationale.
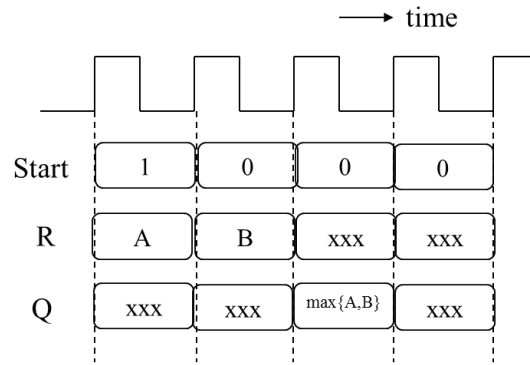
Figure 6.

6. **(25 pts)** Design a circuit to count amount of exact matches and hits among two groups of numbers. The signal interface is shown in Figure 7. The inputs are divided into two groups, $\{A_i\}$ and $\{B_j\}$, each group has 4 numbers. We say B_j is an exact match if $B_j = A_j$. And B_j is a hit if $B_j = A_i$ for some $i \neq j$. Several cycles later (depending on your design), the circuit generates amount of exact matches through output port Q_A and amount of hits through output port Q_B. Note that you can use at most 4 equality comparators. Write down your design with design rationale.
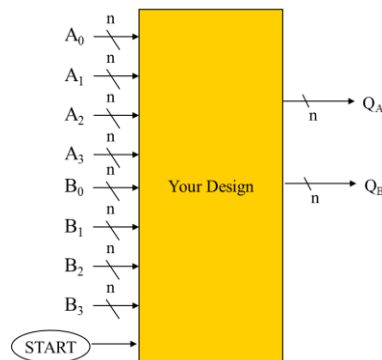

Figure 7.

7. **(30 pts)** Design a circuit to calculate the greatest common divisor (最大公因數) of two input integer numbers A and B. Define the spec by yourself. Present your design alone with how you devise your design starting from the mathematics principle.