

# ModelSim Simple Example

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SoC Lab, CGUCSIE

January 5, 2010

About

Installization

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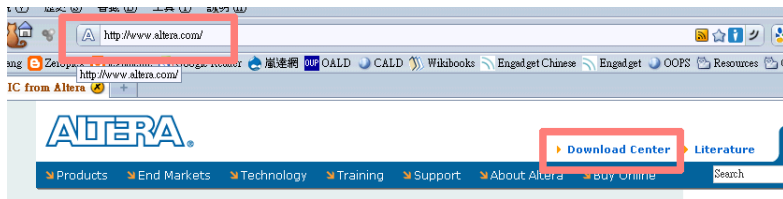
Install

Build a project

Discusses

## Download

- ▶ go to <http://www.altera.com>, and press “Download Center”



# Download

- ▶ Press “ModelSim-Altera” in the “Altera Edition Third-Party Software” block

**Altera Edition Third-Party Software**

- Mentor Graphics® **ModelSim®-Altera®** (two versions available)
- Verilog and VHDL simulation software
  - ModelSim-Altera Starter Edition—No License Required!
  - ModelSim-Altera Edition—A License is Required!
- [VHDL 93 Simulation Model Library](#)
  - VHDL 93-compliant simulation model library files

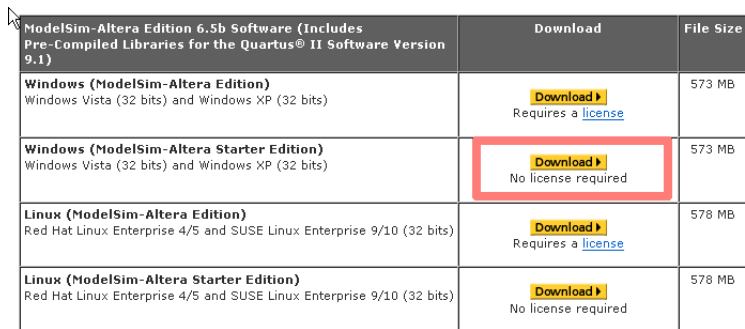
# Download

- Press “6.4a” in the “ModelSim-Altera Starter Edition” block

Download ModelSim-Altera Software			
ModelSim-Altera Starter Edition <b>NEW</b>	ModelSim-Altera Web Edition (1)	ModelSim-Altera Edition	Notes
<a href="#">6.5b</a>	—	<a href="#">6.5b</a>	Use with Quartus II software version 9.1 only
<a href="#">6.4a</a>	—	<a href="#">6.4a</a>	Use with Quartus II software version 9.0 only

## Download

- ▶ Press “Download” picture in the “ModelSim-Altera Starter Edition” block



ModelSim-Altera Edition 6.5b Software (Includes Pre-Compiled Libraries for the Quartus® II Software Version 9.1)	Download	File Size
<b>Windows (ModelSim-Altera Edition)</b> Windows Vista (32 bits) and Windows XP (32 bits)	<a href="#">Download ▶</a> Requires a <a href="#">license</a>	573 MB
<b>Windows (ModelSim-Altera Starter Edition)</b> Windows Vista (32 bits) and Windows XP (32 bits)	<a href="#">Download ▶</a> No license required	573 MB
<b>Linux (ModelSim-Altera Edition)</b> Red Hat Linux Enterprise 4/5 and SUSE Linux Enterprise 9/10 (32 bits)	<a href="#">Download ▶</a> Requires a <a href="#">license</a>	578 MB
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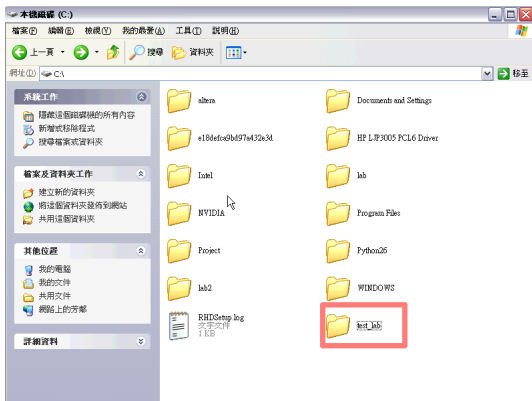
- ▶ The Next step is mentioned in “Quartus II 安裝與建置”

# Install

請自行安裝 XD

## 建立資料夾

- ▶ 首先我們在 C:\ 底下建立一個 “test\_lab”
- ▶ 注意: ModelSim 不接受中文檔名及路徑,  
所以千萬不要把資料放在桌面(桌面本身就含有中文路徑。)





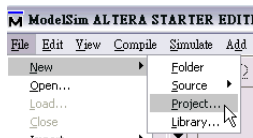
- copy file(testbench.v, data\_memory.v data.mem) to the folder



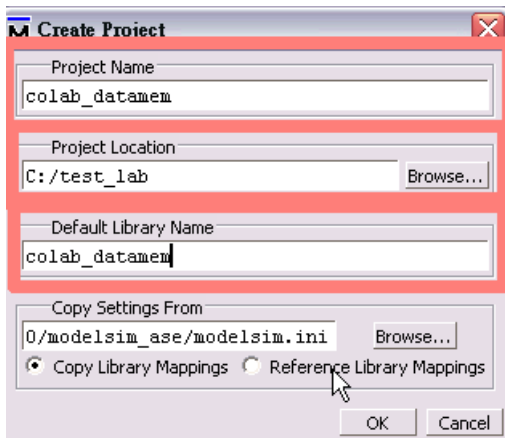
► Open “ModelSim Starter Edition”



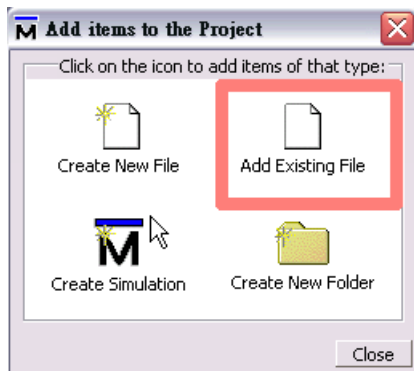
- ▶ Press “File” → “Project”



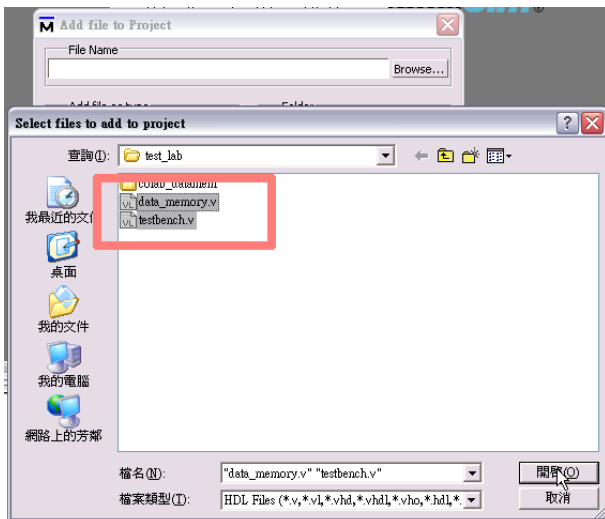
- ▶ Project Name — 不要亂取
- ▶ Project Location — 選取你剛剛所建立的資料夾
- ▶ Default Library — 取一個有意義的名字，等一下會用到



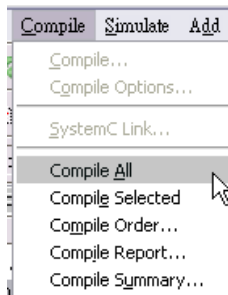
- Press “Add Existing File”



- ▶ Press “Browse”
- ▶ Choose the file what you copied testbench.v, data\_mem.v



- Press “Compile” → “Compile All”



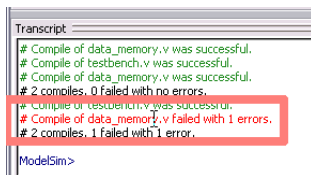
- ▶ You can see message window in the below. It will tell you compile result.
- ▶ You will see “sucessful”.

```
Transcript
# Reading C:/altera/90/modelsim_ase/tcl/vsim/pref.tcl
# Project file C:/test_lab/instr/colab_instr.mpf was not found.
# Unable to open project.
# Loading project colab_datamem
# Compile of testbench.v was successful.
# Compile of data_memory.v was successful.
# 2 compiles, 0 failed with no errors

ModelSim>
```



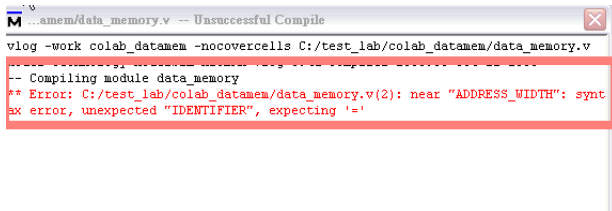
- ▶ If the program have compile error, it would appear **Red word** in the message window.



```
Transcript
# Compile of data_memory.v was successful.
# Compile of testbench.v was successful.
# Compile of data_memory.v was successful.
# 2 compiles. 0 failed with no errors.
# Compile of testbench.v was successful.
# Compile of data_memory.v failed with 1 errors.
# 2 compiles. 1 failed with 1 error.

ModelSim>
```

- ▶ You will see the error message after **pressed** the **Red word**



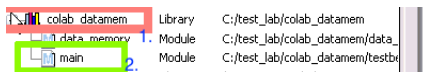
```
...amem/data_memory.v -- Unsuccessful Compile
vlog -work colab_datamem -nocovercells C:/test_lab/colab_datamem/data_memory.v

-- Compiling module data_memory
** Error: C:/test_lab/colab_datamem/data_memory.v(2): near "ADDRESS_WIDTH": synt
ax error, unexpected "IDENTIFIER", expecting '='
```

- ▶ Press “Library” tag page

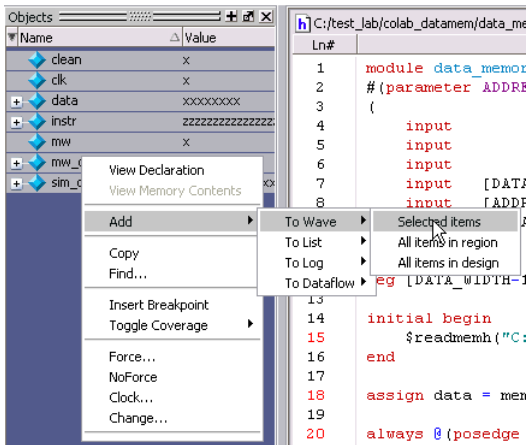


- ▶ find “colab\_datamem”(your “Default Library Name”) and Press “main”

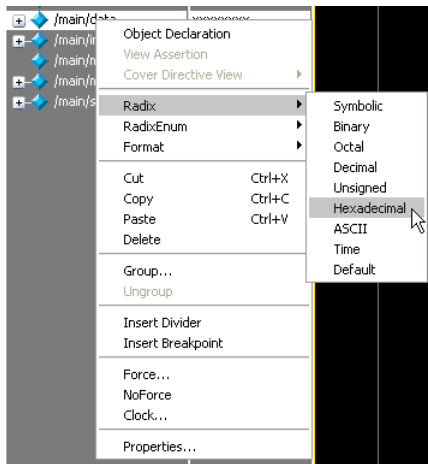




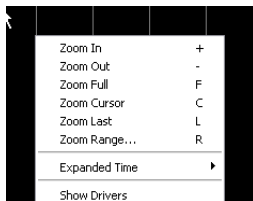
► 選擇你所要顯示的訊號加入 waveform



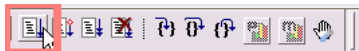
- ▶ every signal show in binary format, you can select the item and press right button of mouse. “Radix” → “Hexadecimal” or “Unsigned”



- ▶ Press right button of mouse in the waveform view, you can Zoom in it.
- ▶ A clock cycle's default length is 10ps.



- ▶ The program will start to simulate after press the button.



- ▶ You will see the simulate result in the waveform view



- ▶ If you set \$display(), you will see the output in the message window.

# Do you have any problem ?