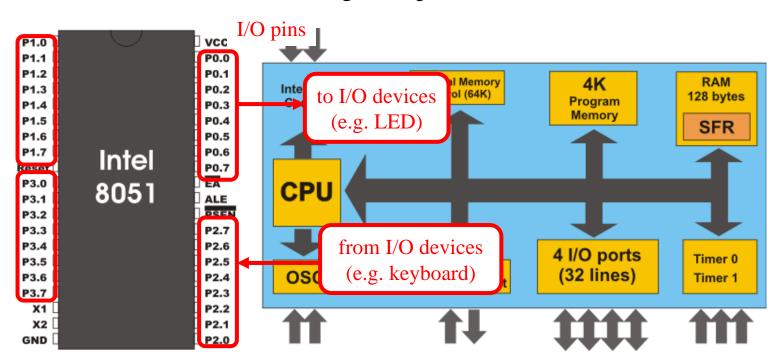
Lab 02 General Purpose Digital I/O (GPIO)

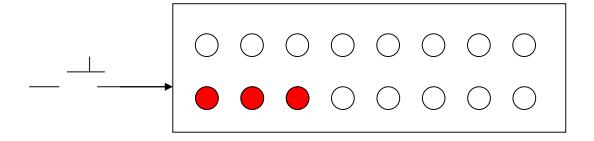
Objectives of this lab

- to build up your imagination on how a program affects hardware signals
- to learn how to send/receive signals from an application processor to external devices through I/O pads



Your work today

- design a LED box
 - initial: all LED off
 - the LED runs some pattern after some button pressed
 - you can design your own pattern



Outline

- Basic concepts of I/O control
- I/O model of legacy 8051 processor
- SiliconLab C8051F040 I/O control
- Simplified programming model

Preparations before the Lab

- Read the data sheet of SiliconLab C8051F040 SoC
 - Chap. 17
- Read the schematics of the Big8051 experiment board
 - On LEDs

Pre-Lab Report

- Q1: Explain what is watch-dog timer
 - Somewhere in your OS textbook
- Q2: Explain what is memory-mapped I/O
 - Check the textbooks of Computer Organization,
 Computer Architecture, or OS

Pre-Lab Report (cont'd)

- Q3:
 - Read Figure 17.1 of C8051F040 spec and the schematics of Big8051
 - List all control signal values to turn-on an LED at P0.0

/WEAK-PULLUP (WEAK) PORT-OUTPUT DGND Analog Select (Ports 1, 2, and 3) ANALOG INPUT PORT-INPUT

Value of these Control signals

Figure 17.1. Port I/O Cell Block Diagram

Pre-Lab Report (cont'd)

- Q4:
 - Read Figure 17.2 of C8051F040 spec
 - List the values of all control registers to configure port P0 as a digital output port

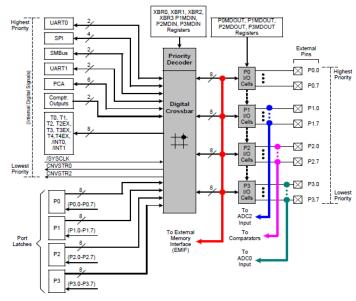
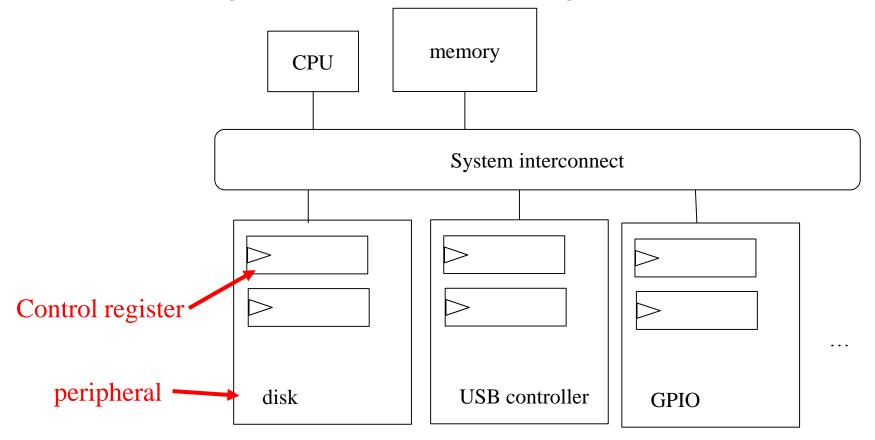


Figure 17.2. Port I/O Functional Block Diagram

General I/O Control Model

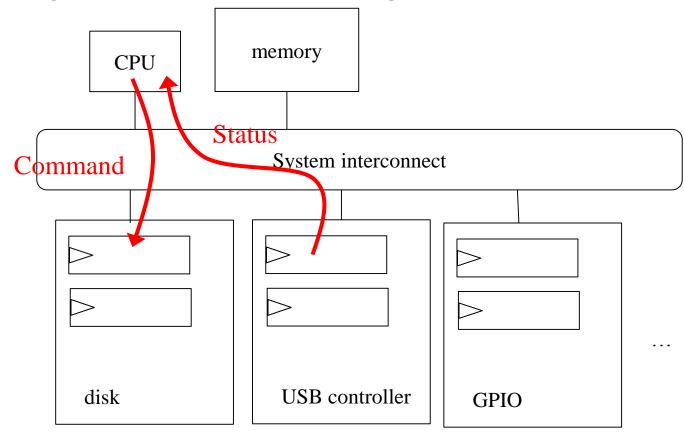
How a processor commands an I/O peripheral

Through access control registers



How a processor commands an I/O peripheral

Through access control registers



How to access control registers: the memory-mapped I/O

- Part of the addressing space is assigned to control registers
- Each control register is mapped to some memory address

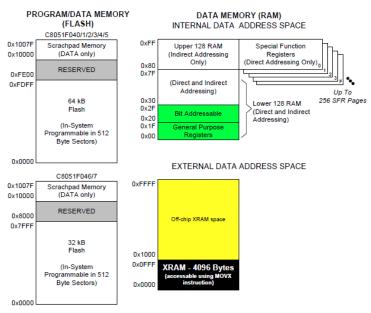
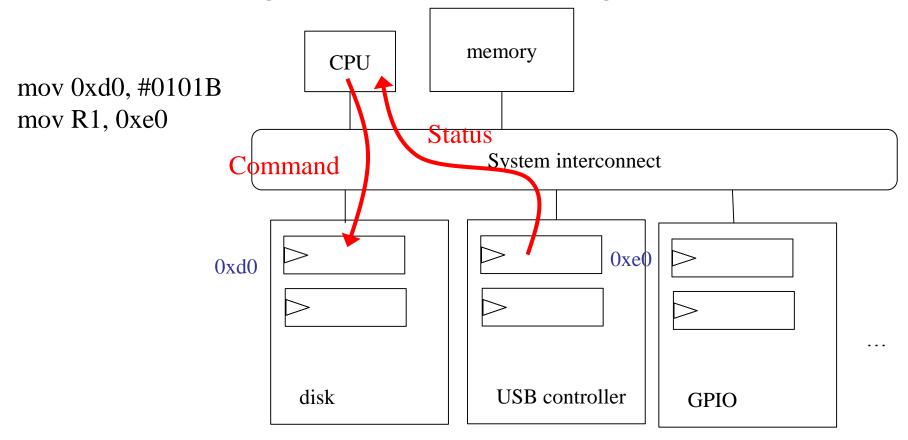


Figure 1.7. On-Chip Memory Map

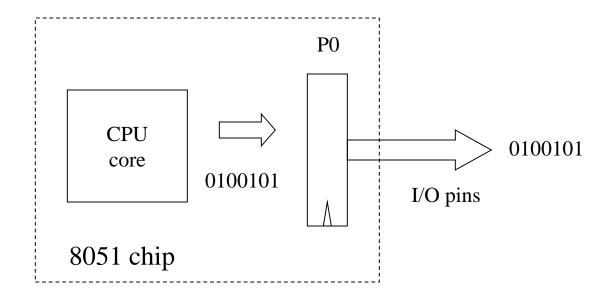
How a processor commands an I/O peripheral

Through access control registers



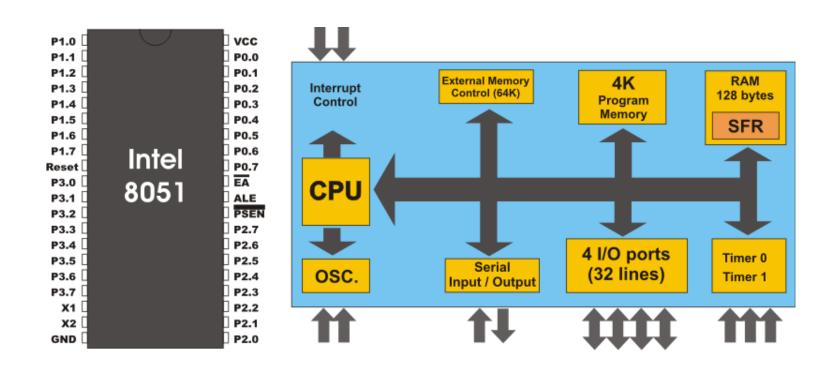
General Purpose Digital I/O

 the processor assigns/examines the logical status of some I/O pins directly

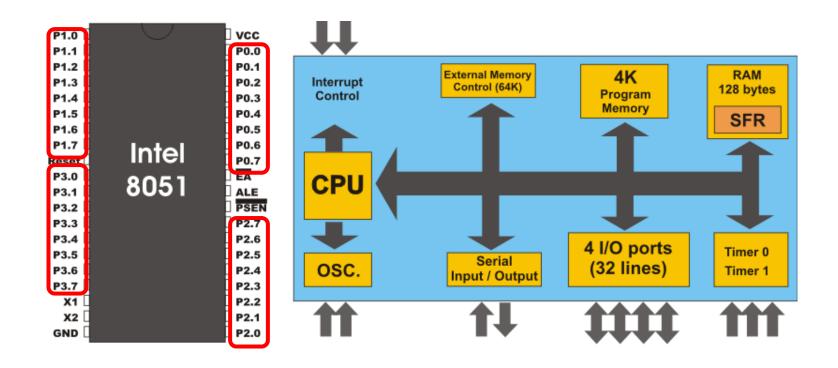


I/O Model of Legacy 8051 Processor

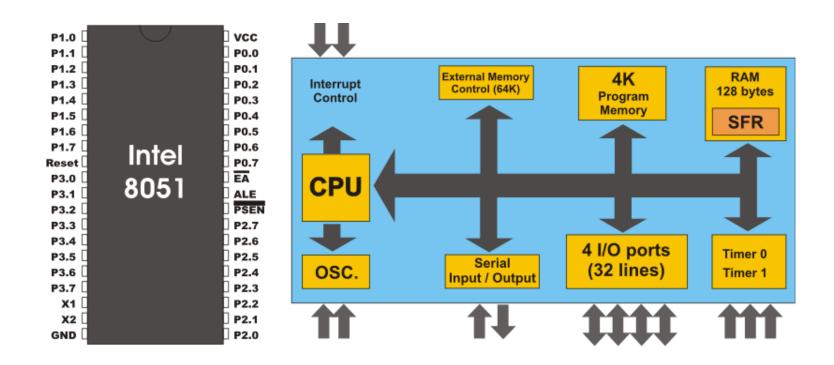
- four 8-bit I/O ports P0-P3
- (2) each pin is bidirectional
 - sometimes input and sometimes output



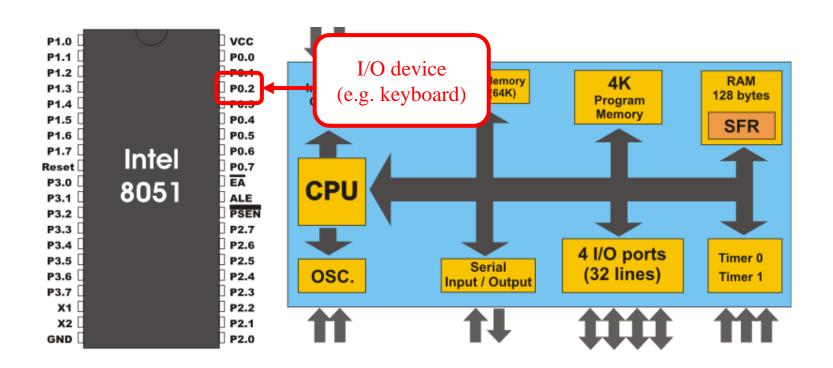
- four 8-bit I/O ports P0-P3
- (2) each pin is bidirectional
 - sometimes input and sometimes output



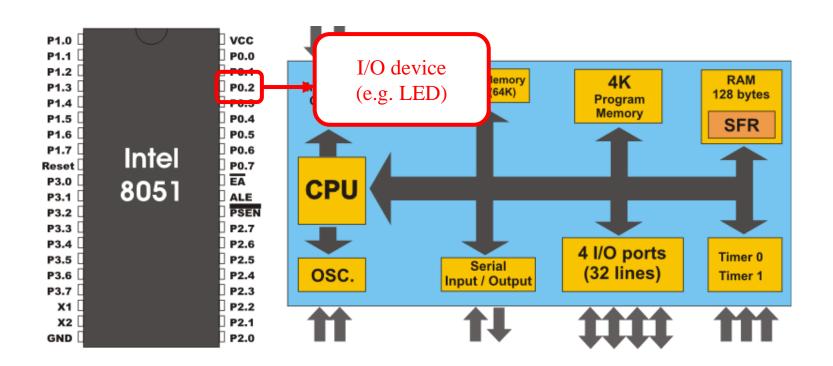
- four 8-bit I/O ports P0-P3
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- four 8-bit I/O ports P0-P3
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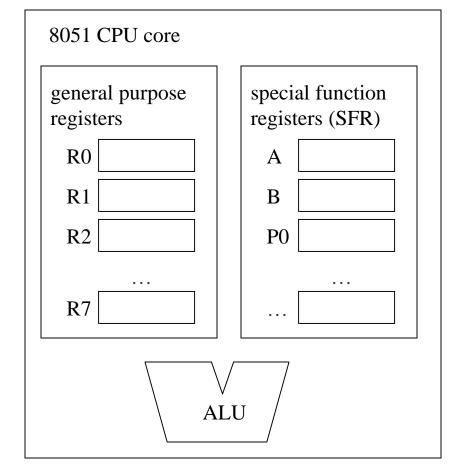


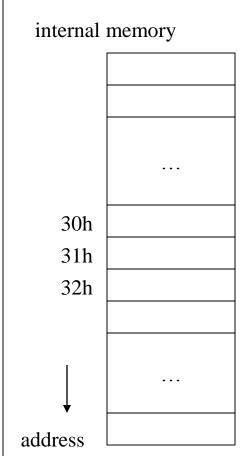
- four 8-bit I/O ports P0-P3
- (2) each pin is bidirectional
 - sometimes input and sometimes output



Imagination on 8051 architecture

Imagine how data flow in the architecture!





How to program I/O ports?

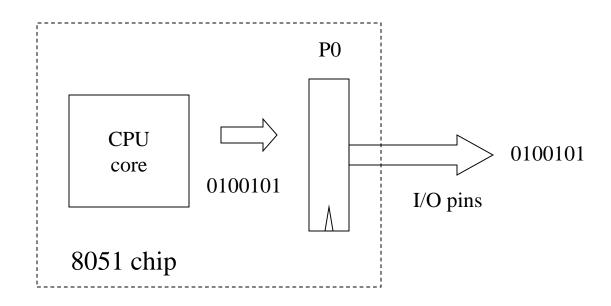
through SFRs P0-P3

F8								FF
F0	В							F7
E8								EF
E0	ACC							E7
D8								DF
D0	PSW							D7
C8								CF
C0								C7
B8	IΡ							BF
B0	P3							В7
A8	TE							AF
A0	P2							A7
	SCON	SBUF						9F
90	P1							97
88	TCON	ГМОD	TL0	TL1	TH0	TH1		8F
80	P0	SP	DPL	DPH			PCON	87

Bit-addressable Registers



MOV R0, #01001101B MOV P0, R0





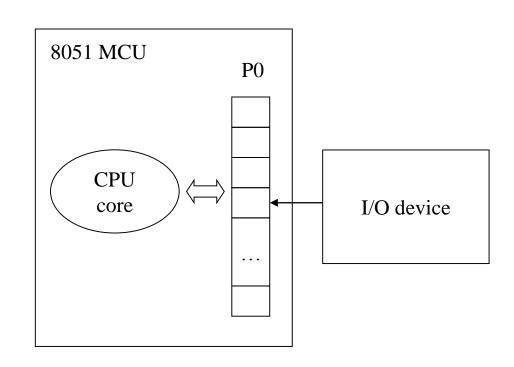
The case of input (receive)

- initial: set a bit (pin) with value 1
- receive (input): wait for the bit to be toggled to be 0

P0.3 = 1

//wait unit P0.3 been set to 0
while (P0.3==1);

//action for the I/O event





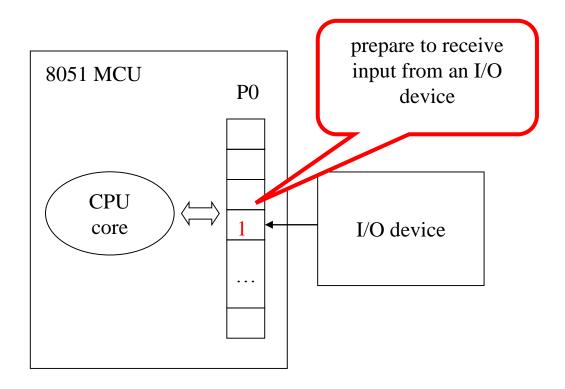
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The case of input (receive)

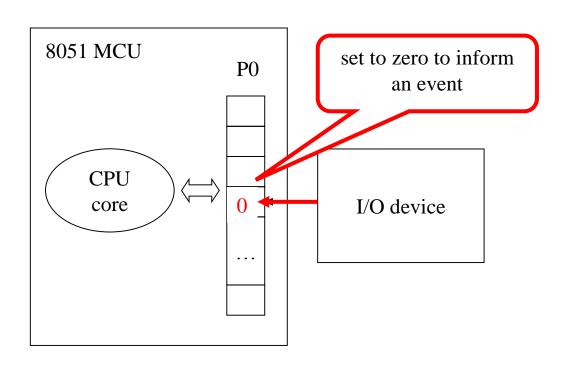
- initial: set a bit (pin) with value 1
- receive (input): wait for the bit to be toggled to be 0

P0.3 = 1

//wait unit P0.3 been set to 0

while (P0.3==1);

//action for the I/O event



The GPIO of C8051F040 SoC

Overview of SFR

- Extension from legacy 8051
- Divided into 3 pages
- Page 145-149 of the C8051F040 data sheet

The port configuration

 Set XBR2, PxMDIN and PxMDOUT to set port Px as general purpose I/O

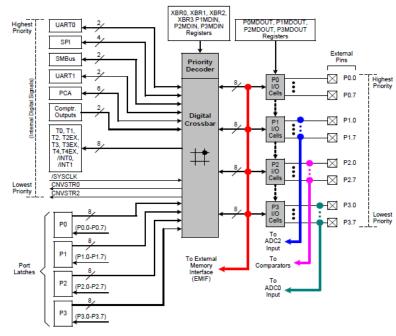


Figure 17.2. Port I/O Functional Block Diagram

The I/O pad

■ To send output 1

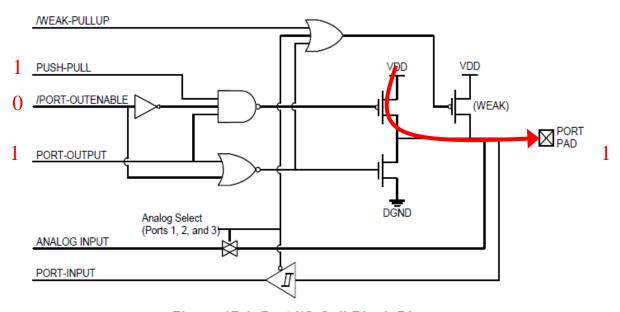


Figure 17.1. Port I/O Cell Block Diagram

The I/O pad

■ To send output 0

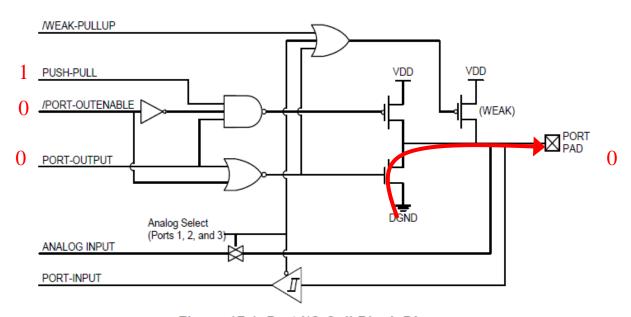
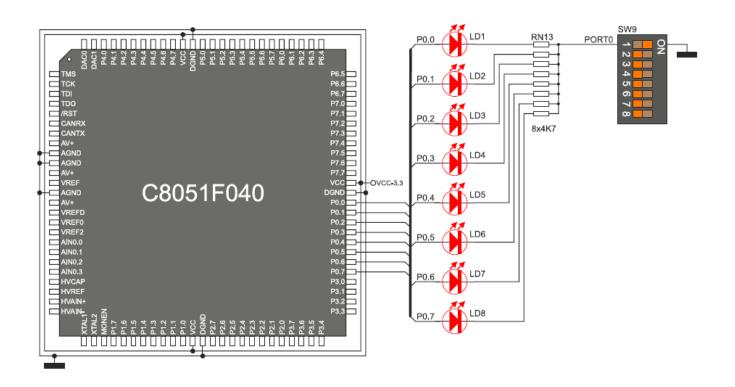


Figure 17.1. Port I/O Cell Block Diagram

Schematics of the LED

mov P0, #10000000h to turn on LD8



Example 1

Detect button press and display on LED

Example Code

```
define control registers (with address)
XBR2
                 equ
                         0e3h
P1MDIN
                         Oadh
                 equ
P2MDOUT
                         Oa6h
                 equ
WDTCN
                         Offh
                 equ
SFRPAGE
                         084h
                 equ
Р1
                         090h
                 equ
P2
                         OaOh
                 equ
define control words
CONFIG PAGE
                         0 \, \text{fh}
                 equ
LEGACY PAGE
                 equ
                         00h
                 ; turn-off the watch-dog timer
                         WDTCN, #0deh
                 mov
                         WDTCN, #Oadh
                 mov
                 ;setup port Configuration
                         SFRPAGE, #CONFIG_PAGE
                         XBR2, #ÓcOh
                 wow
                         PlMDÍN, #Offh
                 mov
                         P2MDOUŤ, #0ffh
                 wow
                         SFRPAGE, #LEGACY PAGE
                 mov
                         RO, #0
                 wow
                 ;detect button and display
Loop_Begin:
                         RO, P1
                 mov
                         P2, R0
                 mov
                         Loop_Begin
                 simp
                 end
```

Example 2: wait for a button pressed

Demo: wait for a button pressed

```
wait:
```

A = P1; if (A==0) goto wait;

exit:

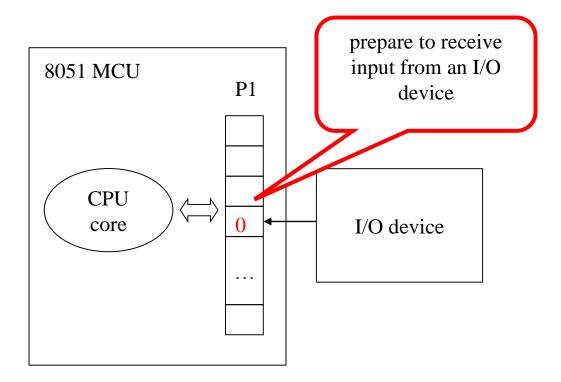
//something after button pressed

wait:

mov A, P1 JZ wait

exit:

//something after button pressed



Demo: wait for a button pressed

```
wait:
```

A = P1; if (A==0) goto wait;

exit:

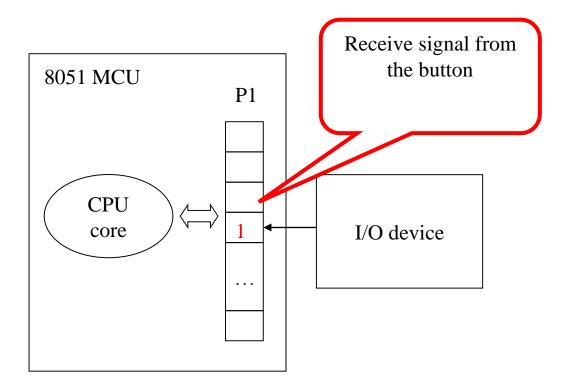
//something after button pressed

wait:

mov A, P1 JZ wait

exit:

//something after button pressed



Example 3: make LED run

show how to output signal

MAIN:

MOV A, #11111110B

MOV PSW, #00H

Loop:

MOV P0, A

LCALL Delay

RR A

LJMP Loop

MOV R0, #50

Delay: MOV R1, #40

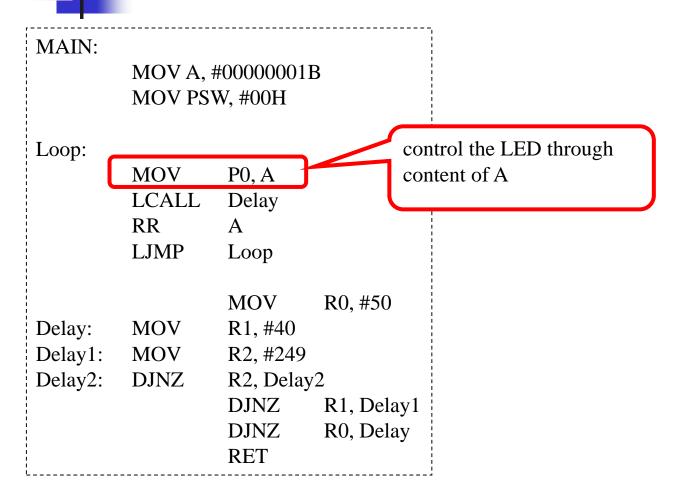
Delay1: MOV R2, #249

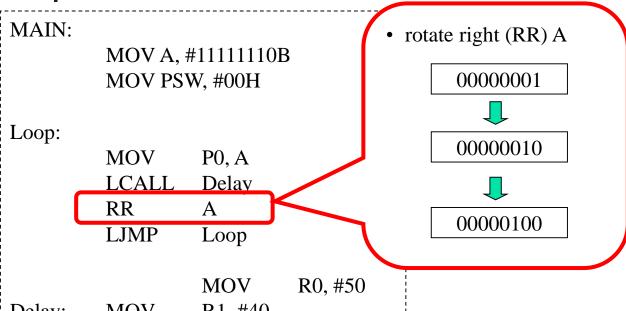
Delay2: DJNZ R2, Delay2

DJNZ R1, Delay1

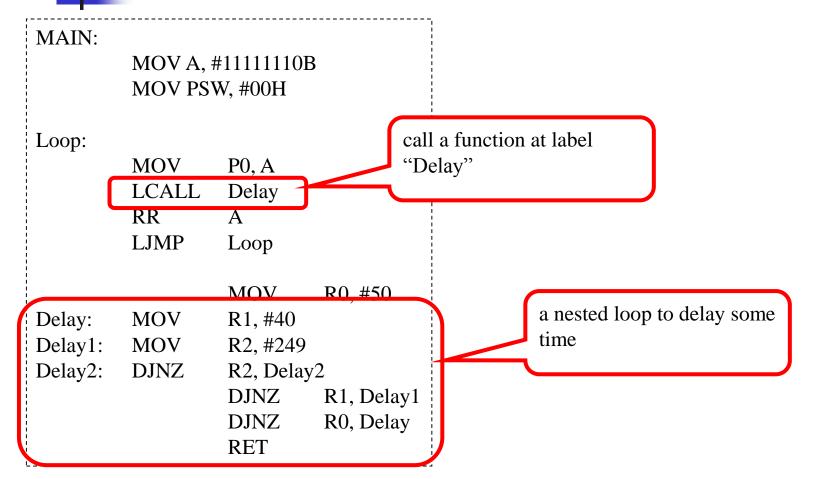
DJNZ R0, Delay

RET





Delay: MOV R1, #40
Delay1: MOV R2, #249
Delay2: DJNZ R2, Delay2
DJNZ R1, Delay1
DJNZ R0, Delay
RET



The Next Lab: Timer and Interrupt

Your Work at Lab 03

 make LED run but using the timer interrupt to trigger pattern change

Pre-Lab Report

- Q1: what is interrupt?
 - check Mano: logic and computer design fundamentals, Section 10-9

- Q2: how to setup an ISR on 8051
 - ISR: interrupt service routine