

Carlos Gross-Martinez

CDA3201C

Logic Design Course

Lab 0 – First circuit wiring design

Truth Table:

- 0) [5] This lab experiment is used for the lab orientation where TAs will walk you through practical steps to build the experiment circuit and test it. You will use the following simple function:

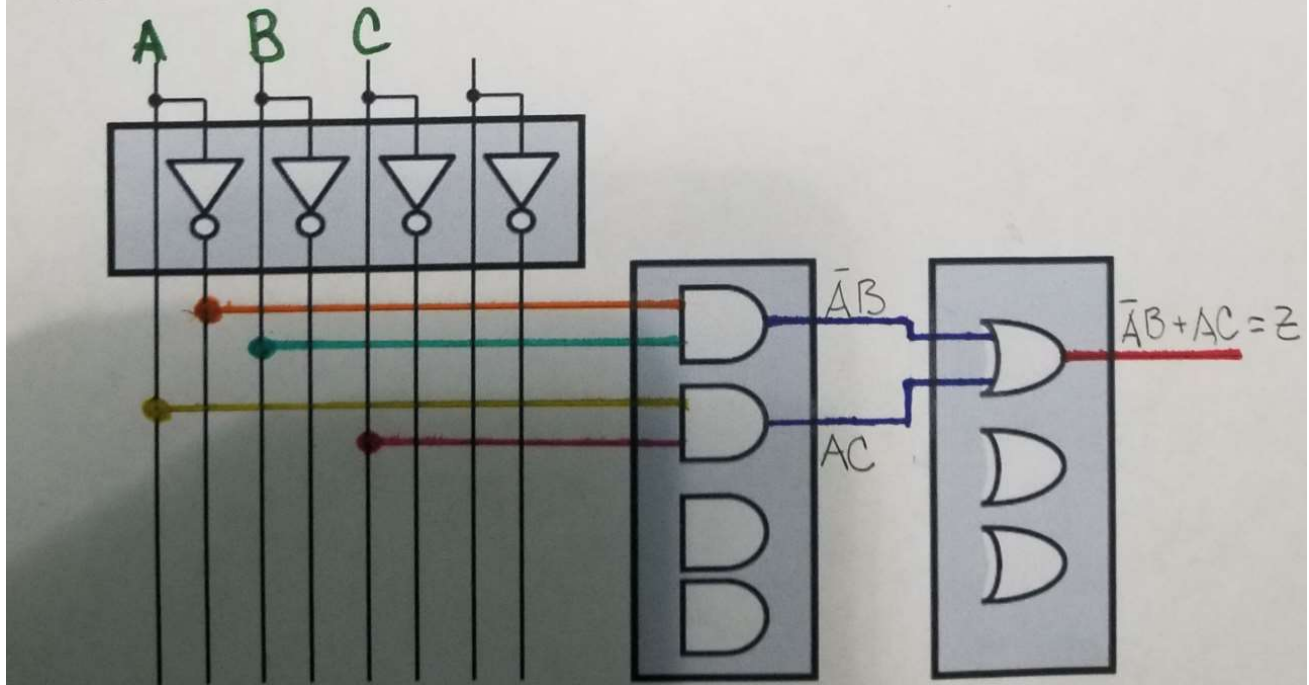
$$Z = A'B + AC$$

- 0.a) [0] Fill the truth table for the above function

A B C	A' B	A C	Z
000	0	0	0
001	0	0	0
010	1	0	1
011	1	0	1
100	0	0	0
101	0	1	1
110	0	0	0
111	0	1	1

Logic Circuit Drawing ($Z = A'B + AC$)

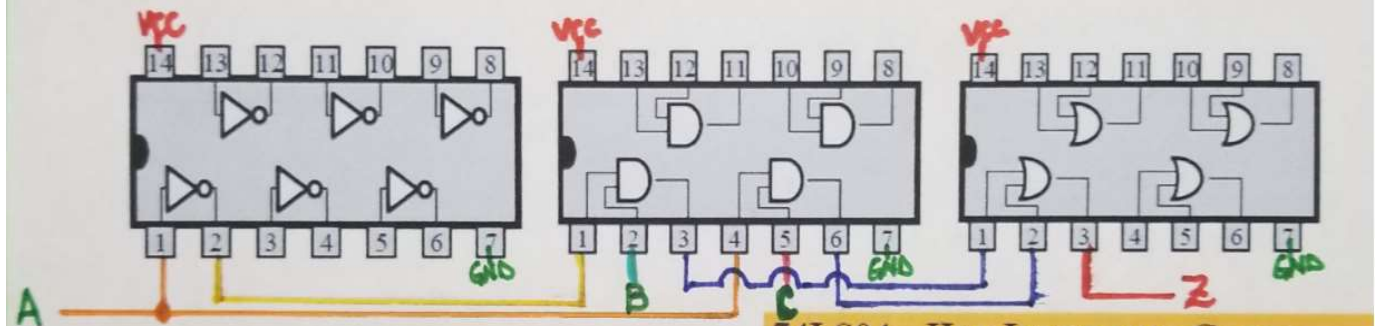
- 0.b) [0] Draw the switching function ($Z = A'B + AC$) using Inverters, AND gates, and OR gate:



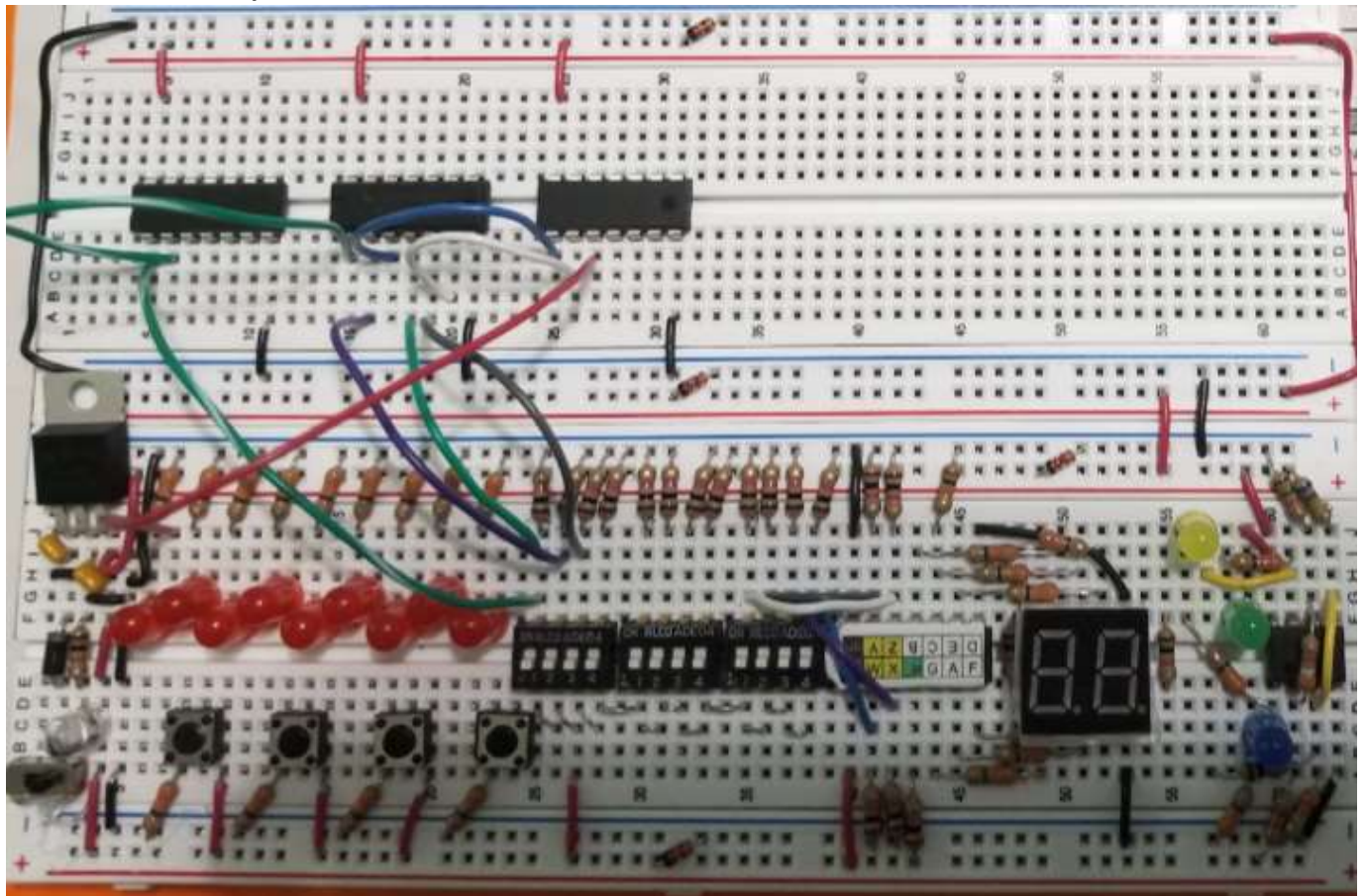
Drawing Using Logic Chips ($Z = A'B + AC$)

0.c) [10] Using the three logic chips below, draw the wires to make the needed connections between the various gates. Note that not all gates in all chips are used.

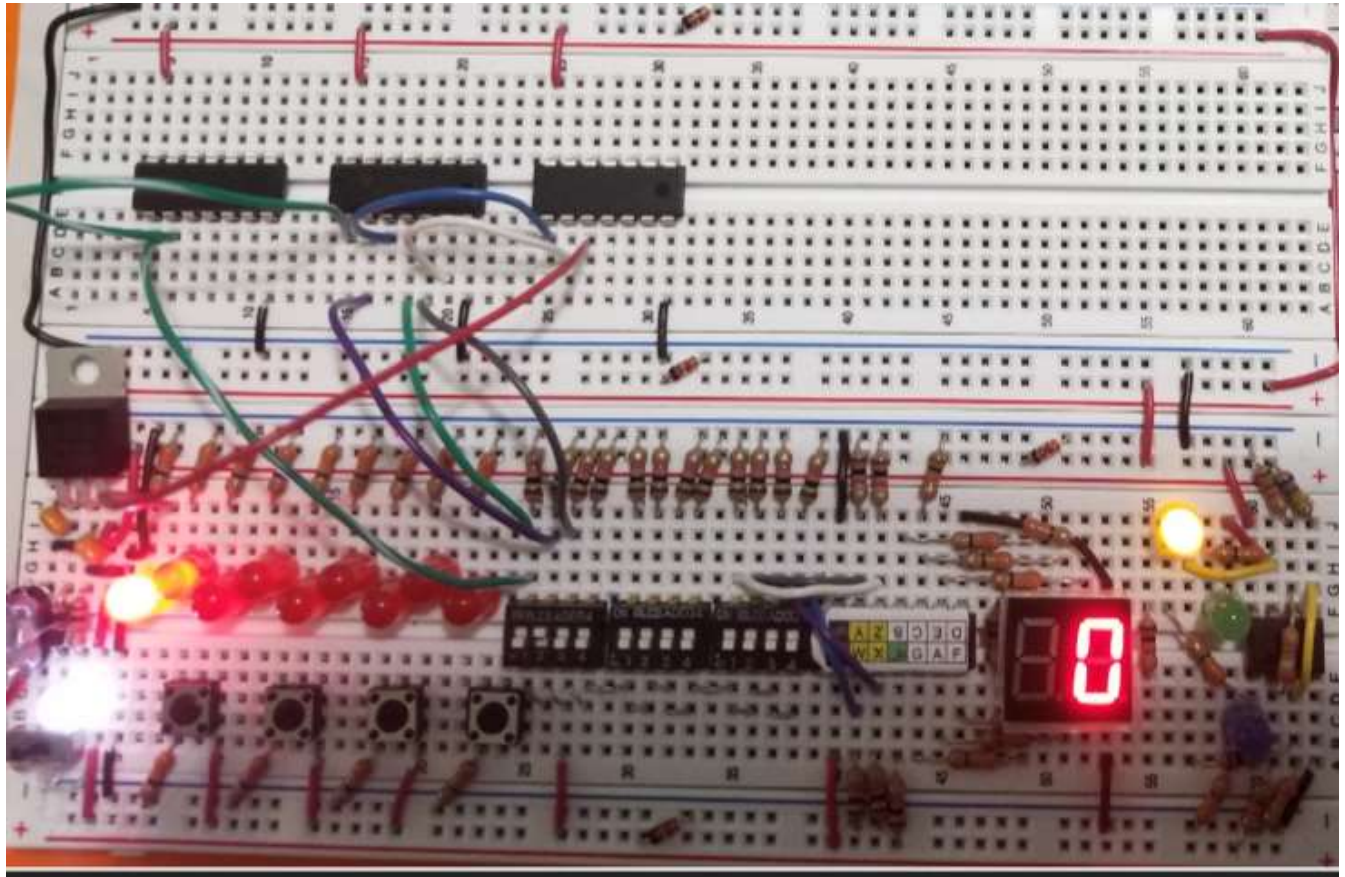
NOTE FROM DR. PETRIE – Do not remove NOT, AND, OR, and NAND chips and wires from 1st part. Look at gates that you did not use in those chips, identify the switches that you will designate A, B, C, note you already have available A and A'. Utilize the open gates and draw the circuits for **$Z = A'B + AC$**



Picture of Completed Circuit on breadboard

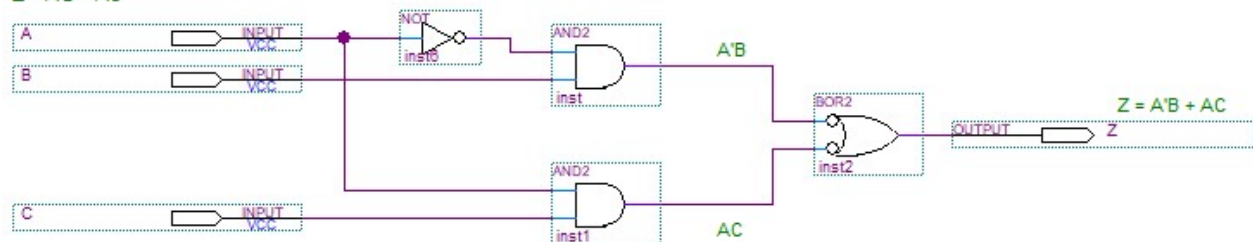


Picture of Completed Circuit on breadboard Working



Quartus Schematic

Carlos Gross-Martinez
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Logic Design Course
Dr. Maria Larrondo Petrie
Lab 0 - First Circuit Wiring Design
 $Z = A'B + AC$



Quartus Compilation Result

Quartus II - C:\Users\Carlos Gross\Desktop\Fall 2019\LogicDesign\LabPortfolio\Lab0\Quartus\Lab0 - Lab0

File Edit View Project Assignments Processing Tools Window Help

Lab0

Project Navigator

Entity: MAX3000A: EPM3032ALC44-10
Lab0

Macros: 1
Pins: 8

Tasks

Flow: Compilation

Task ID: 1
Task Name: Compile Design
Time: 00:00
Status: Success

Task ID: 2
Task Name: Analysis & Synthesis
Time: 00:00
Status: Success

Task ID: 3
Task Name: Filter
Time: 00:00
Status: Success

Task ID: 4
Task Name: Assembler
Time: 00:00
Status: Success

Task ID: 5
Task Name: Classic Timing Analysis
Time: 00:00
Status: Success

Task ID: 6
Task Name: EDA Netlist Writer
Time: 00:00
Status: Success

Compilation Report - Flow Summary

Flow Status: Successful - Fri Sep 13 18:06:32 2019

Quartus II Version: 9.1 Build 250 03/24/2010 SP 2 SJ Web Edition

Revision Name: Lab0

Top-Level Entity Name: Lab0

Family: MAX3000A

Device: EPM3032ALC44-10

Timing Models: Final

Met timing requirements: Yes

Total macros: 1 / 32 (3 %)

Total pins: 8 / 34 (24 %)

Compiler Tool

Analysis & Synthesis: 100 %
Filter: 100 %
Assembler: 100 %
Classic Timing Analyzer: 100 %

Full Completion: 100 %
00:00:04

Start Stop Report

View Quartus II Information
Documentation

Message: Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off Lab0 -c Lab0
Info: Started post-fitting delay annotation
Info: Delay annotation completed successfully
Warning: Timing Analysis does not support the analysis of latches as synchronous elements for the currently selected device family
Warning: No paths found for timing analysis
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 0 warnings

System [13] Processing [28] Extra Info [4] Info [24] Warning [4] Critical Warning [0] Error [0] Suppressed [0] Flag [0]

Message 0 of 60

For Help, press F1

Quartus Waveform

Quartus II - C:\Users\Carlos Gross\Desktop\Fall 2019\LogicDesign\LabPortfolio\Lab0\Quartus\Lab0 - Lab0 - [Lab0.vwf]

File Edit View Project Assignments Processing Tools Window Help

Lab0

Project Navigator

Entity: MAX3000A: EPM3032ALC44-10
Lab0

Macros: 1
Pins: 8

Tasks

Flow: Compilation

Task ID: 1
Task Name: Compile Design
Time: 00:00
Status: Success

Task ID: 2
Task Name: Analysis & Synthesis
Time: 00:00
Status: Success

Task ID: 3
Task Name: Filter
Time: 00:00
Status: Success

Task ID: 4
Task Name: Assembler
Time: 00:00
Status: Success

Task ID: 5
Task Name: Classic Timing Analysis
Time: 00:00
Status: Success

Task ID: 6
Task Name: EDA Netlist Writer
Time: 00:00
Status: Success

Master Time Bar: 200.0 ns
Interval: 2.3 ns
Start: -197.7 ns
End: 200.0 ns

Inputs: A, B, C, Z

Value at 200.0 ns: A: 0, B: 0, C: 0, Z: A1

Waveform: 0 ps, 20.0 ns, 40.0 ns, 60.0 ns, 80.0 ns, 100.0 ns, 120.0 ns, 140.0 ns, 160.0 ns, 180.0 ns, 200.0 ns

Waveform Data: 000, 001, 010, 011, 100, 101, 110, 111

Message: Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 71.43 %
Info: Number of transitions in simulation is 114
Info: Vector file Lab0.vwf is saved in VWF text format. You can compress it into CWF format in order to reduce file size. For more details please refer to the Quartus II Help.
Info: Quartus II Simulator was successful. 0 errors, 0 warnings