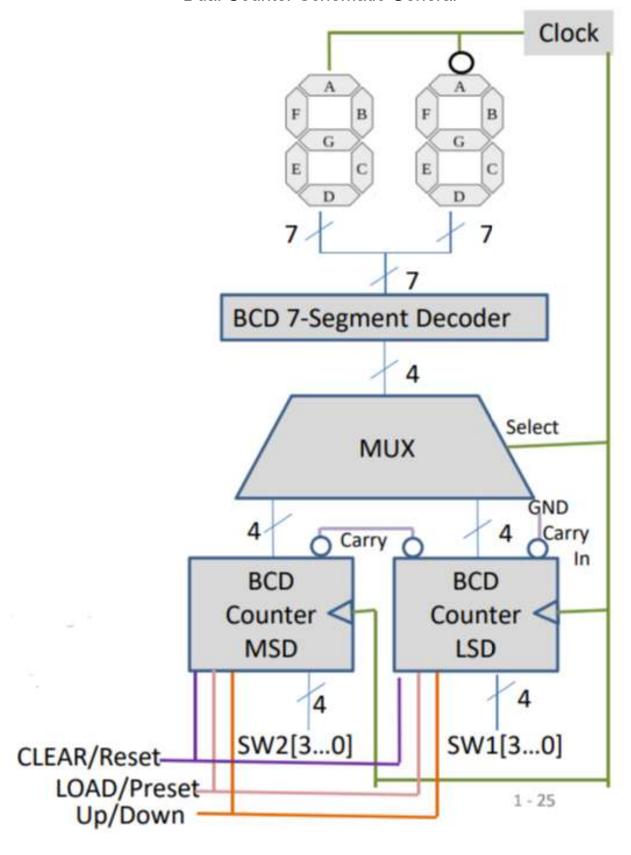
Carlos Gross-Martinez

CDA3201C

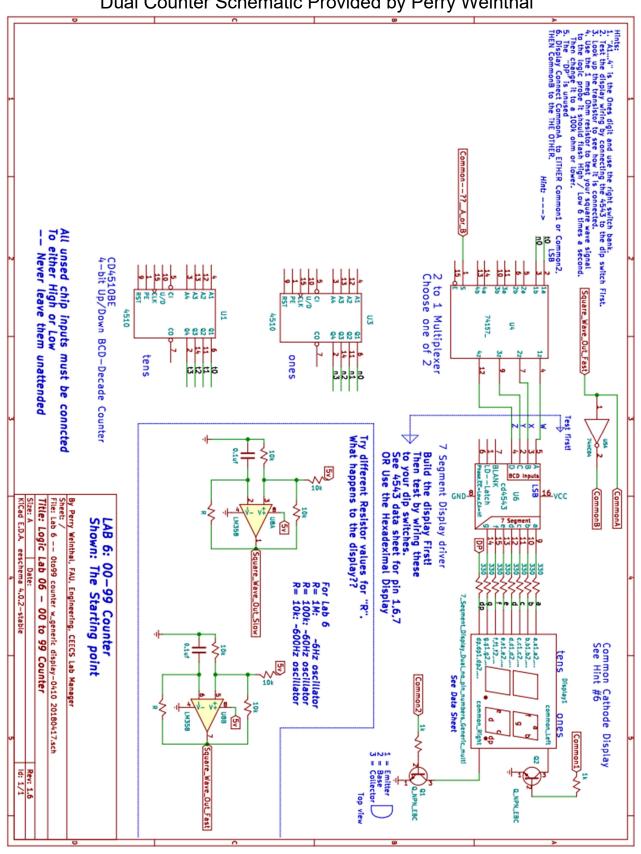
Logic Design Course

Lab 6: Dual Counter

Dual Counter Schematic General



Dual Counter Schematic Provided by Perry Weinthal



Dual Counter Logic Drawing 16 WOOD Lab 6 INPUTS: S CLOC MSB CD4510BE O dot 12 40 2 PRESET-ENABLE TL (CLOCK) RESET 15 CLOCK UP/DOWN 4 0 CD4510BE 1SB SW1[842]] vss Aub 1A 1B 1Y Vcc 4B 11 44 2A 2B 2Y GND figure out if to A,B,C,D or D,C,B, Pin 15 Strobe = GND Pin 4, 7, 9 12 = outputs, go to LE Pin 1 Select = Clock 74LS157 on breadboard clock signal, their NOT clock to D1. Make one line Blue Logic Analyzer, put through Clock = is TTL in Clock section of take from there, you will need 5 NOT. To attach clock to D2 and connections Clock and 1 NOT Clock Load, attach both to switch. otherwise counts down. switch, Counts up when 1, Pin 10 Up/Down = attach to switch. It clears when 1. Pin 9 Reset = attach both to Pin 1 Preset Enable = Paralle CD4510BE in MSD, Carry in of MSD = in LSD, Carry in=GND, Pin 5,7 = Carry (active low Pin 6, 11, 14, 2 = outputs go or B in MUX), and one for MS for the LSD One's Digit (Right each chip to 4 switches, one Pin 4, 12, 13, 3 = inputs, atta Clock = TTL oads when 1. Carry Out of LSD Ten's Digit (Left or A in MUX MUX as shown in lab manua

Picture of Completed Circuit on Breadboard

