Carlos Gross-Martinez

CDA3201C

Logic Design Course

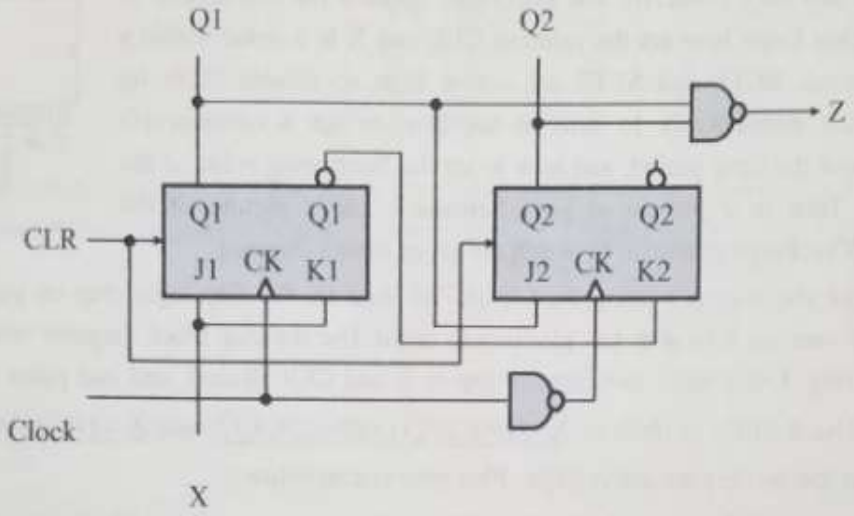
Lab 4: Tracing Master Slave and Waltz Counter

JK Flip-Flops Timing Diagram Trace

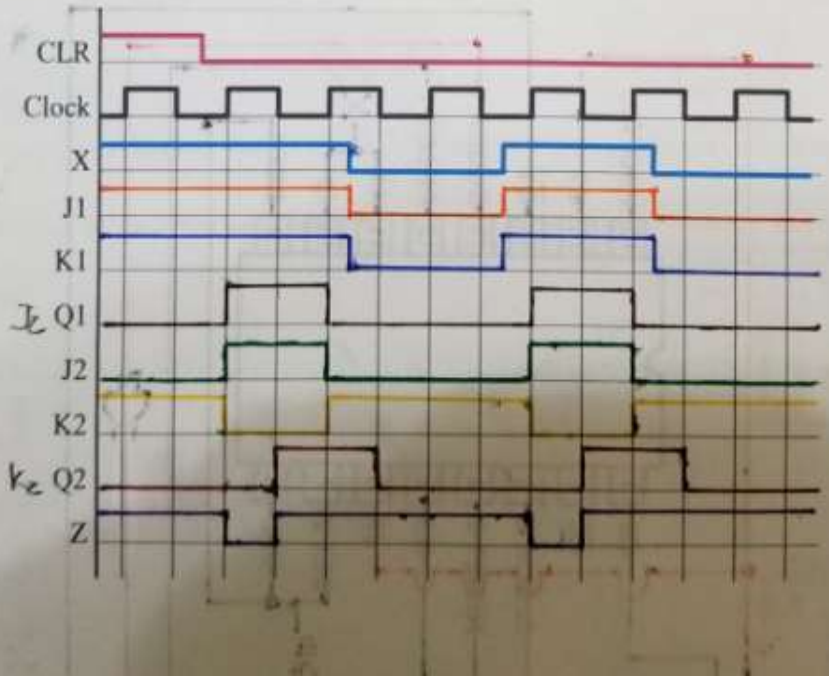
• CDA3201 • Intro to Logic Design • Lab Assignment 4

Name: Carlos Gross-Martinez Grade: /100

4) [40] Consider the following sequential circuit with two positive-edge-triggered JK flip-flops.



4.a) [4] Trace the timing diagram for the above circuit by hand.



Logic Drawing JK Flip-Flops Using Logic Chips

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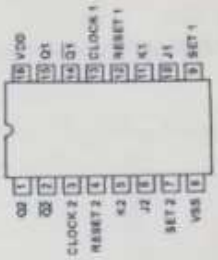
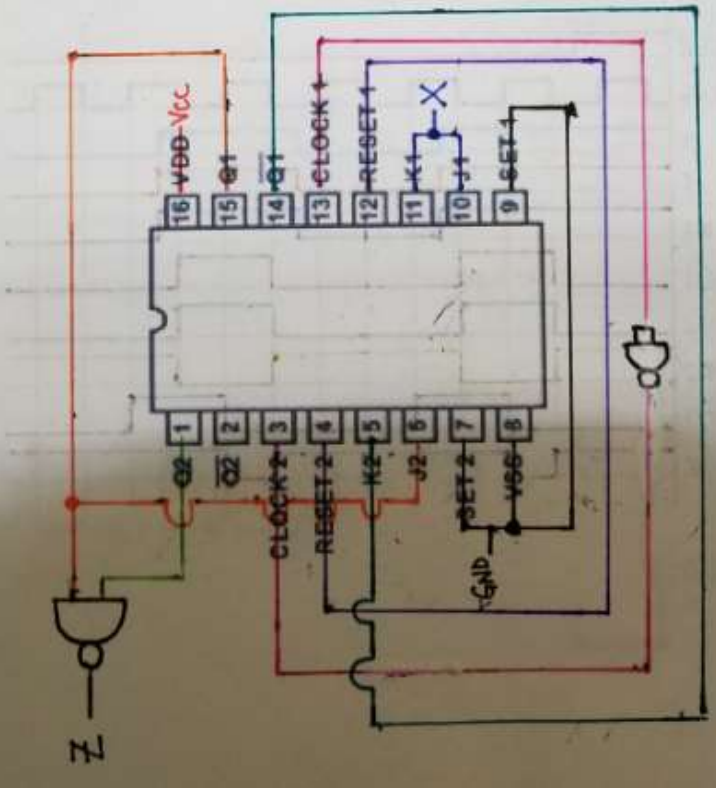


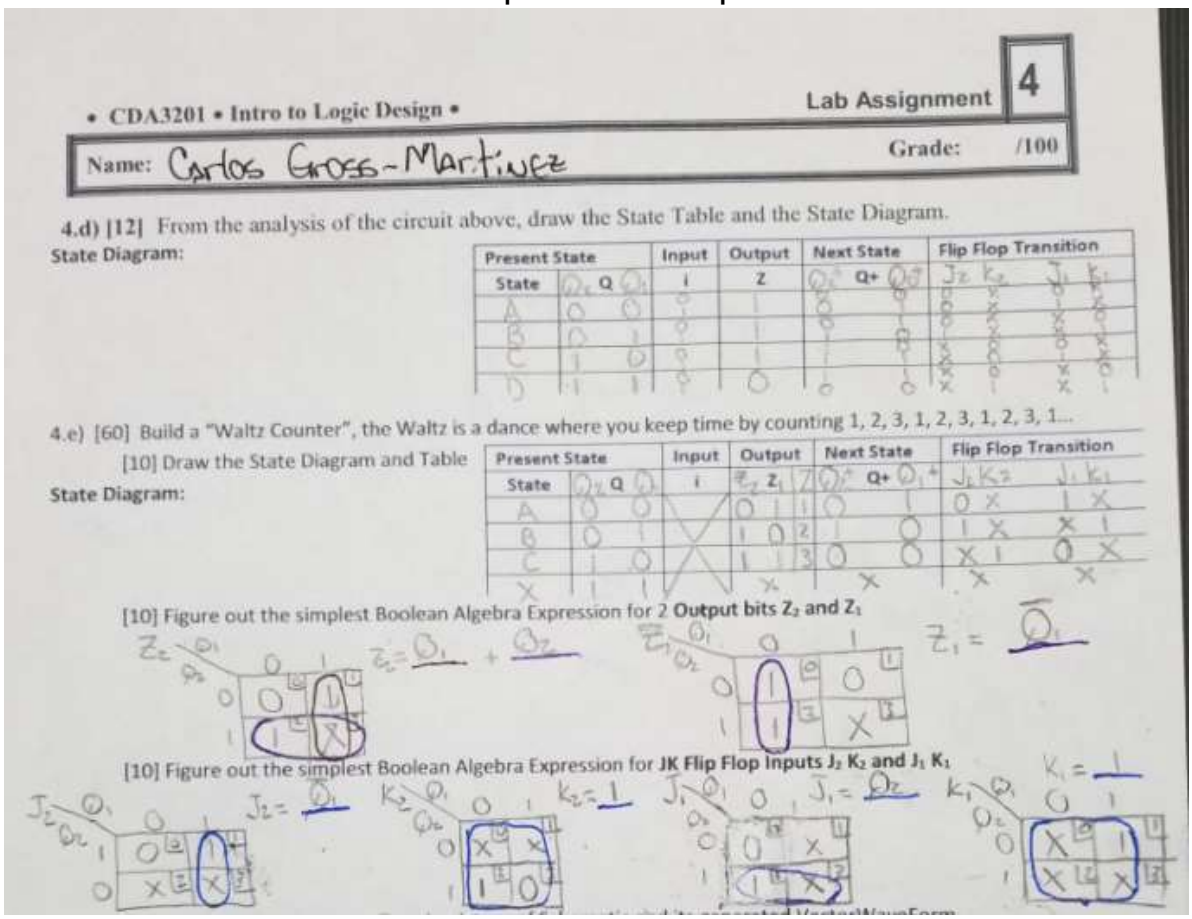
4.c) [8] Verify the circuit design/behavior by implementing the circuit using Quartus and the CD4027BE J-K Flip Flop. Review the PowerPoint in this section know how set the value of CLR and X to a value within a time period. SET1 and SET2 are active high so disable them by connecting permanently to low so see how to set a constant (0) throughout the time period, and how to set the fluctuating value of the clock. Turn in a picture of your Schematic and a picture of the VectorWaveForm generated to match the given timing diagram

4.b) [16] Build the above circuit using the CD4027BE dual JK flip-flop logic chip on your breadboard and then connect it to your test platform to test it. Use the chip block diagram below to plan for your wiring. Use 2 logic switches for inputs X and CLR (Reset), and one pulse switch for the Clock. Use 4 LEDs to observe X=J1= K1, Q1=J2=K2*, Q2, and Z=Q1*+Q2*. Tie the SET inputs to low as they are active high. Plan your circuit below.

Observation: If X is kept high, Q1 will toggle at every positive Clock transition because J1=K1=X=1 (toggle mode).



JK Flip-Flops and Waltz Counter State Diagram and Boolean expression Simplification



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4.d) [12] From the analysis of the circuit above, draw the State Table and the State Diagram.

State Diagram:

Present State		Input	Output	Next State	Flip Flop Transition	
State	Q_2 Q Q_1	i	Z	Q_2^+ Q+ Q_1^+	J_2 K_2	J_1 K_1
A	0 0	0	1	0 0	0 X	0 X
B	0 1	0	1	0 1	0 X	X 0
C	1 0	0	1	1 0	X 0	0 X
D	1 1	0	0	0 0	X 1	X 1

4.e) [60] Build a "Waltz Counter", the Waltz is a dance where you keep time by counting 1, 2, 3, 1, 2, 3, 1, 2, 3, 1...

[10] Draw the State Diagram and Table

State Diagram:

Present State		Input	Output	Next State	Flip Flop Transition	
State	Q_2 Q Q_1	i	Z_2 Z_1	Q_2^+ Q+ Q_1^+	J_2 K_2	J_1 K_1
A	0 0		0 1	0 1	0 X	1 X
B	0 1		1 0	1 0	1 X	X 1
C	1 0		1 1	0 0	X 1	0 X
X	1 1	X	X	X	X	X

[10] Figure out the simplest Boolean Algebra Expression for 2 **Output bits Z_2 and Z_1**

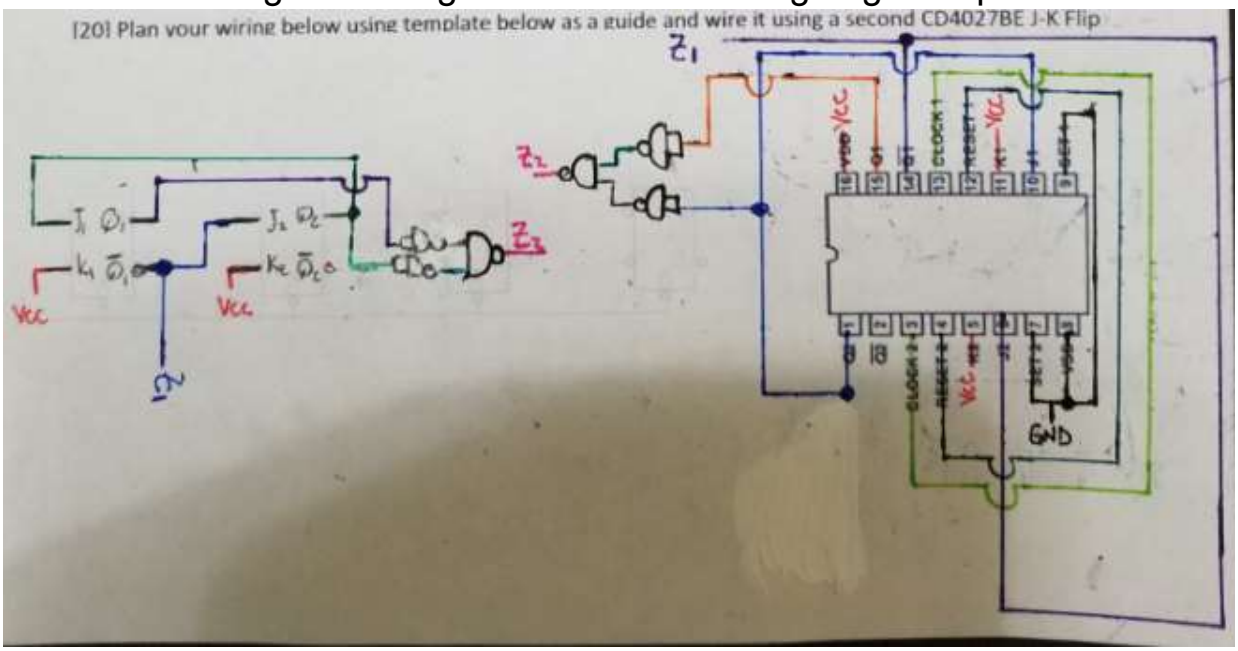
$Z_2 = Q_1 + Q_2$

$Z_1 = \overline{Q_1}$

[10] Figure out the simplest Boolean Algebra Expression for **JK Flip Flop Inputs J_2 K_2 and J_1 K_1**

$J_2 = Q_1$ $K_2 = 1$ $J_1 = Q_2$ $K_1 = 1$

Logic Drawing Waltz Counter Using Logic Chips



[20] Plan your wiring below using template below as a guide and wire it using a second CD4027BE J-K Flip

Z_1

Z_2

J_1 Q_1

J_2 Q_2

K_1 $\overline{Q_1}$

K_2 $\overline{Q_2}$

Z_3

Vcc

Vcc

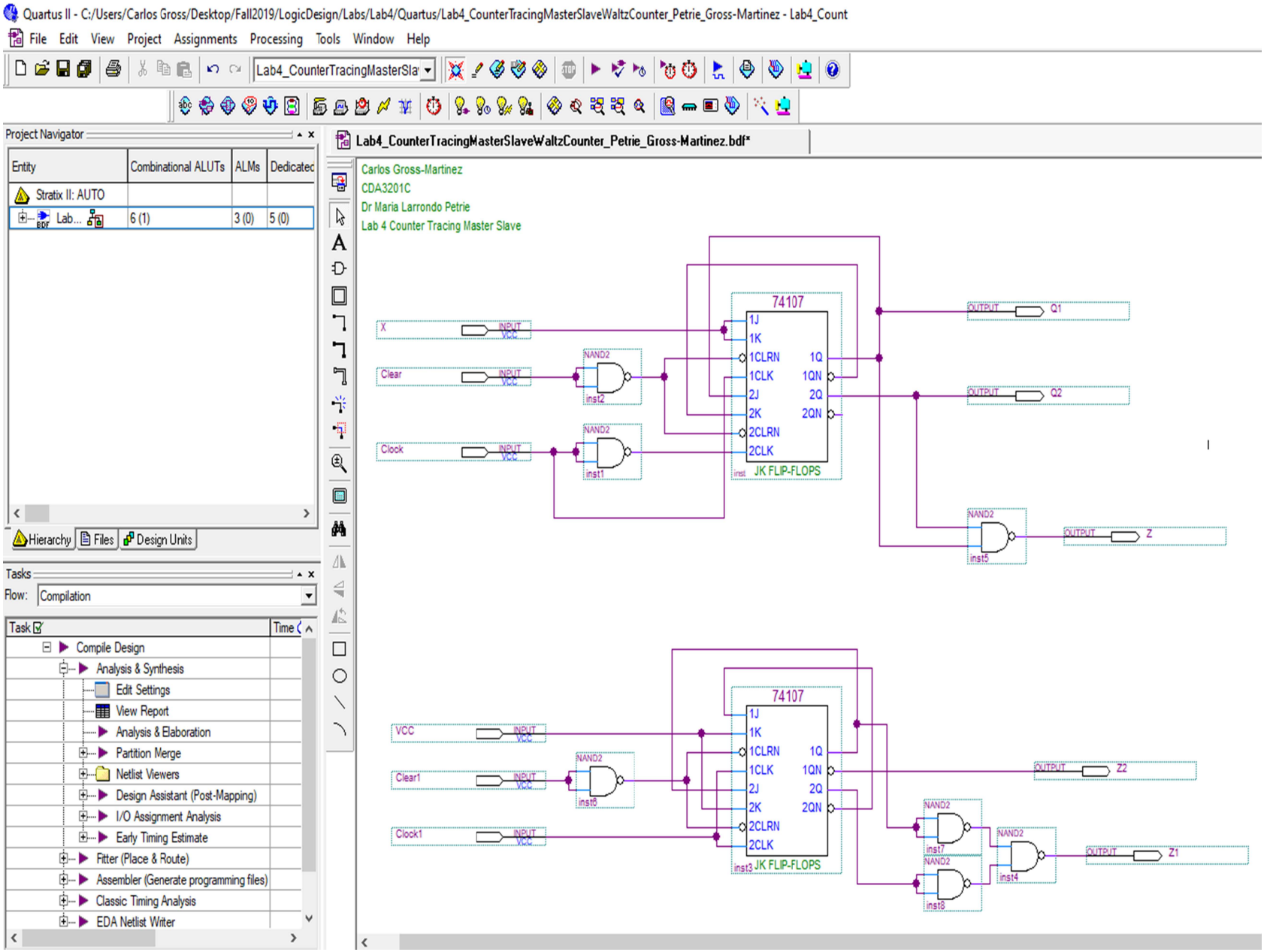
$\overline{Q_2}$

Vcc

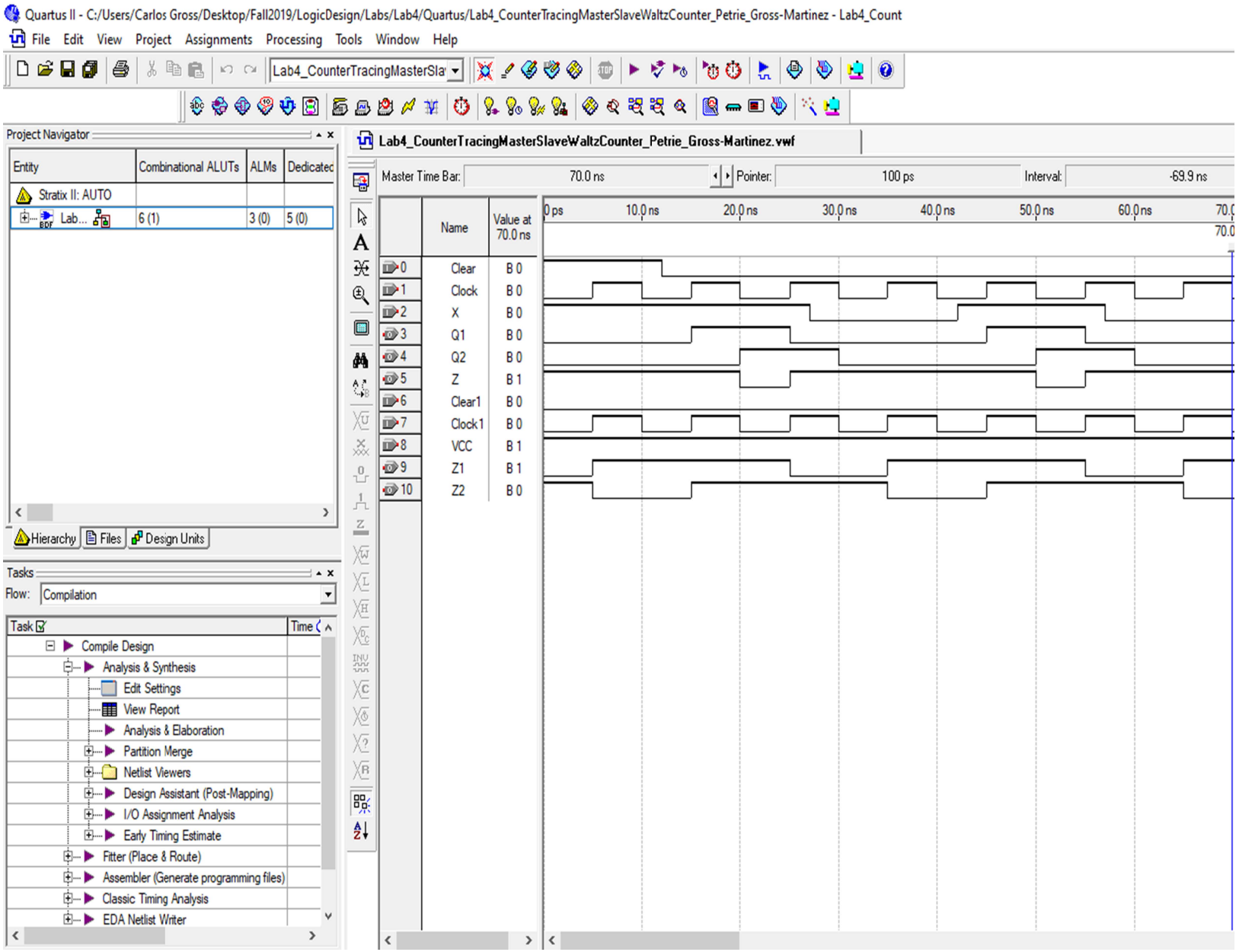
Vcc

GND

Quartus Schematic JK Flip-Flops and Waltz Counter



Quartus Waveform Compilation Result
JK Flip-Flops and Waltz Counter



Picture of Completed Circuit on Breadboard