Carlos Gross-Martinez

CDA3201C

Logic Design Course

Lab 1 – First circuit wiring design

Truth Table:

0) [5] This lab experiment is used for the lab orientation where TAs will walk you through practical steps to build the experiment circuit and test it. You will use the following simple function:

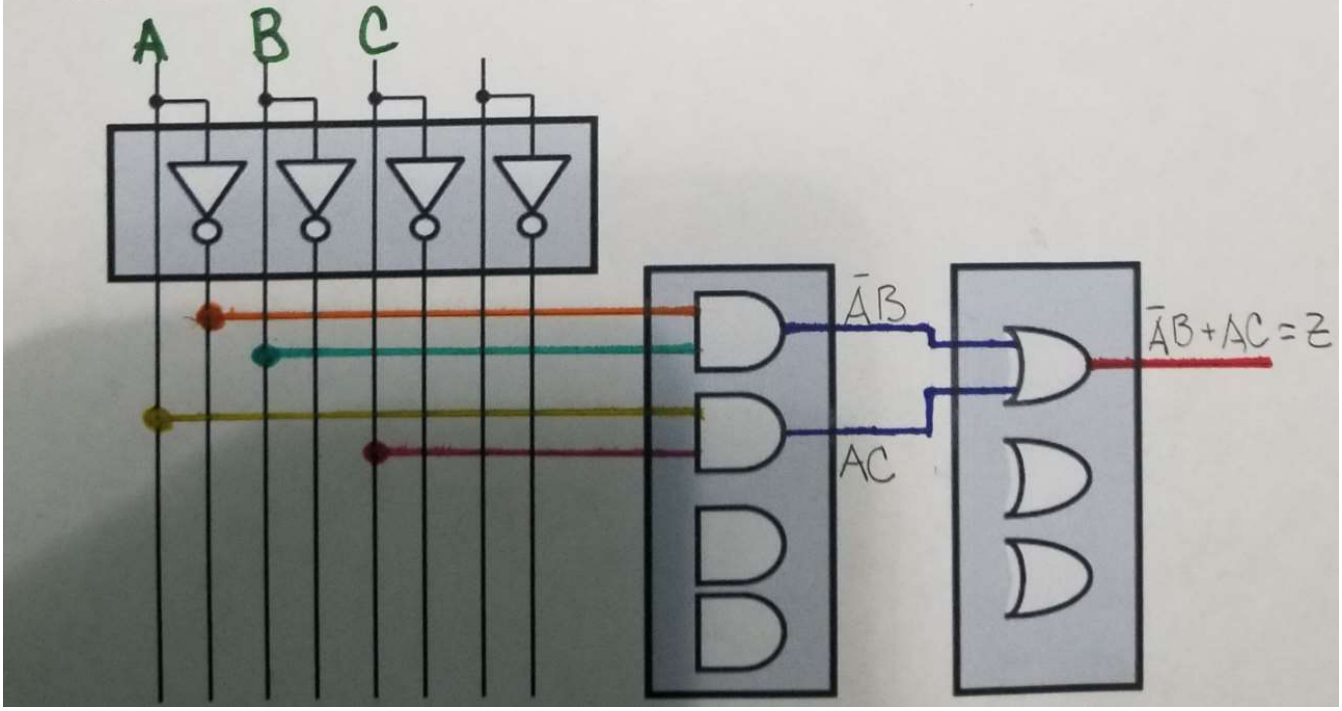
$$Z = A' B + A C$$

0.a) [0] Fill the truth table for the above function

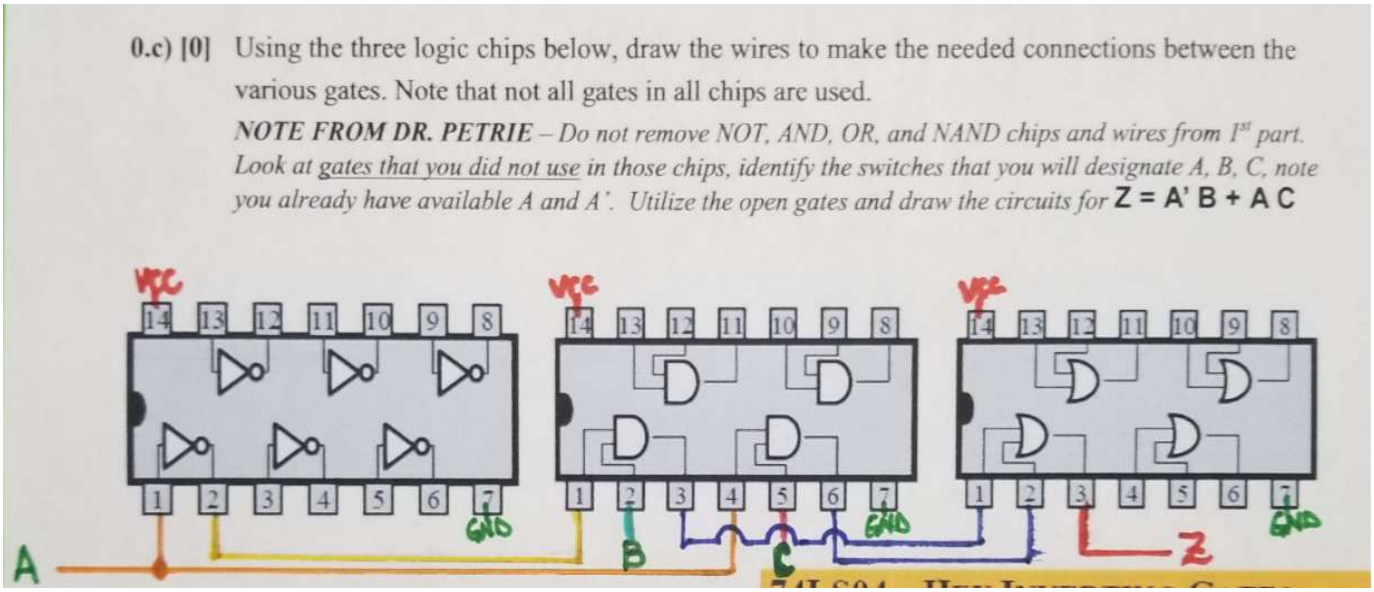
A B C	A' B	A C	Z
000	0	0	0
001	0	0	0
010	1	0	1
011	1	0	1
100	0	0	0
101	0	1	1
110	0	0	0
111	0	1	1

Logic Drawing (Z = A'B + AC)

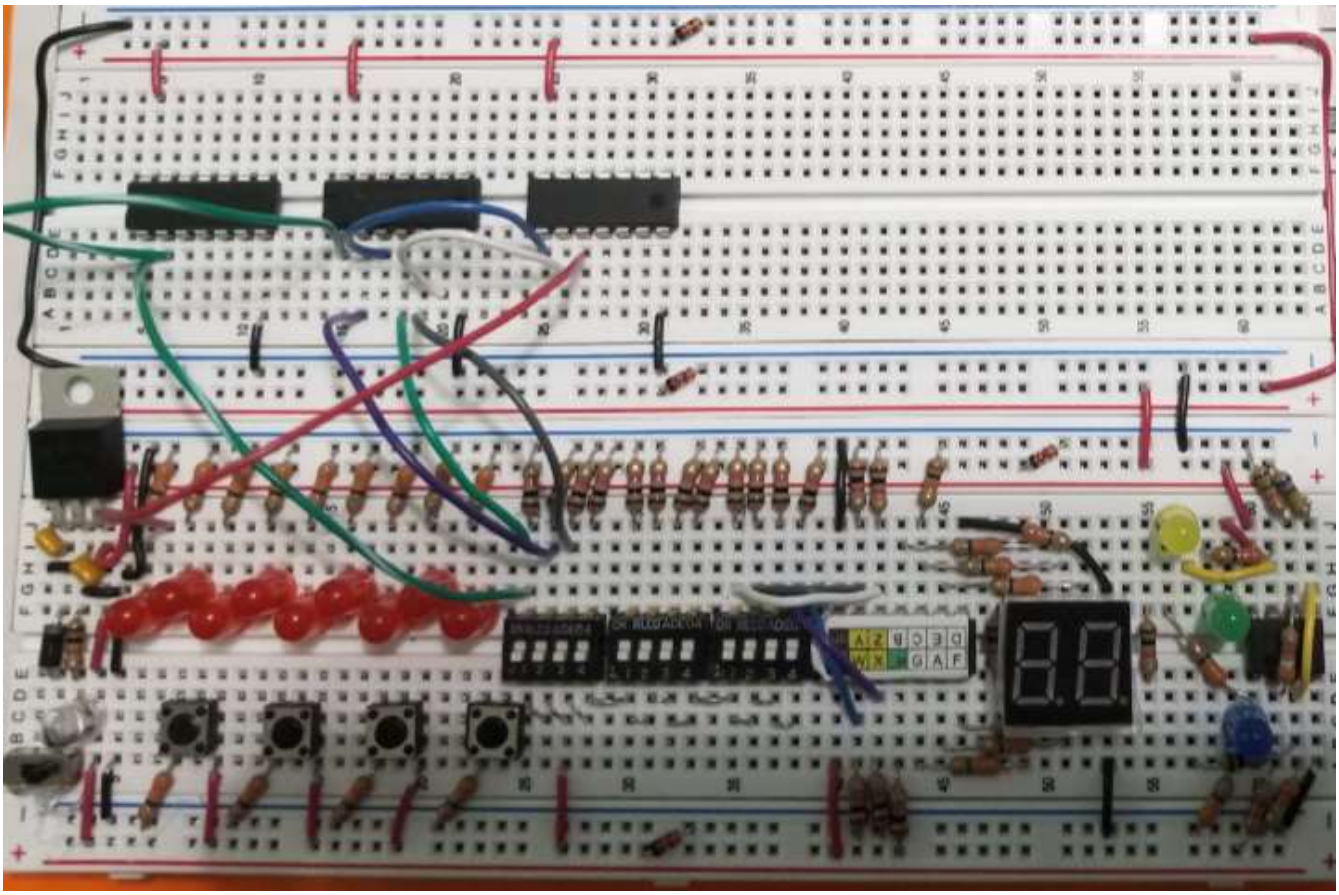
0.b) [0] Draw the switching function (**Z = A' B + A C**) using Inverters, AND gates, and OR gate:



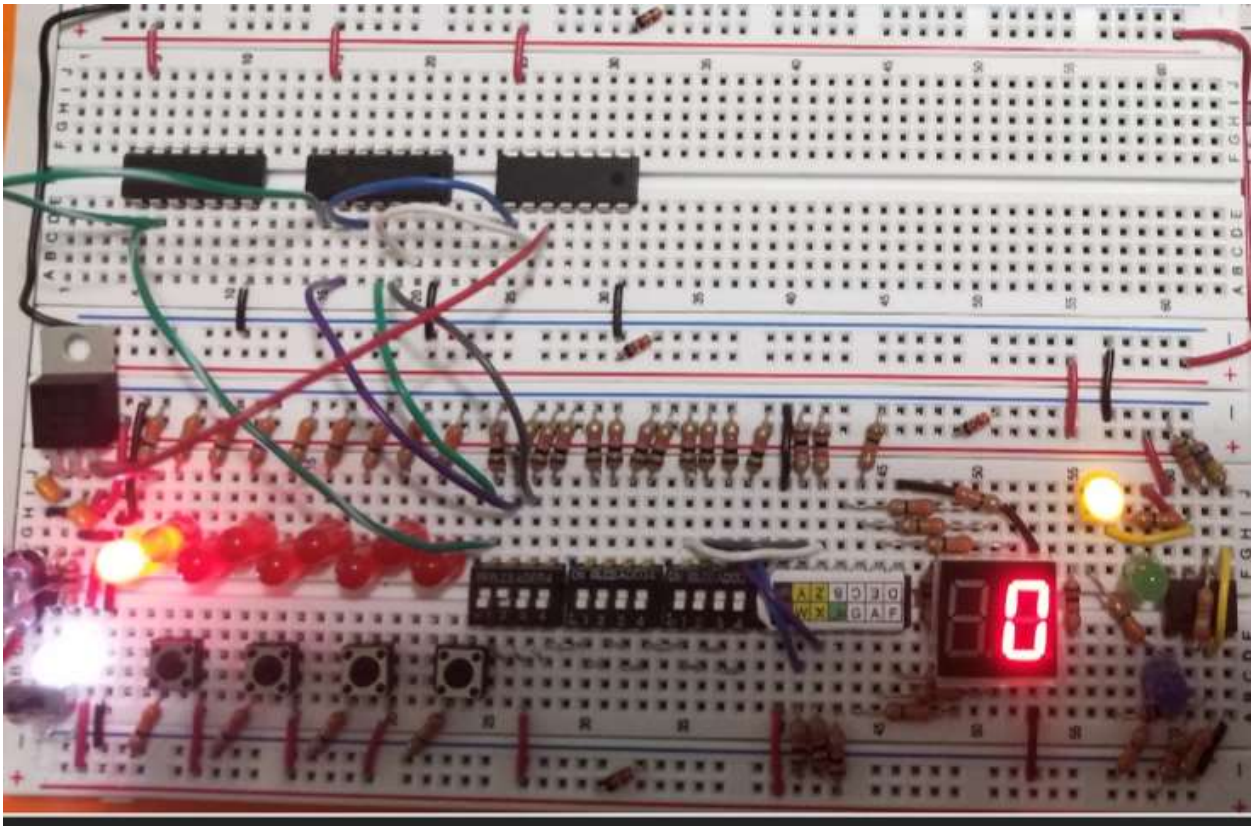
Drawing Using Logic Chips (Z = A'B + AC)

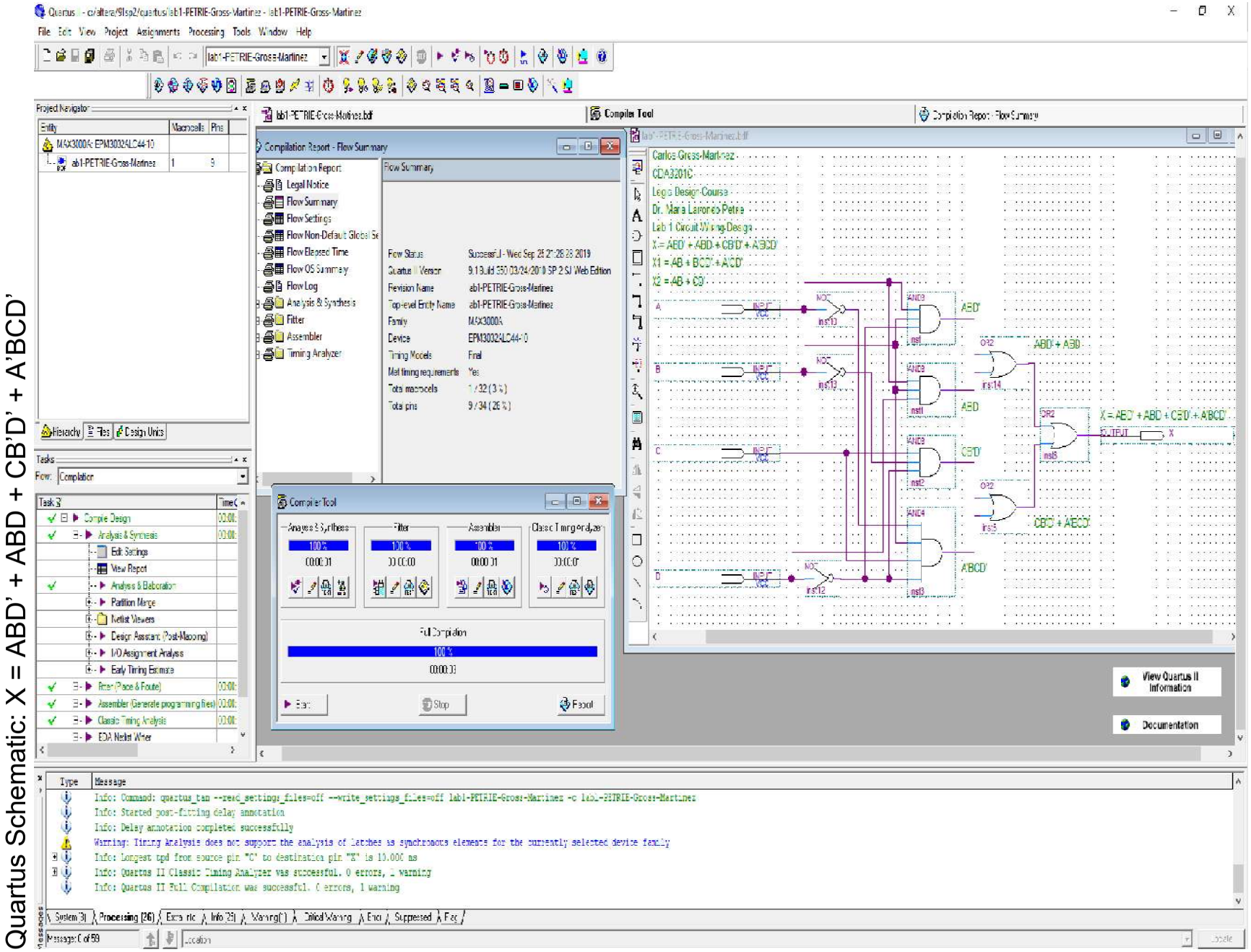


Picture of Completed Circuit on breadboard



Picture of Completed Circuit on breadboard Working




Quartus Schematic: X = ABD' + ABD + CB'D' + A'BCD'
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Macrocells
Pins
Compilation Report - Flow Summary
Flow Summary
Legal Notice
Flow Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Flow Status
Successful - Wed Sep 25 21:26:28 2019
Quartus II Version
Revision Name
lab1-PETRIE-Gross-Martinez
Top-level Entity Name
lab1-PETRIE-Gross-Martinez
Family
MAX3000A
Device
EPM3032ALC44-10
Timing Models
Final
Met timing requirements
Yes
Total macrocells
1 / 32 (3 %)
Total pins
9 / 34 (26 %)
Compiler Tool
Analysis & Synthesis
Fitter
Assembler
Classic Timing Analyzer
Full Compilation
Start
Stop
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Dr. Maria Larrondo Petrie
Lab 1 Circuit Wiring Design
X = ABD' + ABD + CB'D' + A'BCD'
X1 = AB + BCD' + A'CD'
X2 = AB + CD
A
B
C
D
AND3
AND4
OR2
OR4
ABD' + A'BD
A'BD
CB'D'
A'BCD'
X = ABD' + ABD + CB'D' + A'BCD'
OUTPUT
View Quartus II Information
Documentation
Type
Message
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off lab1-PETRIE-Gross-Martinez -c lab1-PETRIE-Gross-Martinez
Info: Started post-fitting delay annotation
Info: Delay annotation completed successfully
Warning: Timing Analysis does not support the analysis of latches as synchronous elements for the currently selected device family
Info: Longest tpd from source pin "C" to destination pin "X" is 10.000 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 1 warning

Quartus Waveform