

Assignment – 2

Full adder Verilog code ,Testbench along with Screenshot?

// Verilog Code

```
module full_adder (  
    input wire a,  
    input wire b,  
    input wire cin,  
    output wire sum,  
    output wire cout);  
    assign sum = a ^ b ^ cin;  
    assign cout = (a & b) | (b & cin) | (a & cin);  
endmodule
```

//Testbench

```
`timescale 1ns / 1ps  
module tb_full_adder;  
    reg a, b, cin;  
    wire sum, cout;  
    full_adder uut (  
        .a(a),  
        .b(b),  
        .cin(cin),  
        .sum(sum),  
        .cout(cout));  
    initial begin  
        $dumpfile("full_adder.vcd");  
        $dumpvars(0, tb_full_adder);
```

end

initial begin

a = 0; b = 0; cin = 0; #10;

a = 0; b = 0; cin = 1; #10;

a = 0; b = 1; cin = 0; #10;

a = 0; b = 1; cin = 1; #10;

a = 1; b = 0; cin = 0; #10;

a = 1; b = 0; cin = 1; #10;

a = 1; b = 1; cin = 0; #10;

a = 1; b = 1; cin = 1; #10;

end

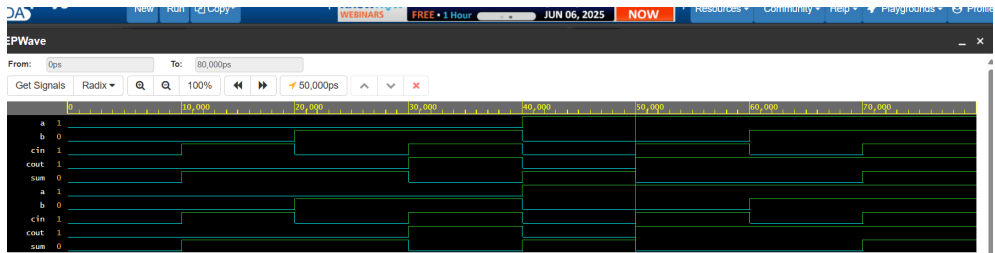
endmodule

The screenshot shows the EDA Playground web interface. The top navigation bar includes 'playground', 'New', 'Run', 'Copy', and a 'KnowHow' banner for 'Essential SystemVerilog Assertions (Reading, UK)' with a 'FIND OUT MORE' button. The left sidebar contains links for 'Help to you by OULOS', 'Languages & Libraries', 'Tools & Simulators' (set to 'Verilog 12.0'), 'File Options' (set to 'g2012'), 'Options', 'Run' (with a 'run.bash' script), 'Examples', and 'Log/EDA Playground'. The main editor area has two tabs: 'testbench.sv' and 'design.sv'. The 'testbench.sv' tab is active, showing a Verilog testbench for a full adder. The 'design.sv' tab shows the full adder module code. The bottom status bar displays a log of events, including a warning about missing time units and the opening of the EPWave viewer.

```
module tb_full_adder;
  reg a, b, cin;
  wire sum, cout;
  full_adder uut (
    .a(a),
    .b(b),
    .cin(cin),
    .sum(sum),
    .cout(cout)
  );
  initial begin
    $dumpfile("full_adder.vcd");
    $dumpvars(0, tb_full_adder);
  end
  initial begin
    a = 0; b = 0; cin = 0; #10;
    a = 0; b = 0; cin = 1; #10;
    a = 0; b = 1; cin = 0; #10;
    a = 0; b = 1; cin = 1; #10;
    a = 1; b = 0; cin = 0; #10;
    a = 1; b = 0; cin = 1; #10;
    a = 1; b = 1; cin = 0; #10;
    a = 1; b = 1; cin = 1; #10;
  end
endmodule
```

```
// Code your design here
module full_adder (
  input wire a,
  input wire b,
  input wire cin,
  output wire sum,
  output wire cout;
);
  assign sum = a ^ b ^ cin;
  assign cout = (a & b) | (b & cin) | (a & cin);
endmodule
```

Log: [2025-05-31 16:58:29 UTC] iverilog "-wall" "-g2012" design.sv testbench.sv && unbuffer vvp a.out
warning: Some design elements have no explicit time unit and/or
: time precision. This may cause confusing timing results.
: Affected design elements are:
: -- module full_adder declared here: design.sv:2
VCD info: dumpfile full_adder.vcd opened for output.
Finding VCD file...
./full_adder.vcd
[2025-05-31 16:58:29 UTC] Opening EPWave...



Note: To revert to EPWave opening in a new browser window, set that option on your profile page.