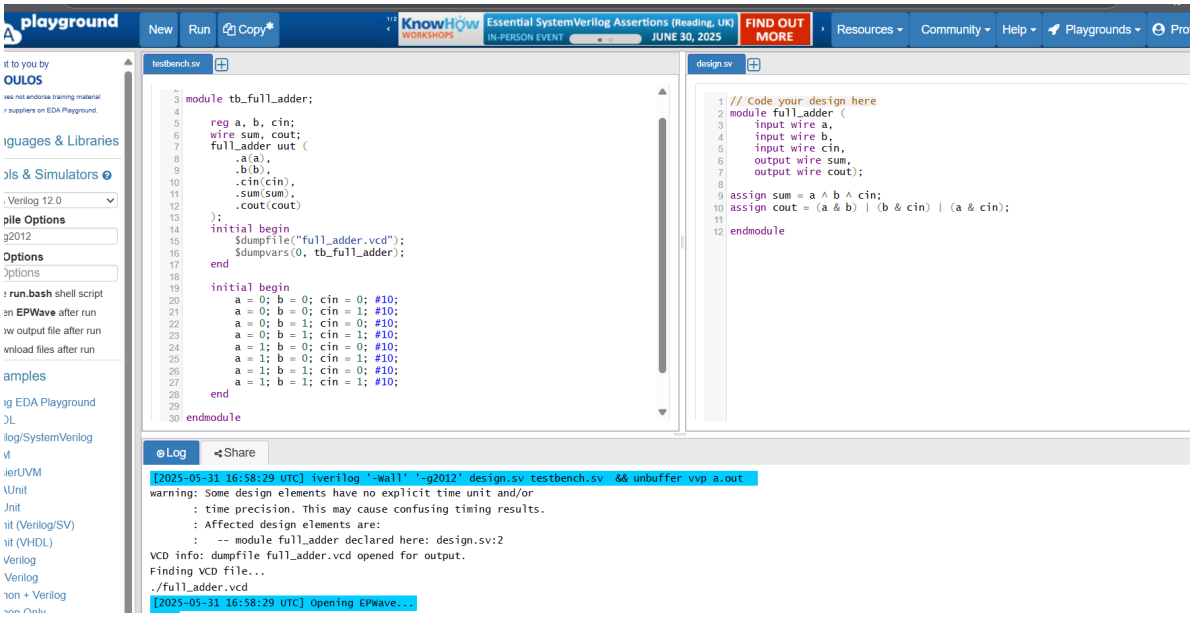
Assignment – 2

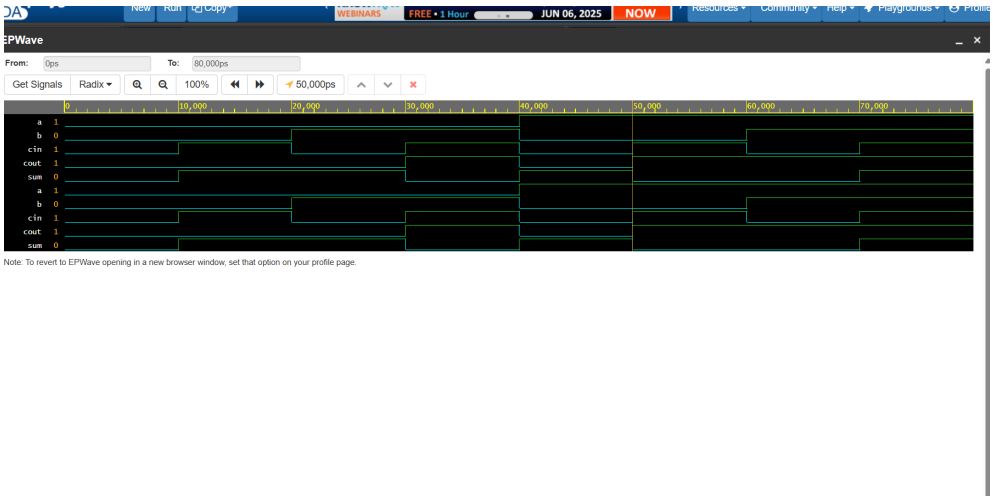
Full adder Verilog code ,Testbench along with Screenshot?

```
// Verilog Code
module full_adder (
    input wire a,
    input wire b,
    input wire cin,
    output wire sum,
    output wire cout);
assign sum = a ^ b ^ cin;
assign cout = (a & b) | (b & cin) | (a & cin);
endmodule

//Testbench
`timescale 1ns / 1ps
module tb_full_adder;
    reg a, b, cin;
    wire sum, cout;
    full_adder uut (
        .a(a),
        .b(b),
        .cin(cin),
        .sum(sum),
        .cout(cout));
    initial begin
        $dumpfile("full_adder.vcd");
        $dumpvars(0, tb_full_adder);
```

```
    end
    initial begin
        a = 0; b = 0; cin = 0; #10;
        a = 0; b = 0; cin = 1; #10;
        a = 0; b = 1; cin = 0; #10;
        a = 0; b = 1; cin = 1; #10;
        a = 1; b = 0; cin = 0; #10;
        a = 1; b = 0; cin = 1; #10;
        a = 1; b = 1; cin = 0; #10;
        a = 1; b = 1; cin = 1; #10;
    end
endmodule
```





Note: To revert to EPWave opening in a new browser window, set that option on your profile page.