**Assignment – 2**

Full adder Verilog code ,Testbench along with Screenshot?

// Verilog Code

module full\_adder (

input wire a,

input wire b,

input wire cin,

output wire sum,

output wire cout);

assign sum = a ^ b ^ cin;

assign cout = (a & b) | (b & cin) | (a & cin);

endmodule

//Testbench

`timescale 1ns / 1ps

module tb\_full\_adder;

reg a, b, cin;

wire sum, cout;

full\_adder uut (

.a(a),

.b(b),

.cin(cin),

.sum(sum),

.cout(cout));

initial begin

$dumpfile("full\_adder.vcd");

$dumpvars(0, tb\_full\_adder);

end

initial begin

a = 0; b = 0; cin = 0; #10;

a = 0; b = 0; cin = 1; #10;

a = 0; b = 1; cin = 0; #10;

a = 0; b = 1; cin = 1; #10;

a = 1; b = 0; cin = 0; #10;

a = 1; b = 0; cin = 1; #10;

a = 1; b = 1; cin = 0; #10;

a = 1; b = 1; cin = 1; #10;

end

endmodule



