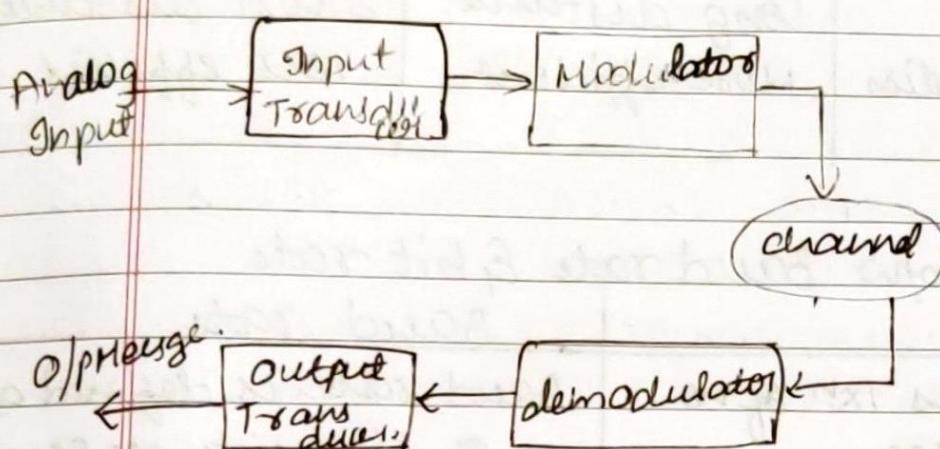


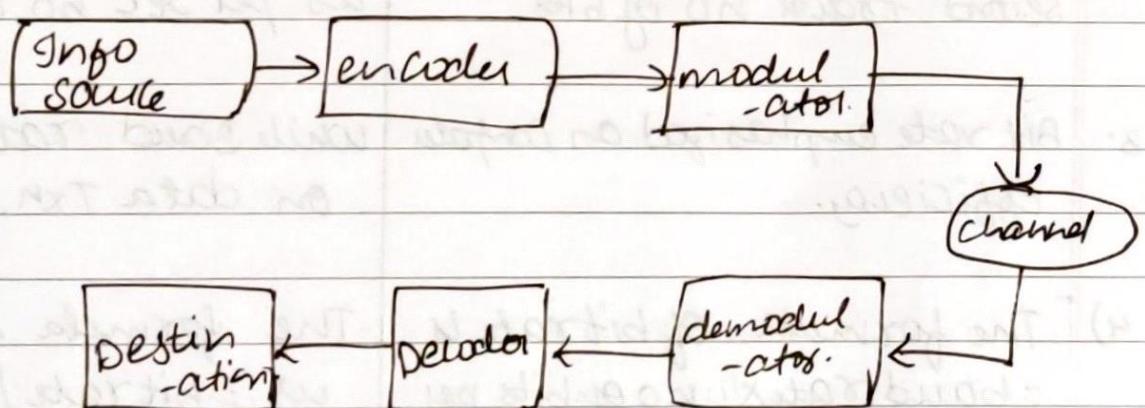
Assignment-2.

1. List the d/f b/w analog & digital communication

	Analog communication	Digital communication
parameters		
Def'n	Analog commun is a technology which uses analog sig for the Txn of info.	It is technology which uses digital sig for txn of info.
noise & distortion	Get affected by noise	Immune from noise & distortion
error probability	Error probability is high due to parallax	Error probability is low.
Hardware	It is complicated & less flexible than digital sm.	It is flexible & less complicated than analog
cost	low cost	High cost
power requirement	High power is required	Low power is required
portability	less portable as components are heavy	more portable due to compact equipment
Modulation used	Amplitude & angle modulation	PCM, DPCM etc.
Signal values	consist of continuous values	consist of discrete values
ex of signal	Analog sig comprises of voice sound etc.	Digital sig are used in computers.



Analog communication s/m



Digital communication s/m.

2) List the d/f b/w serial & parallel comm.

Basis for comparison

	serial communication	parallel communication
1) Data tx'n Speed	slow	comparatively fast
2) No of comm'n links used	single	multiple
3) No of Tx bit/clockcycle	only one bit	n no of link will carry n bits
4) Cost	low	high
5) Crosstalk	Not present	Present
6) S/m up-gradation	easy	quite difficult
7) Mode of tx'n	full duplex	Half duplex.

Suitable for
high freq operation

long distance
more efficient

short distance
less efficient

3. List the d/f b/w Band rate & bit rate.

Bit rate

Band rate

1. It is defined as Txn of no of bits per sec

Band rate is defined as no of S/g units per sec

2) Bit rate is also defined as per second travel no of bits

Band rate is also defined as per sec no of change

3. Bit rate emphasized on computer efficiency.

while Band rate emphasize on data Txn.

4) The formula of bit rate is
= band rate \times no of bits per sec

The formula for band rate
is = bit rate / the no of bit per baud.

5) Bit rate is not used to decide requirement of bandwidth of Txn of S/g

while band rate is used to decide the requirement of bandwidth for Txn S/g

5. what is RS232? with neat diagram explain RS232 D89 pins & its Handshaking process with modem

In RS232, 'RS' stands for Recommended Standard it defines the serial commn using DTE & DCE sig. Handshaking involves 4 steps.

- The Data terminal equipment (DTE) puts RTS line into "On" state
- The Data commn equipment (DCE) puts the CTS line into "On" state
- The DTE puts the DTR into the "On" state
- The DTR line remains "On" state while data being transmitted.

After the Txn of data is completed, the DTE puts DTE & RTS lines into "Off" state & DCE puts CTS line into "Off" state.

With RS232 handshaking, RS232 communications only will take place when both ends of RS232 link are ready. Thus RS232 handshake process enables DTE to request control of communications link from a related modem and allows modems to inform the terminal equipment that the control has been acquired.

6. What are DTE & DCE equipments. Give examples

Data Terminal Equipment is an end instrument that converts user information into sig or reconstructs received sig. These can also be called tail cts. A DTE device communicates with data circuit-terminating equipment (DCE).

DCE - element - The Data circuit element terminating equipment is a device that sits b/w the data terminal equipment & data Txn CKT. It is also called data communication equipment &

data carrier equipment. usually the DTE device is terminal & DCE is a modem.

A modem is most common kind of DCE. Other common examples are ISDN adapters, satellites, microwave stations, base stations & network interface cards.

7. If Baud rate is 9600, how much time is required to transmit single bit

$$\text{Bit time} = \text{no of bit} / \text{baud rate}$$

$$\text{Baud rate} = 9600$$

$$1/9600 = 1.0417 \times 10^{-5} \text{ ms}$$

8. What is SPI? List its features. Also differentiate

Serial Peripheral Interface is a interface bus commonly used to send data b/w microcontrollers & small peripherals such as shift registers, sensors, SD cards. It uses separate clock & data lines, along with a select line to choose the device you wish to talk to.

SPI applications

1. SD card module
2. RFID card reader module
3. Wireless Transmitter/receiver.

features

unique benefit of SPI is fact that data can be transferred without interruption. Any no of bits can be sent or received in a continuous stream.

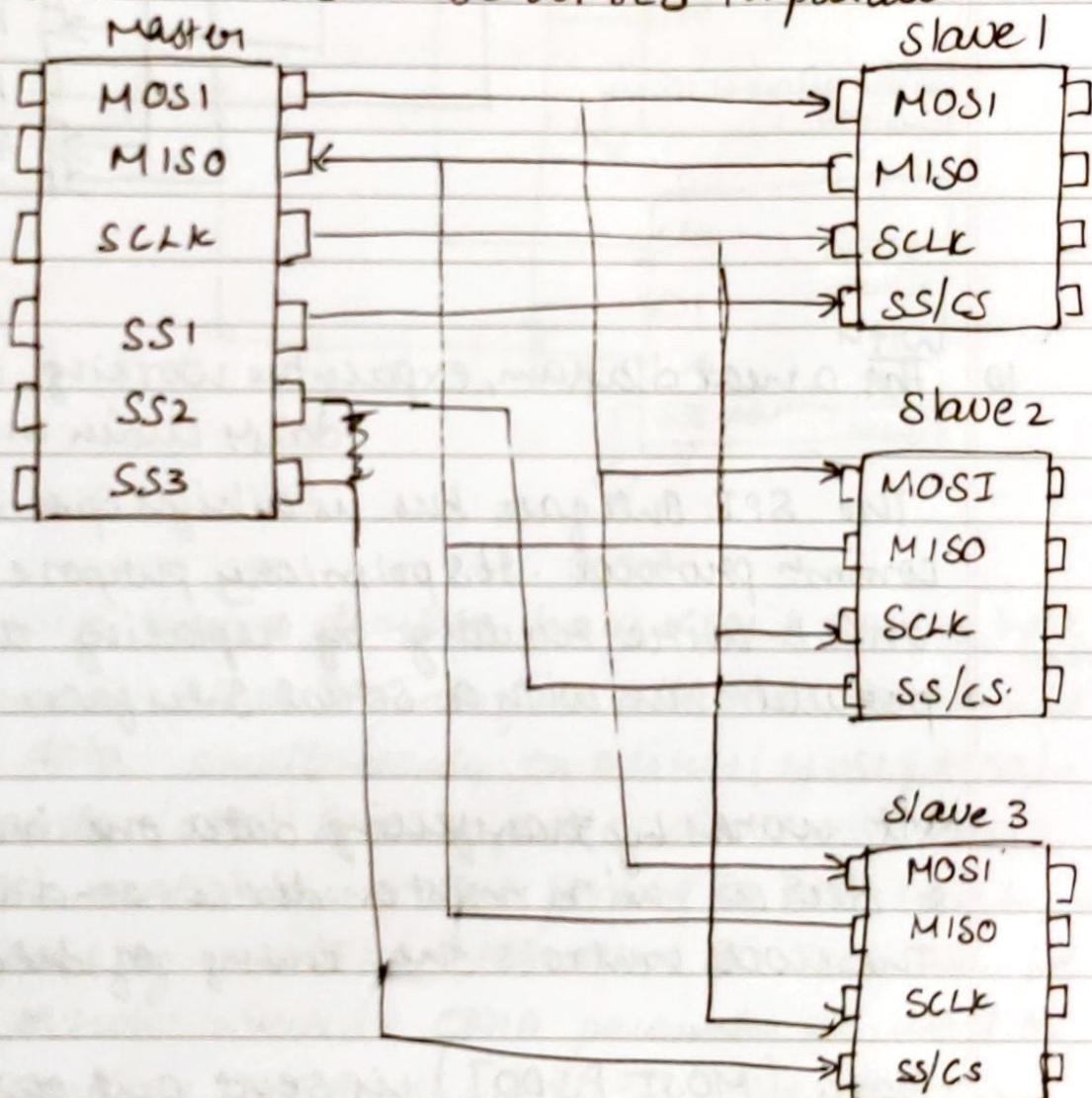
With I2C & UART, data is sent in packets, limited to a specific no. of bits. Start & stop conditions define beginning & end of each packet, so data is interrupted during Txn.

Devices communicating via SPI are in master-slave relationship. The Master is the controlling device (usually a microcontroller), while the slave (usually a sensor, display, or memory chip) takes instruction from the Master. The simplest configuration of

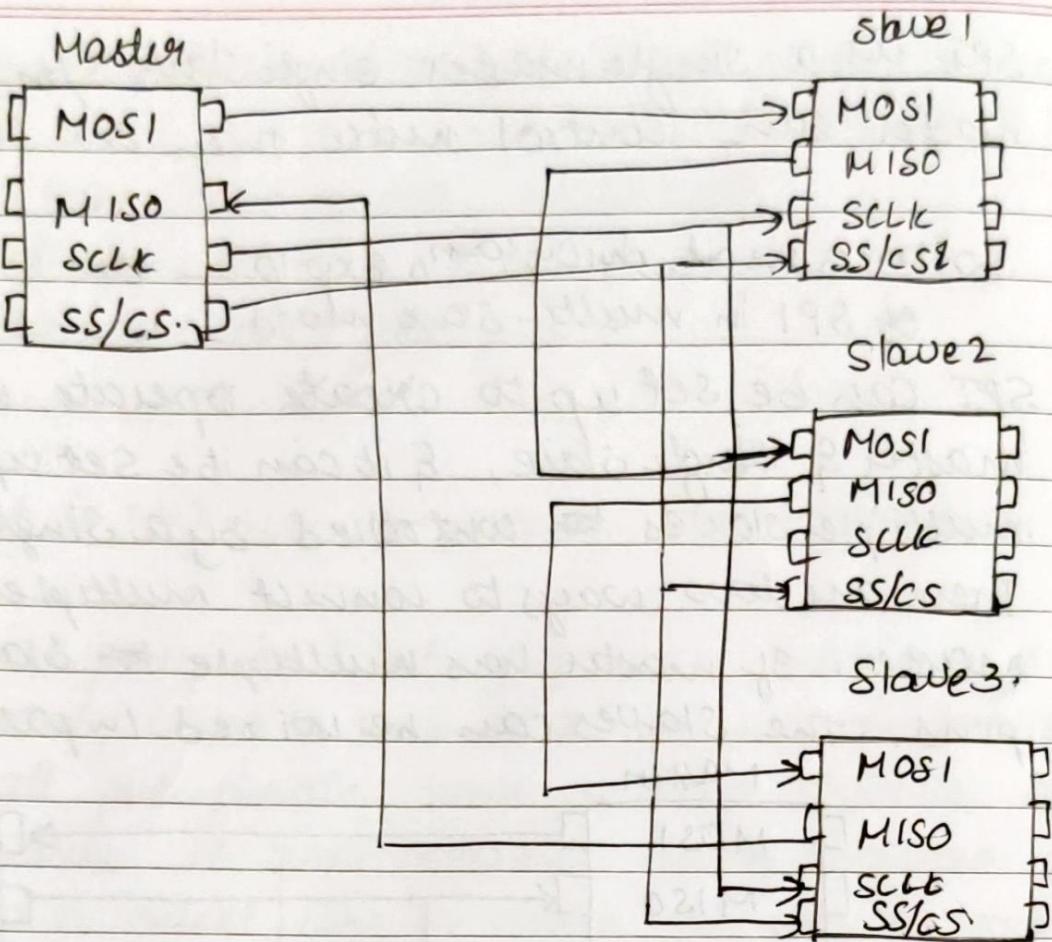
SPI is a single master single slave S/m, but no master can control more than one slave.

- Q. With a neat diagram, explain the working of SPI in multi-slave mode

SPI can be set up to operate with a single master & single slave, & it can be set up with multiple slaves to be controlled by a single master. There are two ways to connect multiple slaves to master. If master has multiple SS pins, the slaves can be wired in parallel like this



If only one slave select pin is available, the slaves can be daisy-chained like this



10. ^{With} ~~The~~ a neat diagram, explain the working of SPI in daisy chain mode.

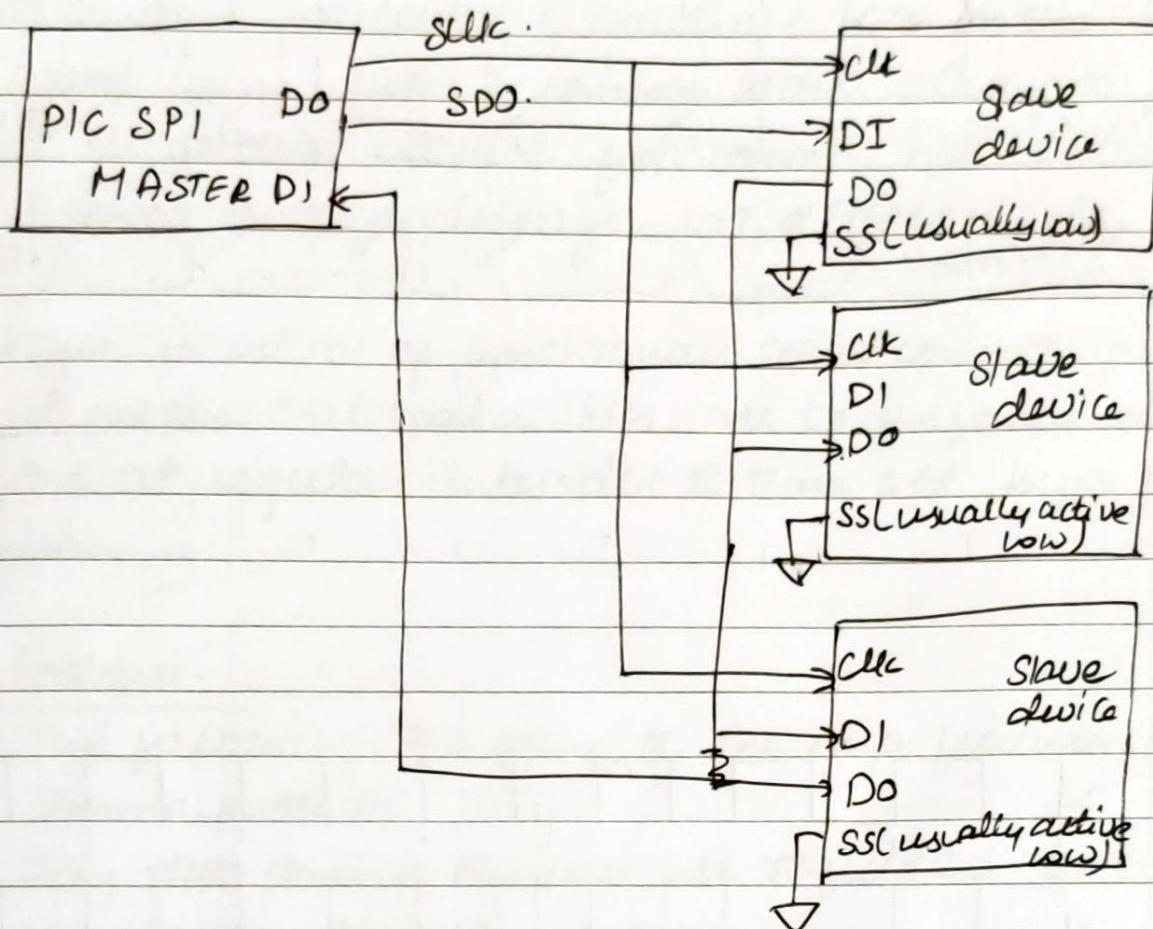
The SPI interface bus is a high speed, 3 wire, serial communication protocol. Its primary purpose is to reduce on PCB wire routing by replacing the traditional parallel bus with a serial interface.

It works by transferring data one bit at a time b/w 2 devices with master device sending CLK sig. The clock controls the timing of data transfer.

Data (MOSI [SDO]) is sent out of shift register in master SPI device along with a clock sig (SCLK) while at the same time another shift register receives data from the slave (MISO [SDI]). The Master is always in a control & initiates data transfer using CLK sig. Slave devices are selected using a separate slave select sig i.e.

S/W controlled i.e those sig are separate from SPI Hardware module.

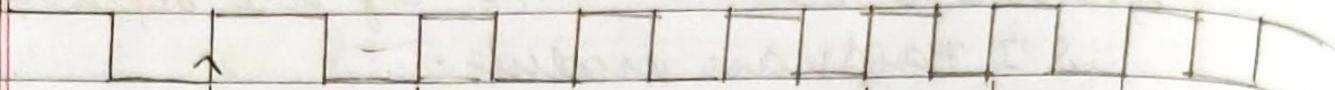
SPI with daisy chain.



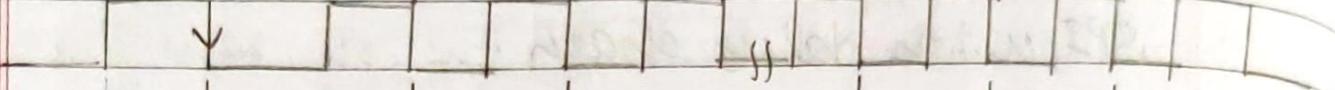
11. Explain with timing diagram, how CPOL & CPhase help in SPI
- The purpose is - The SPI interface allows to transmit & receive data simultaneously on 2 lines (MOSI & MISO). clock polarity (CPOL) & clock phase are the main parameters that define clock format to be used by SPI bus. Depending on CPOL parameter . SPI clock may be Inverted or non inverted. CPHA parameter is used to shift sampling phase. if CPHA=0 the data are sampled on leading clock edge.

In SPI the master can select the clock polarity & clock phase. The CPOL bit sets polarity of clock sig during idle state. The idle state defined as period when CS is high & transitioning to low at start of Txn & when CS is low & transitioning to high at end of Txn

CPOL=1



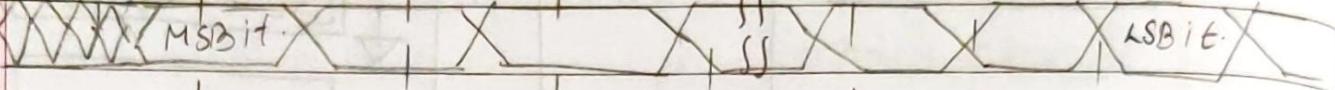
CPOL=0.



MOSI

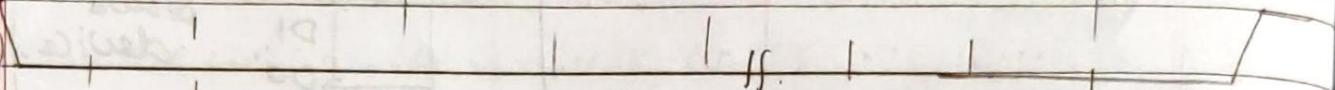


MISO



NSS

(to slave)

Capture
Strobe

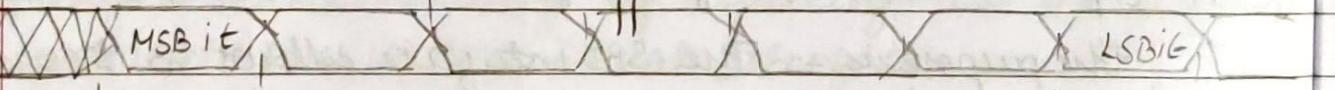
CPOL=1



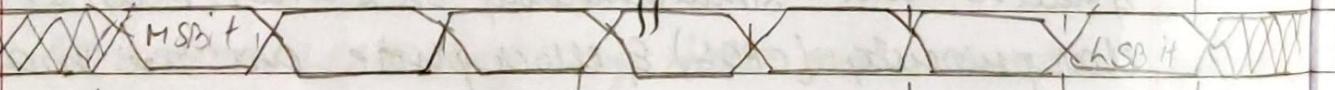
CPOL=0.



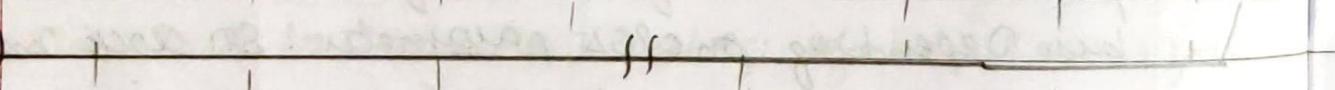
MOSI



MISO



NSS(to slave)

Capture
Strobe

12. Explain I²C Protocol & its features

I²C communication is the short form for inter-integrated circuits. It is a common protocol developed by Philips Semiconductors for the transfer of data b/w a central processor & multiple IC's on the same PCB board using just 2 common wires. Owing to simplicity, it is widely adopted for common b/w microcontrollers & sensor arrays, displays, IoT, EEPROM etc.

* This is a type of synchronous serial communication protocol. It means that data bits are transferred one by one at regular intervals of time set by a ref clock line.

features.

The following are some of the imp features of I²C communication protocol-

only two common bus lines are required to control any device on I²C network.

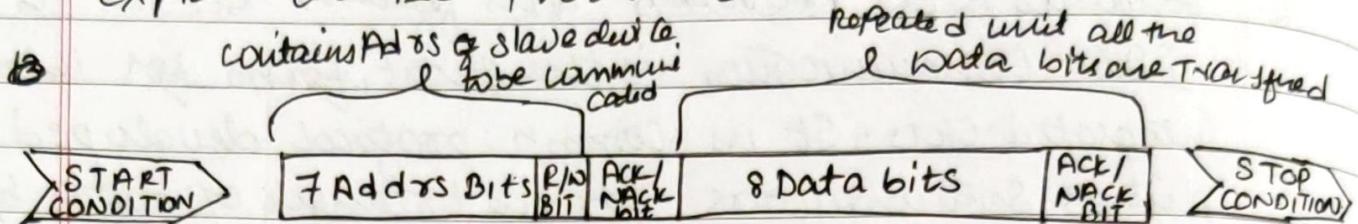
Simple mechanism for validation of data transferred

uses 7 bit addressing S/m to target a specific device/IC on I²C bus.

I²C networks are easy to scale. New devices can simply be connected to 2 common I²C bus lines.

I²C nw are easy to scale. New devices can simply be connected to the common I²C bus lines.

13. explain the I2C protocol bits



start condition

Whenever a master device / IC decides to start a transaction, it switches SDA line from high V_H level to a low V_L level before the SCL line switches from high to low. Once a start condition is sent by master device, all slave devices get active even if they are in sleep mode & wait for address bits.

Address Block-

It comprises of 7 bits and are filled with the address of slave device to / from which master device needs send/receive data.

Read/Write bit.

This bit specifies the direction of data transfer if the master IC needs to receive data from slave device, it is set to 1.

Ack/Nack Bit

It stands for ACK/NACK bit. If the physical address of any slave device coincides with address broadcasted by the master device, the value of this bit set to '0' by slave device. otherwise it remains at logic '1'

Data block-

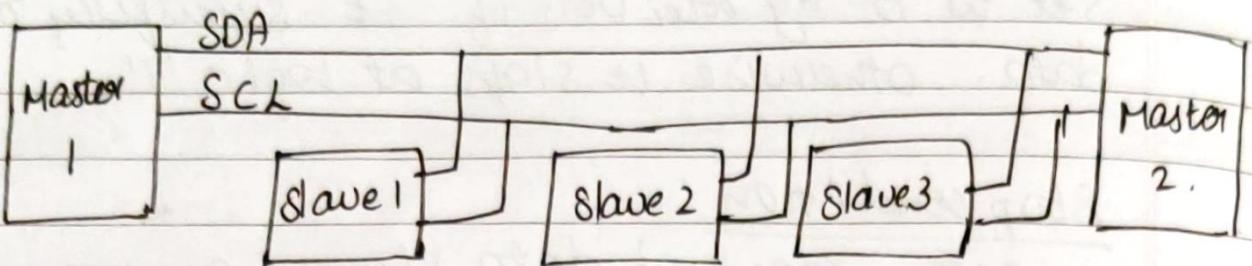
It comprises of 8 bits & they are set by sender with the data bits needs to transfer to receiver.

This block is followed by Ack / NACK bit is set to '0' by receiver if it successfully receives data. otherwise it stays at logic '1'

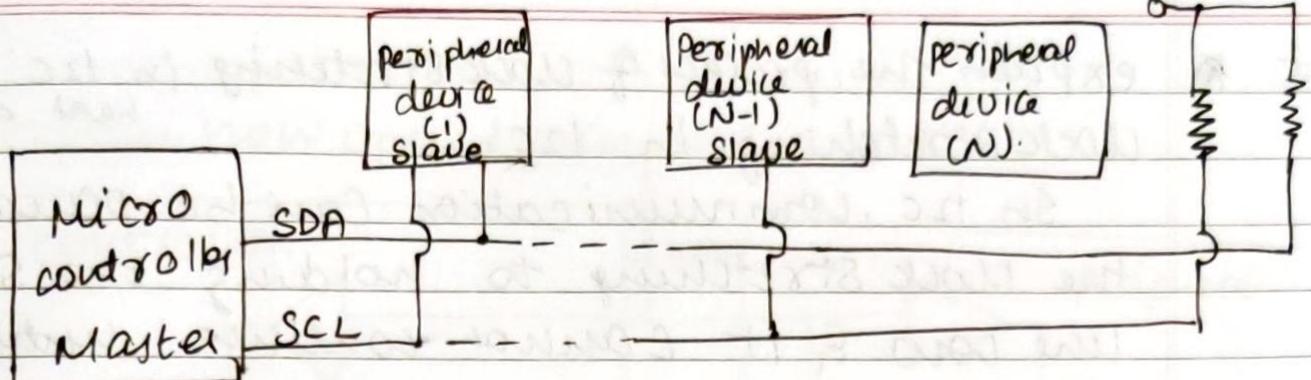
Stop condition

After required data blocks are transferred through the SDA line, the master device switches the SDA line from low v/g level to high v/g level before the SCL lines switches from high to low.

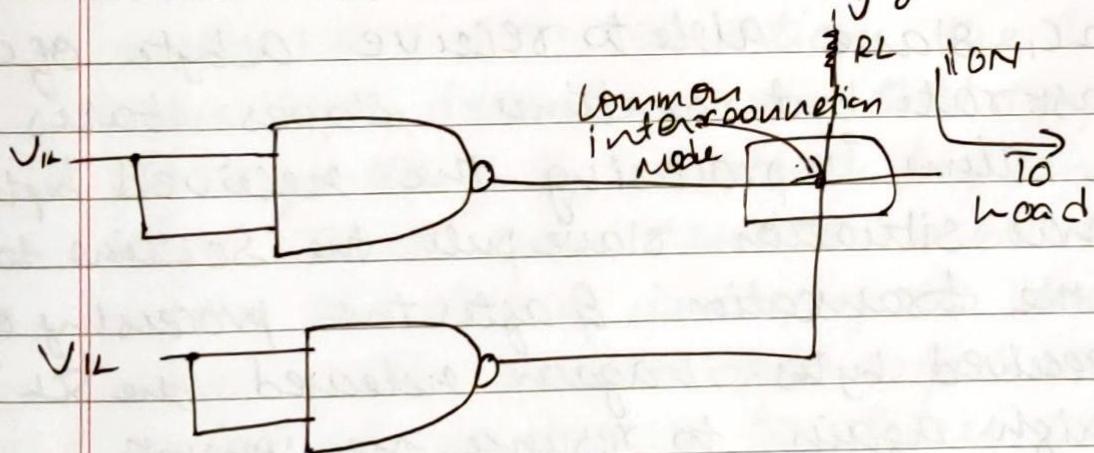
14. explain the arbitration process in I₂C



I₂C is designed for multiple master purpose this means that more than one device can initiate transfer during the Transfer. the Masters constantly monitor SDA & SCL. If one of them detects that SDA is low when it should actually high. It assumes that another master is active & immediately stops the transfer. This process is called arbitration for ex master 1 issues a Start Seq & sends an address , all slaves will likes. Including master2 which at the time , is considered a slave as well if address does not match master2 with holds its transaction until the bus becomes idle. The Structure of bus line low then the line stayslow. When master 2 changes the state of line to high then bus line doesn't go high then the bus is occupied already by some other device which has put the bus low such as master 1. Thus master doesn't get its data on bus. For as long as there has been no stop sequence present on bus it has to reach the bus & leaves the SCL & SDA line alone. If master can't make data line to go high then it loses the arbitration & needs to go back off & wait until the stop seq is seen later it can check the line & make another attempt when line is free.



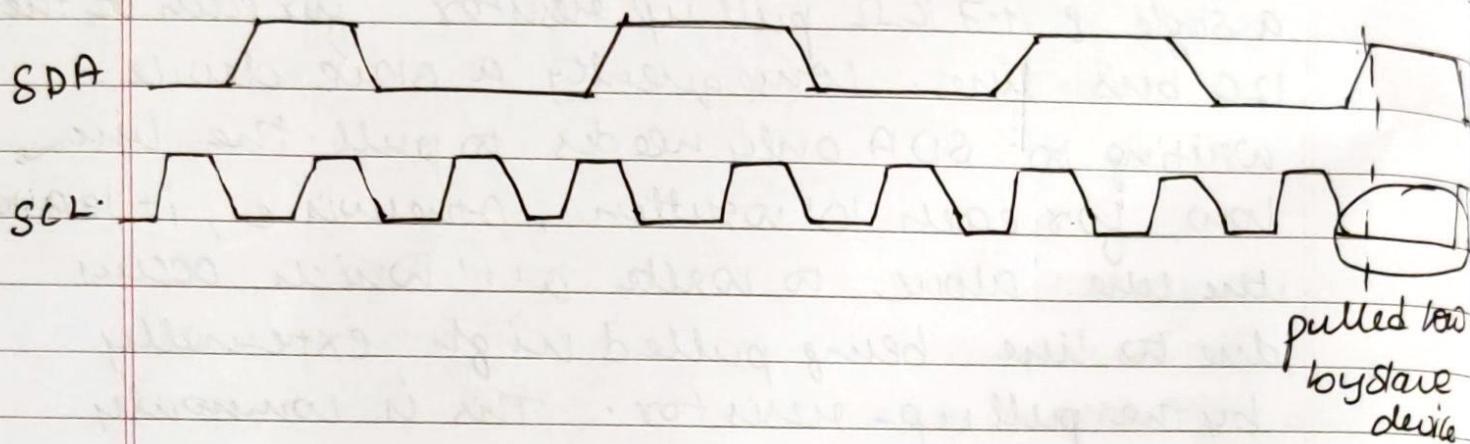
Electrical interconnection beyond the wires is a single $\pm 4.7\text{ k}\Omega$ pull up resistor for each of the I₂C bus lines. Consequently a slave device waiting to SDA only needs to pull the line low for each '0' written; otherwise, it leaves the line alone to write a '1' which occurs due to line being pulled high externally by the pull up-resistor. This is commonly known as wired-AND config.



Inputs		Outputs
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

15. Explain the process of clock stretching in I₂C with neat diagram.

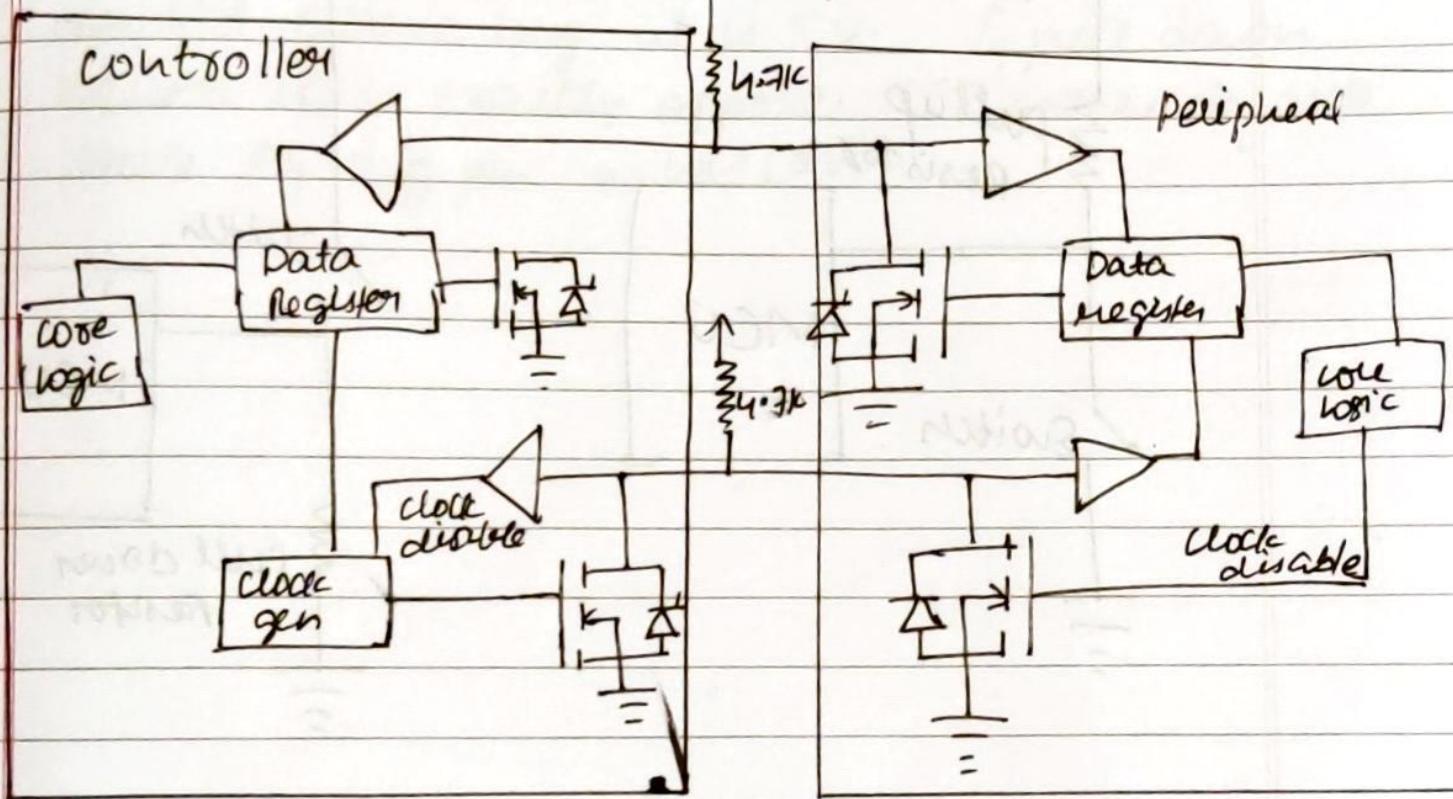
In I₂C, communication can be paused by the clock stretching to holding the SCL line low & it cannot continue until the SCL line released high again.



In I₂C, slave able to receive a byte of data on fast rate but sometimes slaves takes more time in processing the received bytes in that situation slave pull the SCL line to pause the transaction & after the processing of the received bytes. it again released the SCL line high again to resume the comm.

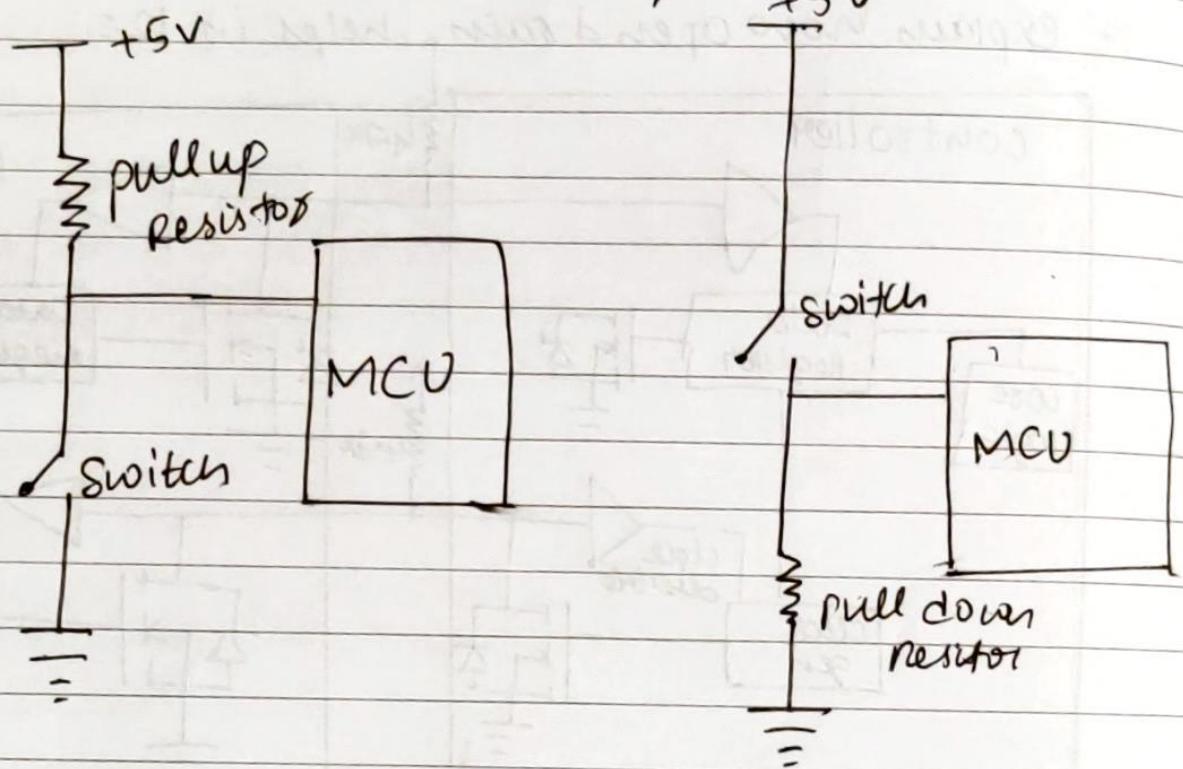
The clock stretching is the way in which slave drive the SCL line but it is fact most of the slave donot drives SCL line

17 explain how open drain helps in I²C



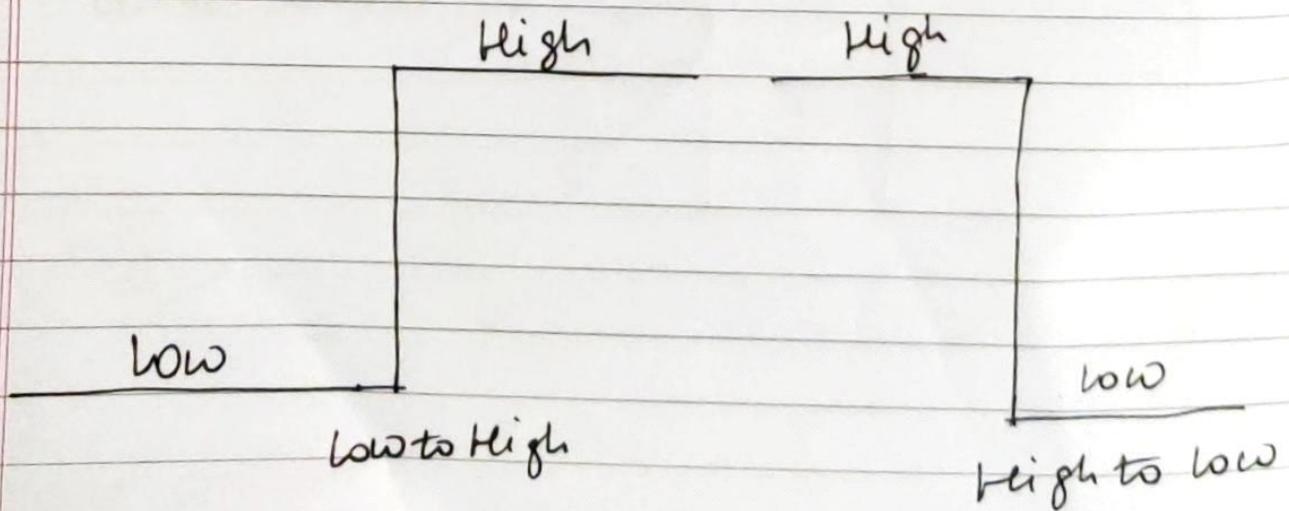
Unlike UART or SPI connections, the I²C bus drivers are "open drain", meaning that they can pull the corresponding S/g line low, but can't drive it high. Thus, there can be no bus contention where one device is trying to drive the line high while another tries to pull low, eliminating potential for damage to drivers or excessive power dissipation in S/m. Each S/g line has a pull up resistor on it; to restore the S/g to high when no device is asserting it low.

18. explain a) pullup resistor b) pulldown resistor



If we consider a digital CLCT, the pins are always be either 0 or 1. In some cases we need to change the state from 0 to 1 or from 1 to 0. in either case, we need to hold the d/g pin either 0 & then change the state to 1 or we need to hold it to 0 & then change to 1. In both cases, we need to make digital pin either 'High' or 'Low' but it can't be left floating.

SO in each case, the state gets changed as shown below.



A pull up resistor is used to make the default state of d/g pin as high or the logic level in the above img it is 5V. & pull down resistor does exactly opposite. It makes default state of d/g pin as low(0V)