Seminar #4 Report

Group 7

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This seminar consists of two parts, which are both regarding DC-DC converter. For the two parts, we carried out simulations with Simulink.

1 Boost converter

This simulation is concerning the step-up converter, whose main application is in regulated dc power supplies and the regenerative braking of DC motors.

1.1 Simulation Model

1.1.1 Circuit diagram

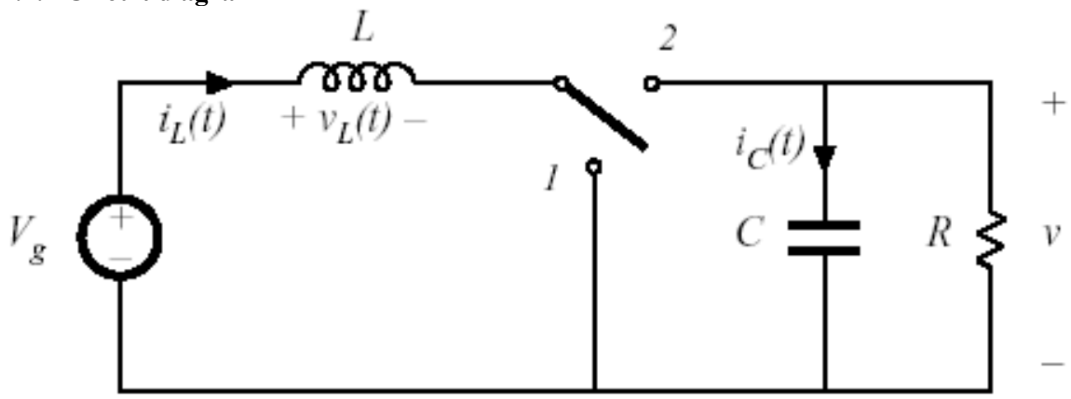

Fig. 1-1 Boost converter

As the name implies, the output voltage is always greater than the input voltage. When the switch is on, the diode is reversed biased, thus isolating the output stage. The input supplies energy to the inductor. When the switch is off, the output stage receives energy from the inductor as well as from the input. In the steady state analysis presented here, the output filter capacitor is assumed to be very large to ensure a constant output voltage.

1.2 Task 1

1.2.1 Task requirement

For given input/output voltage and circuit parameters, we need to calculate the theoretical value of inductor current ripple, capacitor voltage ripple and do simulations to verify the calculation results.

1.2.2 Simulink circuit diagram

In Simulink, we use the model as below to carry out simulation.

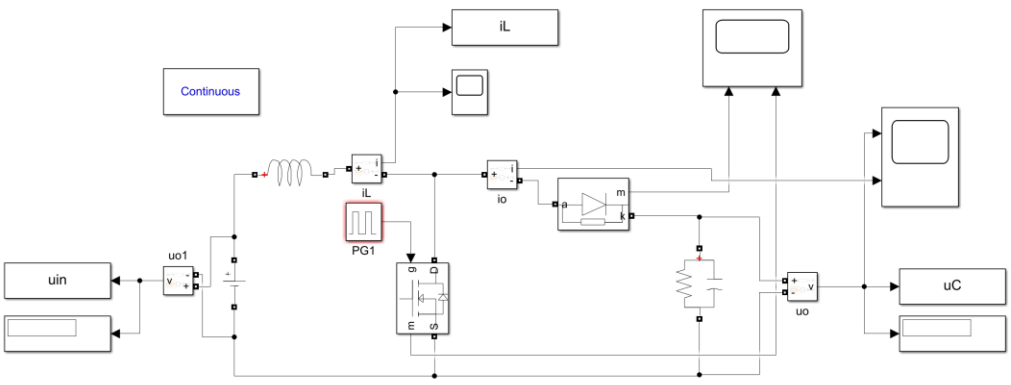

Fig. 1-2 Simulation model

And the parameters in the circuit are $V_{in} = 300V, V_o = 400V, f_s = 100kHz, R_L = 20\Omega,\ L = 300\mu H, C = 200\mu F$. For boost converter, we know that

$$U_o = \frac{1}{\beta}E = \frac{1}{1-\alpha}E = 400V$$

$$\alpha = 0.25$$

Therefore, we set the duty ratio to 25% so as to make the output voltage be $400V$.At steady state, we plot the waveform of the output.

1.2.3 Parameter setup

Tab. 1-1 Parameter setup of our group

Boost converter	Vin	Vo	RL	fs	L	C
	300V	400V	100Ω	100kHz	800uH	200uF

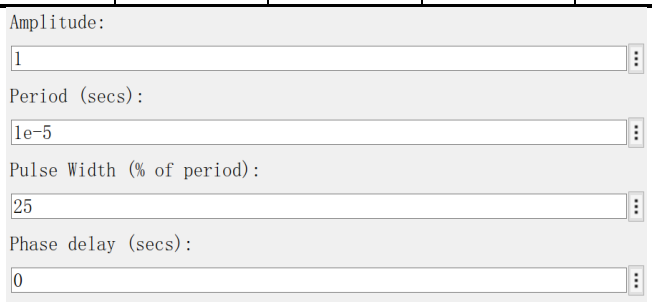

Fig. 1-3 pulse parameter setup

Fig. 1-4 input voltage parameter setup

Fig. 1-5 inductance parameter setup

Fig. 1-6 capacitor and resistance parameter setup

1.2.4 Result Waveform

When the duty cycle is 25%, we can get the output voltage is 400V. And from Ohm's law, we know the output current is 20A, which are the same as we can see in the simulation result.

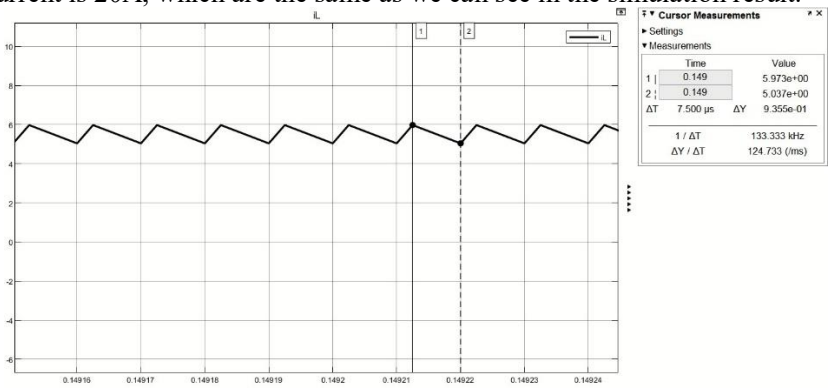

Fig. 1-7 Inductor current ripple

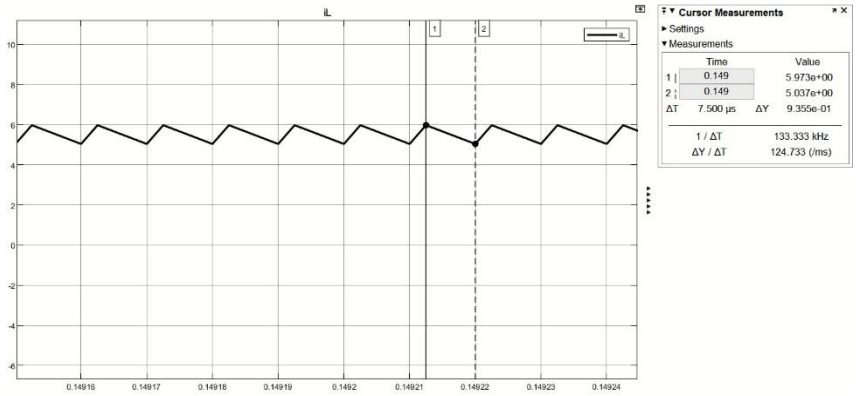

Fig. 1-8 Inductor current ripple

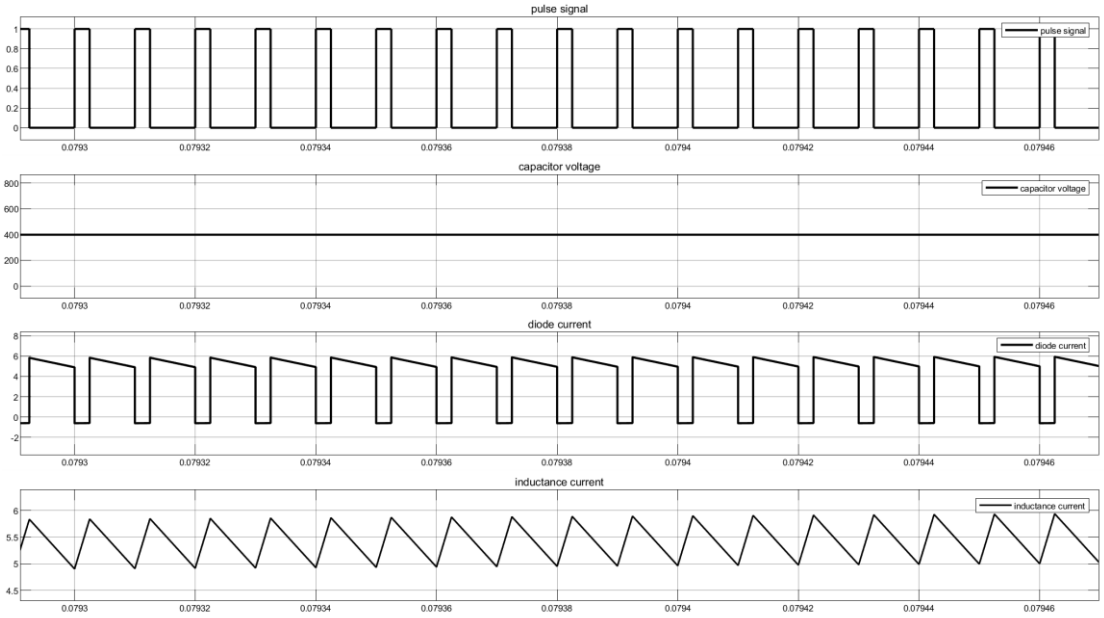

Fig. 1-9 Simulation result

1.2.5 Inductor current ripple

Similarly, the inductor current ripple could be derived from:

$$\Delta i_L = \frac{V_{in} D T_s}{L}$$

Based on the given parameter, we could calculate our inductor current ripple

$$\Delta i_L = \frac{300 \times 0.25}{800\mu \times 100k} = 0.9375\text{A}$$

What's more, we could also derive from differential equations based on the definition of ripple, but that's not so convenient as the method above.

1.2.6 Capacitor voltage ripple

The peak-to-peak ripple in the output voltage could be calculated by considering the waveform below. Assuming that all the ripple current component of diode current i_D flows through the diode current capacitor and its average value flow through the load resistor because the voltage ripple is very small. The charge ΔQ is represented by the shaded area in the following waveform. Therefore, the peak-to-peak voltage ripple is given by

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{I_o D T_s}{C} = \frac{V_o}{R} \frac{D T_s}{C}$$

Based on the given parameter, we could calculate our output voltage ripple

$$\Delta V_o = \frac{400 \times 0.25}{100 \times 200\mu \times 100k} = 0.05\text{V}$$

1.2.7 Comparison between theory and simulation

Getting the simulation value from the figure, we analyze the error as below.

Tab. 1-2 Comparison of theoretical and simulation value

	Theoretical value	Simulation value	Percentage error
Inductor current ripple	0.9375A	0.9355A	0.213%
Capacitor voltage ripple	0.05V	0.05567V	13.34%

From the comparison, we can see the theoretical value and simulation value are almost the same.

1.3 Task 2

1.3.1 Task requirement

For boost converter, we adjusted the duty cycle D from 0.3 to 0.8, describe the relationships between duty cycle D and inductor current ripple, capacitor voltage ripple, voltage gain and verify your results through simulation.

1.3.2 simulation result

1.3.2.1 Relationship between G and D

For boost converter, we all know that

$$V_C = \frac{1}{1-D} V_{in}$$

.

Therefore, we can easily get the relationship between voltage gain and D as

$$G = \frac{1}{1-D} = \frac{V_C}{V_{in}}$$

As a consequence, we plotted the theoretical value of G and the fit of simulation result of G to compare with each other. As it shows in the Fig. 1-8, the red line is the theoretical result of G and the black line is the simulation result of G.

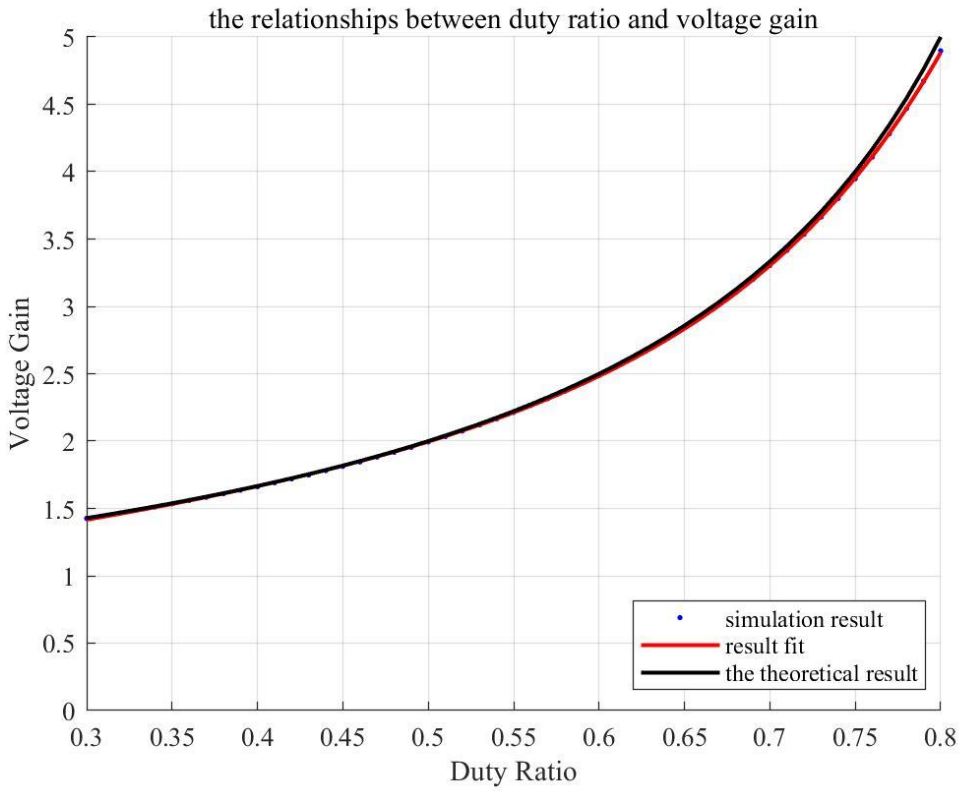

Fig. 1-10 Relationship between G and D

The diagram shows they are quite close. From the Matlab, we can get the fit result and error as following:

```
gof =
          sse: 0.0010
      rsquare: 1.0000
          dfe: 47
    adjrsquare: 1.0000
         rmse: 0.0046
```

Because the value of square of R is close to 1, the Matlab shows the voltage gain fits quite well.

1.3.2.2 Relationship between inductor current ripple and D

In our simulation, we get the curve between inductor current ripple and duty cycle as below.

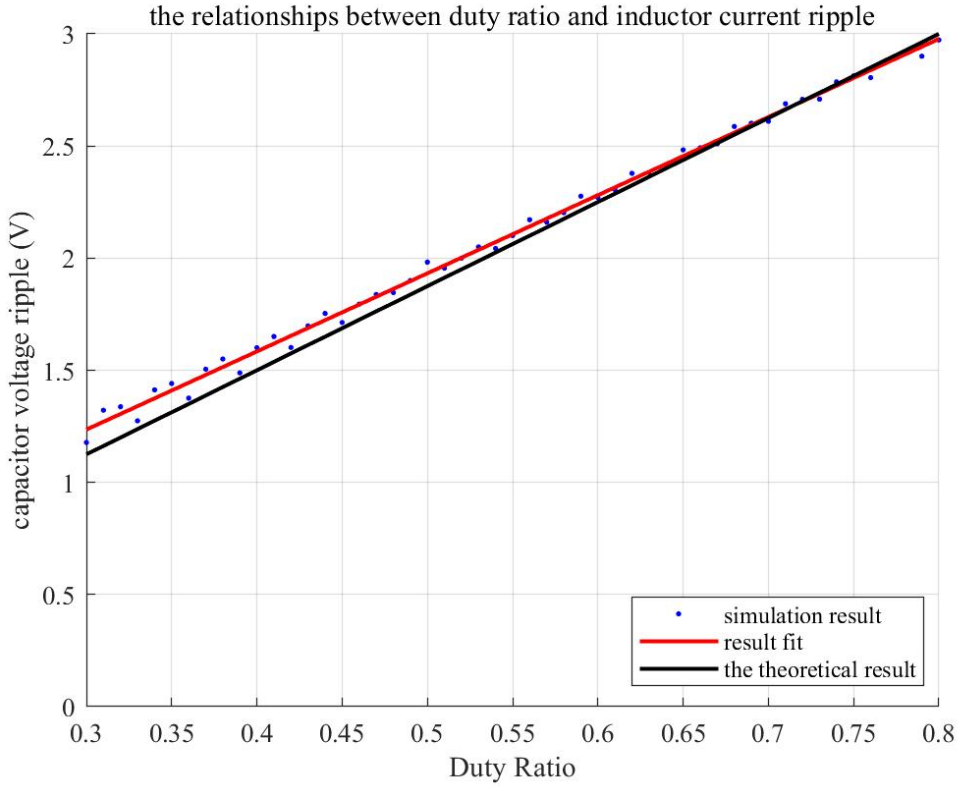

Fig. 1-11 Relationship between Δi_L and D

From the textbook, we can get the equation:

$$\Delta i_L = \frac{V_{in}}{L} t_{on}$$

When $V_{in} = const$, the function between D and Δi_L should be a straight line just like the black curve showed in the diagram above. Besides, the red curve shows the result from simulation. The error between blue curve and red one is very small, so we can think the simulation successful.

The diagram shows they are quite close. From the Matlab, we can get the fit result and error as following:

```
gof =
          sse: 0.0452
      rsquare: 0.9966
          dfe: 49
    adjrsquare: 0.9966
         rmse: 0.0304
```

Because the value of square of R is close to 1, the Matlab shows the voltage gain fits quite well.

1.3.2.3 Relationship between capacitor voltage ripple and D
In Simulink, we plot the curve between Δu_C and D.

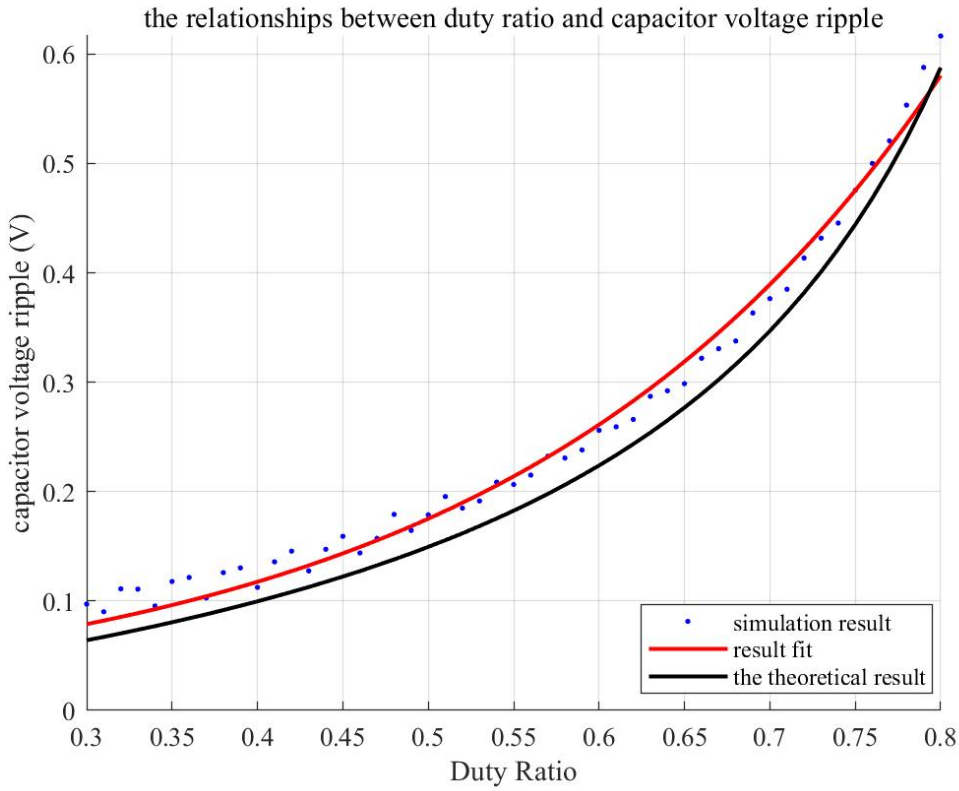

Fig. 1-12 Relationship between Δu_C and D

The peak-to-peak ripple in the output voltage can be calculated by considering the waveforms shown in Fig. for a continuous mode of operation. Assuming that all the ripple current component of the diode current i_D flows through the capacitor and its average value flows through the load resistor, the shaded area in Fig. represents charge $\triangle Q$. Therefore, the peak-peak voltage ripple is given by

$$\Delta U_C = \frac{\Delta Q}{C} = \frac{I_o D T_s}{C} = \frac{V_o D T_s}{RC}$$

When $V_{in} = const$, the function between D and ΔU_C should be a straight line just like the black curve showed in the diagram above. Besides, the red curve shows the result from simulation. The error between blue curve and red one is very small, so we can think the simulation successful.
The diagram shows they are quite close. From the Matlab, we can get the fit result and error as following:

```
gof =
          sse: 0.0104
      rsquare: 0.9898
          dfe: 49
   adjrsquare: 0.9896
         rmse: 0.0146
```

Because the value of square of R is close to 1, the Matlab shows the voltage gain fits not so well.

1.3.3 simulation error

We plotted the figure of the relative error of simulation.

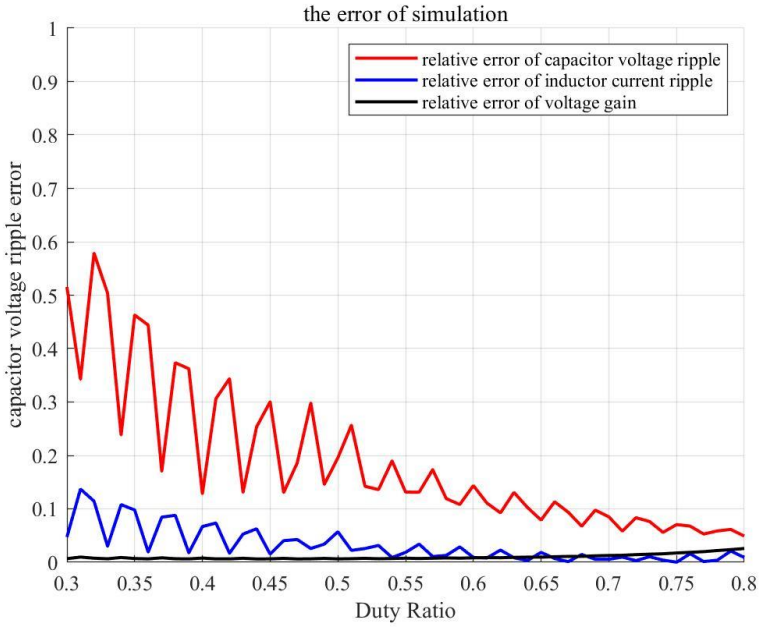

Fig. 1-7 the error of the simulation

The figure shows the relative error of capacitor voltage ripple is the largest and the figure shows the relative error of inductance current ripple is the smallest. We could know that the relative error of inductance current ripple is about 10% at first and drops slowly as the duty ratio increases, reaching almost zero when duty ratio is about 60%. Besides, we could know that the relative error of capacitor voltage ripple is about 60% at first and drops slowly as the duty ratio increases, reaching almost 10% when duty ratio is about 80%. For the simulation of voltage gain, the result is pleasing, there's almost no error between calculation results and simulation results.

1.3.4 Appendix

This part includes the analysis program and the figure program about the simulation. The file 'analysis.m' is to research the relationships between duty cycle D and inductor current ripple, capacitor voltage ripple, voltage gain (G=Vo/Vin) with different duty ratio. And the file 's4_figure' is to plot the figure of the relationships between duty cycle D and inductor current ripple, capacitor voltage ripple, voltage gain (G=Vo/Vin) and plot the error of simulations

1.3.4.1 analysis.m

```
clc;
clear;
close all;


%% parameter setup
j = 0; % 计数变量
Vin = 300; % 输入电压
RL = 100; % 负载电阻
f = 1e5; % 频率
T = 1./f; % 周期
C = 200e-6; % 电容
L = 800e-6; % 电感
step = 0.01; % 步长
```

```
D = [0.3:step:0.8]; % 占空比

%% result matrix initialization
num = length(D);
iL_result = zeros(1,num);
uC_result = zeros(1,num);
uin_result = zeros(1,num);
delta_uC = zeros(1,num);
delta_iL = zeros(1,num);

%% run simulation with different Duty ratio
for d = 30:100*step:80
    tem = d; % middle tem
    set_param('seminar4_topic1/PG1','PulseWidth','tem'); % Set up
duty ratio
    sim('seminar4_topic1',[0,0.1]); % Run simulation
    iL_result(j+1) = iL(end);
    uC_result(j+1) = uC(end);
    uin_result(j+1) = uin(end);
    delta_uC(j+1) = max(uC(end-50:end))-min(uC(end-50:end));
    delta_iL(j+1) = max(iL(end-500:end))-min(iL(end-500:end));
    % result check
    disp(['When Duty Ratio is ',num2str(d),'%']);
    disp(['Capacitor Voltage is ',num2str(uC(end)),'V']);
    disp(['Inductance Voltage is ',num2str(iL(end)),'A']);
    disp(['Capacitor Voltage Ripple is
',num2str(delta_uC(j+1)),'V']);
    disp(['Inductor Current Ripple is
',num2str(delta_iL(j+1)),'A']);
    disp('~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~')
    j = j+1;
end

%% calculate inductor current ripple, capacitor voltage ripple,
voltage gain
delta_uC_cal = (uC_result.*D.* T) ./ (C.*RL);
delta_iL_cal = Vin.*D.*T./L;
G = uC_result./uin_result;

%% save DATA
save SEMINAR4_DATA D delta_uC delta_iL G delta_uC_cal
delta_iL_cal
```

1.3.4.2 s4_figure.m

```
clc;
```

```
clear;
close all;

load SEMINAR4_DATA
load SEMINAR4_DATA_TOPIC
% fit figure
[fitresult, gof] = createFit1(D, delta_uC, delta_uC_cal);
[fitresult, gof] = createFit3(D, delta_iL, delta_iL_cal);
[fitresult, gof] = createFit2(D, G);

%% error analysis
% capacitor voltage ripple error
figure('name','v')
plot(D,abs(delta_uC-delta_uC_cal)./delta_uC_cal,'k-
','linewidth',1.5);
xlabel('Duty Ratio')
ylabel('capacitor voltage ripple error')
axis([0.3,0.8,0,1]);
set(gca,'FontName','Times New Roman');
set(findobj('Type','line'),'LineWidth',1.5)
title('the error of simulation about capacitor voltage ripple')
grid on

% inductor current ripple error
figure('name','i')
plot(D,abs(delta_iL-delta_iL_cal)./delta_iL_cal,'k-
','linewidth',1.5);
xlabel('Duty Ratio')
ylabel('inductor current ripple error')
axis([0.3,0.8,0,1]);
set(gca,'FontName','Times New Roman');
set(findobj('Type','line'),'LineWidth',1.5)
title('the error of simulation about inductor current ripple')
grid on

% voltage gain error
figure('name','g')
plot(D,abs(G-1./(1-D))./(D./(1-D)),'k-','linewidth',1.5);
xlabel('Duty Ratio')
ylabel('voltage gain error')
axis([0.3,0.8,0,1]);
set(gca,'FontName','Times New Roman');
set(findobj('Type','line'),'LineWidth',1.5)
title('the error of simulation about voltage gain')
```

```
grid on

%% the relationships between D and voltage gain
[fitresult, gof] = createFit4(D1, G1);
```

1.3.4.3 creatFit1.m

```
function [fitresult, gof] = createFit1(D, delta_uC, delta_uC_cal)
%CREATEFIT(D,DELTA_UC)
%  Create a fit.
%
%  Data for 'untitled fit 1' fit:
%      X Input : D
%      Y Output: delta_uC
%  Output:
%      fitresult : a fit object representing the fit.
%      gof : structure with goodness-of fit info.
%
%  另请参阅 FIT, CFIT, SFIT.

%  由 MATLAB 于 22-Nov-2020 12:01:16 自动生成


%% Fit: 'untitled fit 1'.
[xData, yData] = prepareCurveData( D, delta_uC );

% Set up fittype and options.
ft = fittype( 'exp1' );
opts = fitoptions( 'Method', 'NonlinearLeastSquares' );
opts.Display = 'Off';
opts.StartPoint = [188.632179365306 4.19747074498863];

% Fit model to data.
[fitresult, gof] = fit( xData, yData, ft, opts );

% Plot fit with data.
figure( 'Name', 'untitled fit 1' );
hold on
plot( fitresult, xData, yData );
plot(D,delta_uC_cal,'k-','linewidth',1.5);
hold off
xlabel('Duty Ratio')
ylabel('capacitor voltage ripple (V)')
axis([-inf,inf,0,inf]);
set(gca,'FontName','Times New Roman');
set(findobj('Type','line'),'LineWidth',1.5)
```

```
legend('simulation result','result fit','the theoretical
result');
title('the relationships between duty ratio and capacitor voltage
ripple')
grid on
```

(the other functions are similar to this function, they are all using the curve fit tool toolbox in MATLAB, so they are not posted here.)

2 full-bridge inverter + full-wave rectifier

2.1 Simulation model

This simulation is concerning the full-bridge inverter + full-wave rectifier , whose main application is in regulated dc power supplies and the regenerative braking of DC motors.

2.1.1 Circuit diagram

In Simulink, we use the model as below to carry out simulation.

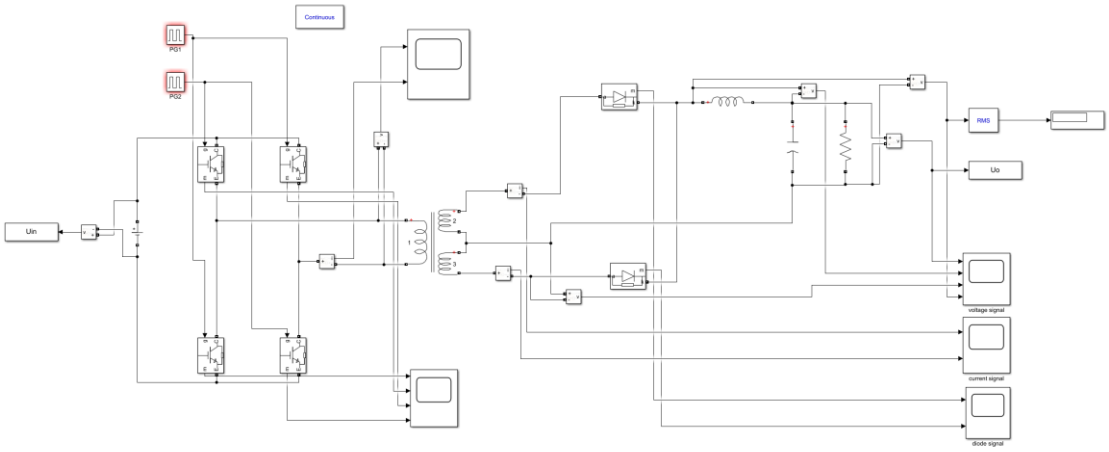

Fig. 2-1 Simulink model

And the parameters in the circuit are $V_{in} = 600V, V_o = 200V, f_s = 100kHz, R_L = 10\Omega,\ \ L = 300\mu H, C = 200\mu F, k = 4:1:1$.

In the circuit, we have that

$$\frac{V_o}{V_{in}} = \frac{2D}{T}$$

Therefore, we set the duty ratio to 16% so as to make the output voltage be $48V$.

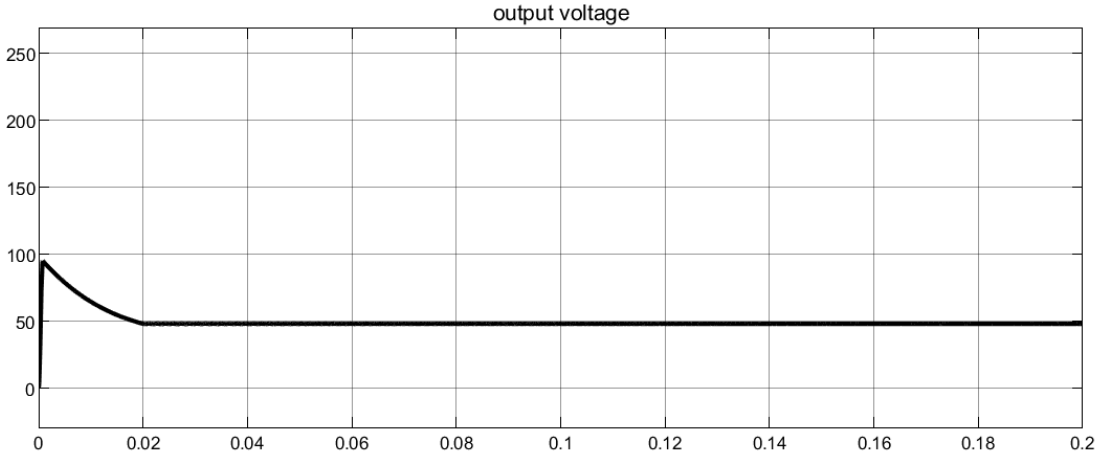

Fig. 2-2 waveform of RMS value of output voltage

2.2 Task 1

2.2.1 Task requirement

For given input/output voltage and circuit parameters, we need to do simulations to study the operating principle and analyze the operating sequence.

2.2.2 Parameter setup

Table 2-1. The Given Parameters for Topic2

Vin	Vo	RL	fs	L	C	Vin
600V	48V	4:1:1	10	100kHz	300uH	200uF

2.2.3 Operating principle and sequence

This circuit can be divided into two parts by the transformer, a full-bridge inverter on the left and a full-wave rectifier on the right. Through the inverter, the direct current will be transformed into alternating current. Then, the transformer will convert the voltage level. Owing to the two power diodes, the AC will be converted to DC finally. Therefore, the structure is an indirect DC to DC converter.

2.2.3.1 Full-bridge inverter

In the full-bridge inverter, the four MOSFETs are divided into two groups. S_1 and S_4 are in group 1 and group 2 consists of S_2 and S_3. MOSFETs in one group conduct together and the two groups conduct alternant. The duty cycle D is defined as the time one group conducts in one period. We set D = 0.16 to learn the principle of the circuit. Waveforms of triggering pulses and MOSFET voltage and current are shown as below.

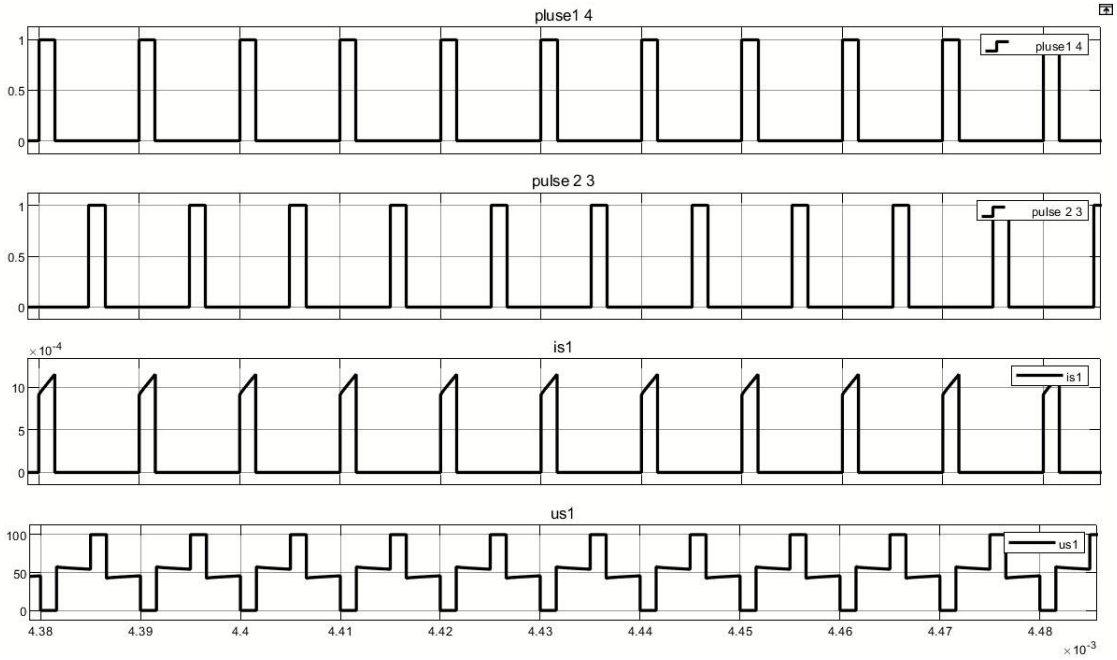

Fig. 2-3 Waveforms of triggering and voltage and current of MOSFET

We have V_{in}=600V. When S1 and S4 at on state, the current flow through S2 and S3 increases gradually and the voltage across S2/S3 is 600V. When S2 and S3 are on, the situation is the same. When S1-S4 are all at off state, the voltage across each MOSFET is $\frac{V_{in}}{2} = 300V$.

From the figure, we can easily get operating sequence shown as below.

Tab. 2-1 Operating sequence

Time interval	Conductive MOSFET
0-DT	S_1, S_4
DT-T/2	\
T/2-(D+1/2) T	S_2, S_3
(D+1/2) T-T	\

2.2.3.2 Full-wave rectifier

The voltage waveforms of primary side and secondary side of the linear transformer are shown below.

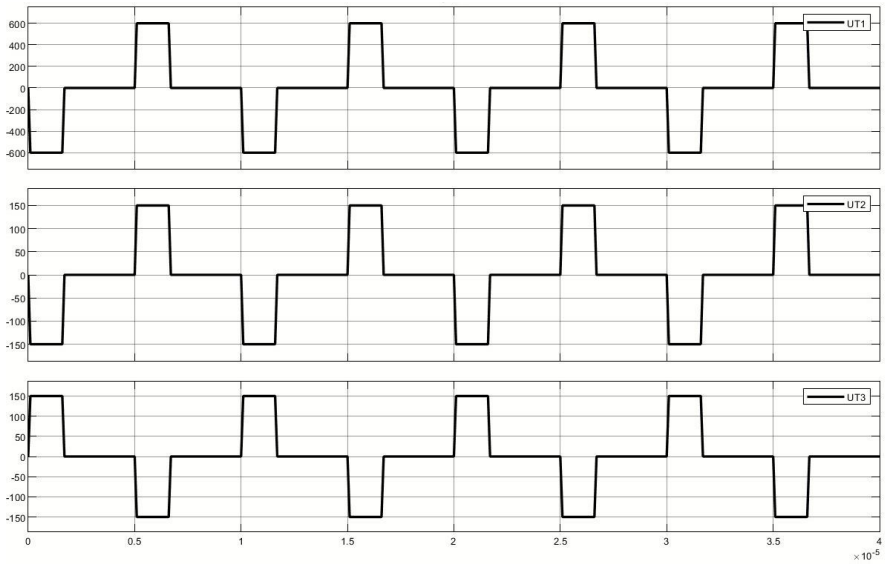

Fig. 2-4 Transformer voltage waveform

From the figure, the amplitude value of voltage equals to 600V and 150V on the primary side and secondary side respectively, which fits the ratio of transformation (4:1:1).

Then we plot the waveforms of load conductor and two diodes current.

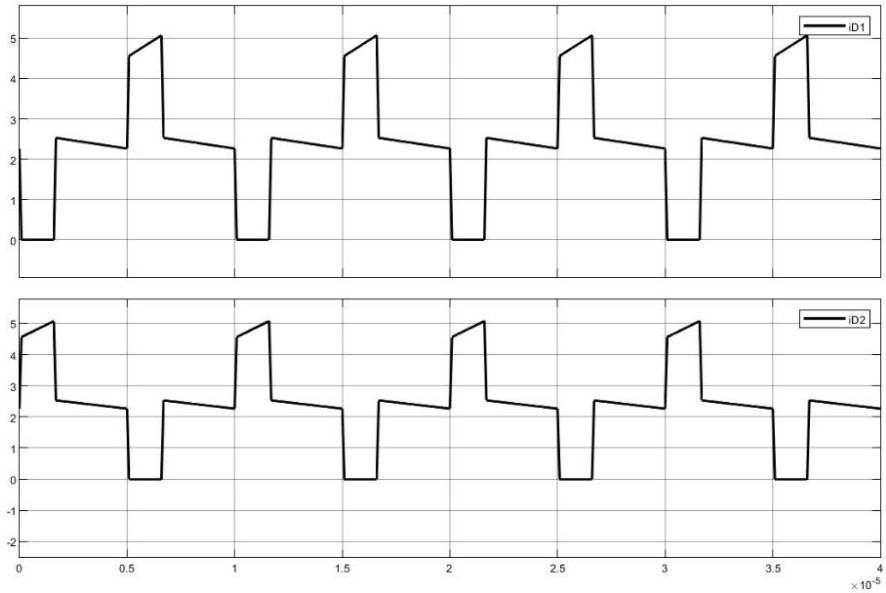

Fig. 2-5 Sequence of two diodes

When S1 and S4 conduct, UT2 is positive and VD1 is at on-state. When S2 and S3 conduct, UT2 is negative and VD2 is at on-state. If the four MOSFETs are all at off-state, the inductor discharges through the two diodes.

The figure below shows the value of output voltage, we measure the value by using the cursor in scope. We could know that the output voltage is exactly 48V, the same as the calculation result.

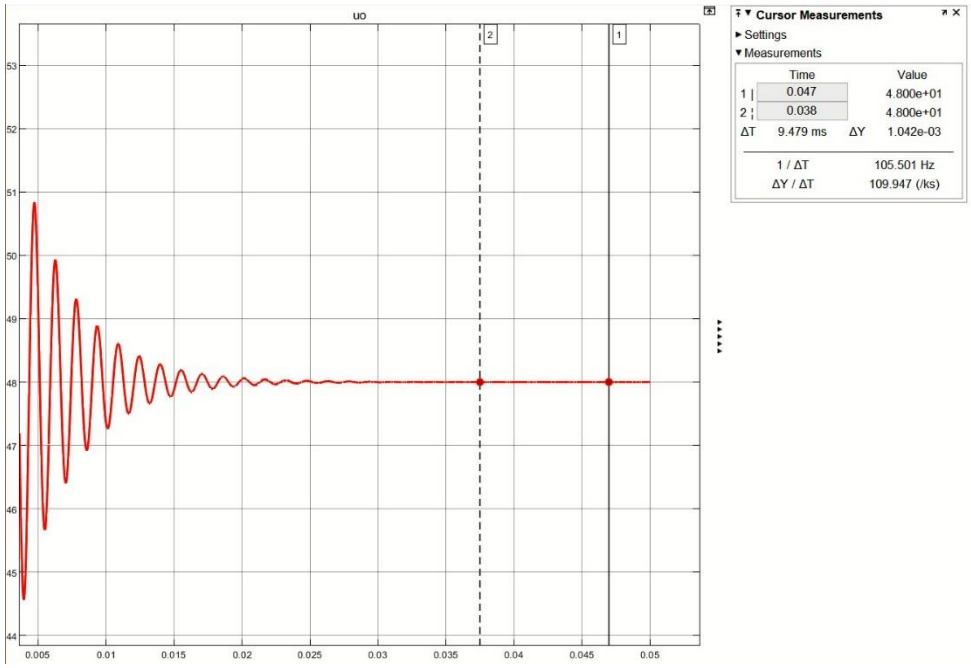

Fig. 2-6 Conductor voltage and current and output voltage

Afterwards, we got the waveform of inductor current and the detailed waveform of output voltage, which are shown below:

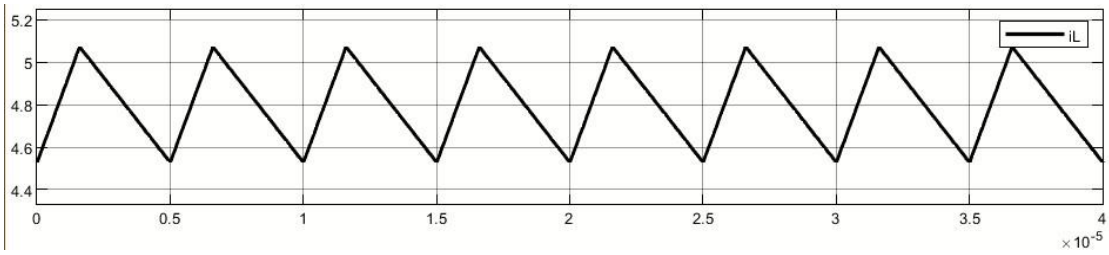

Fig. 2-7 Inductance current signal

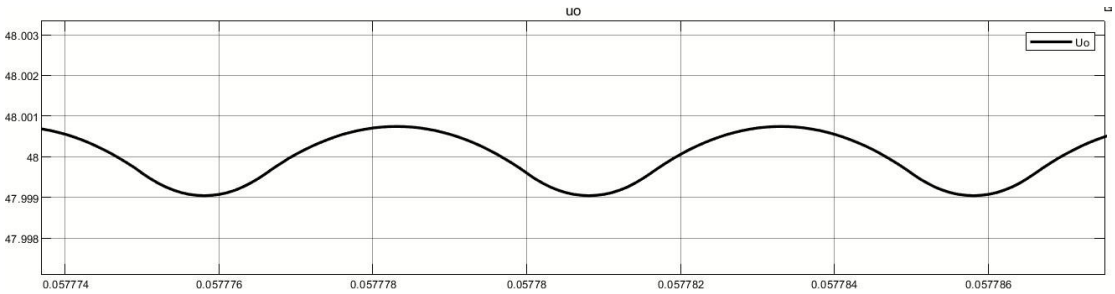

Fig. 2-8 capacitor voltage signal

Given that $u_L = L\frac{di}{dt}$, so when the inductor is charging, the voltage is positive and when it's discharging, the voltage is negative. The inductor and capacitor make up a low-pass filter, which makes the output voltage almost a constant value with small ripple, which fits the figure.

2.3 Task 2

2.3.1 Task requirement

We need to adjust the load resistor to realize continuous current mode (CCM) and discontinuous current mode (DCM) and verify through simulation.

2.3.2 Theoretical analyzation

In the indirect DC converter, CCM and DCM is determined by the conductor current. Due to the current ripple, in some case the conductor ripple may be zero and we term this mode is DCM. On

the contrary, if the current is always bigger than zero, the mode is termed CCM.
In this part, the circuit consists of a full-bridge inverter and a full-wave rectifier. In order to analyze the inductor current, the circuit can be equivalent to a boost converter. And the equivalent circuit and parameters are shown as below.

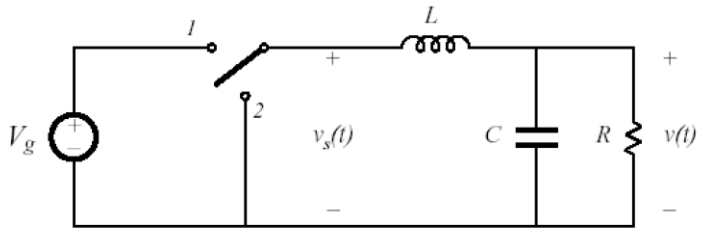

Fig. 2-9 Equivalent boost converter

Tab. 2-2 Equivalent parameters

Parameters	Equivalent parameters	Value
V_{in}	$\frac{V_{in}}{k}$	600V
V_o	V_o	48V
D	2D	0.32
f_s	$2f_s$	100kHz
R	R	10Ω
L	L	300μH
C	C	100μF

From the former analyzation, we know output voltage ripple is very small, so we can neglect the voltage ripple and think the output is constant voltage v_o.
In Fig. 2-7, we can see the on state of the boost converter.

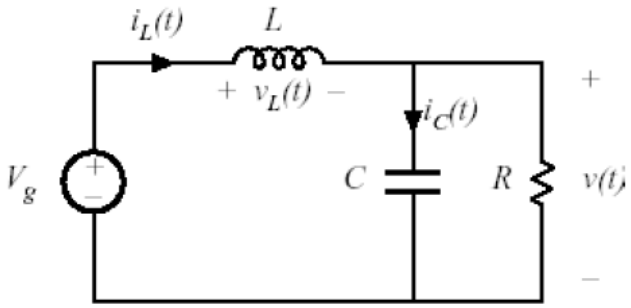

Fig. 2-10 On state of boost converter

We assume output is a constant voltage, so we have

$$V_{in} - V_o = L\frac{di_L}{dt}$$

The slope of inductor current is constant

$$\frac{di_L}{dt} = \frac{V_{in} - V_o}{L}$$

Similarly, at the off state, the slope of inductor current is also constant.

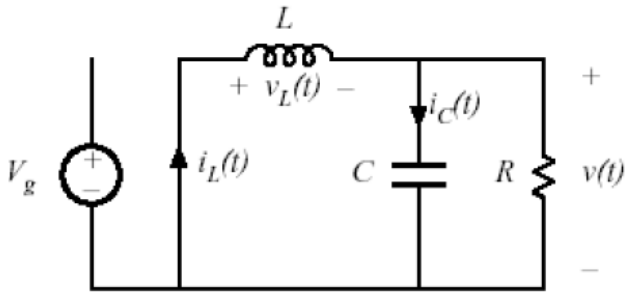

Fig. 2-11 Off state of boost converter

$$-V_o = L\frac{di_L}{dt}$$
$$\frac{di_L}{dt} = -\frac{V_o}{L}$$

Therefore, the waveform of inductor current is linearly as below.

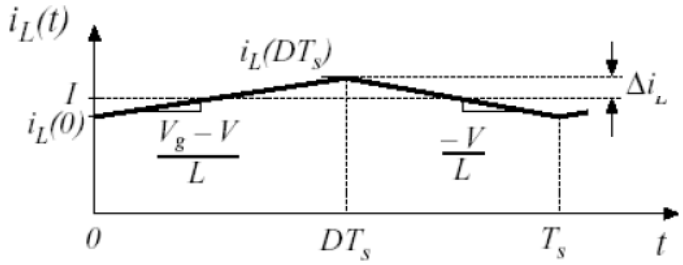

Fig. 2-9 Waveform of inductor current

When the current is continuous, we have

$$\frac{V_o}{R} > \Delta i = \frac{V_{in} - V_o}{2L}DT$$
$$R < \frac{2LV_o}{(V_{in} - V_o)DT} = 176.4706\Omega$$

2.2.3 Simulation verification

From the calculation, we know the critical resistance is 176.4706Ω. In Simulink, we plot the waveform of the current.

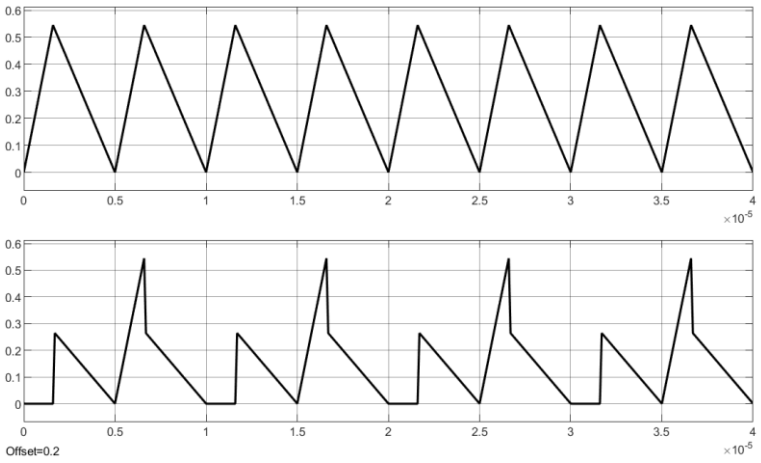

Fig. 2-12 Critical mode current

From the waveform, we can see the minimum of the current is 0.
Actually in the simulation, we cannot get the ideal current when $R = 176.4706\Omega$. We get Fig. 2-10 with $R = 100\Omega$. The deviation may be led by the nonideal devices in the simulation circuit.
With $R = 200\Omega$ and $R = 100\Omega$, we get the current waveforms under CCM and DCM and show them below respectively.

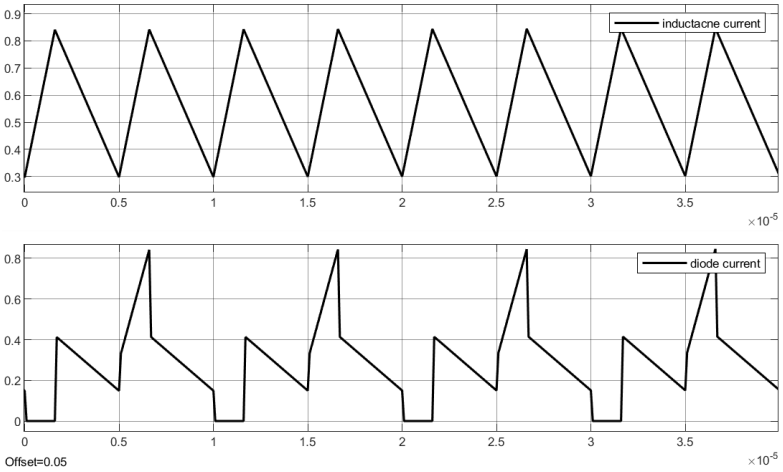

Fig. 2-13 CCM inductor current

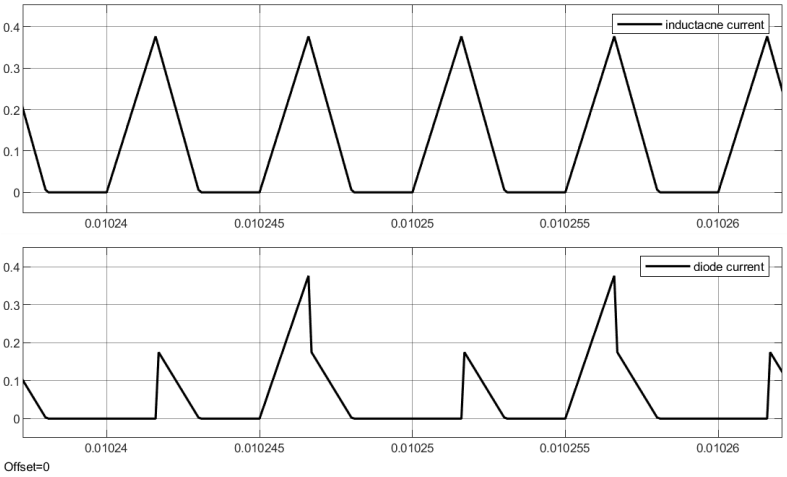

Fig. 2-14 DCM inductor current

2.4 Task 3

2.4.1 Task requirement

In this task we need to adjust duty cycle D and analyze the relationships between D and voltage gain.

2.4.2 Simulation result and analyzation

In order to avoid the situation where the four MOSFETs conduct together during the commutation (it may destroy the circuit), duty cycle shouldn't be bigger than 0.5. We adjust D from 0 to 0.5 to carry out the simulation and get the result as below.

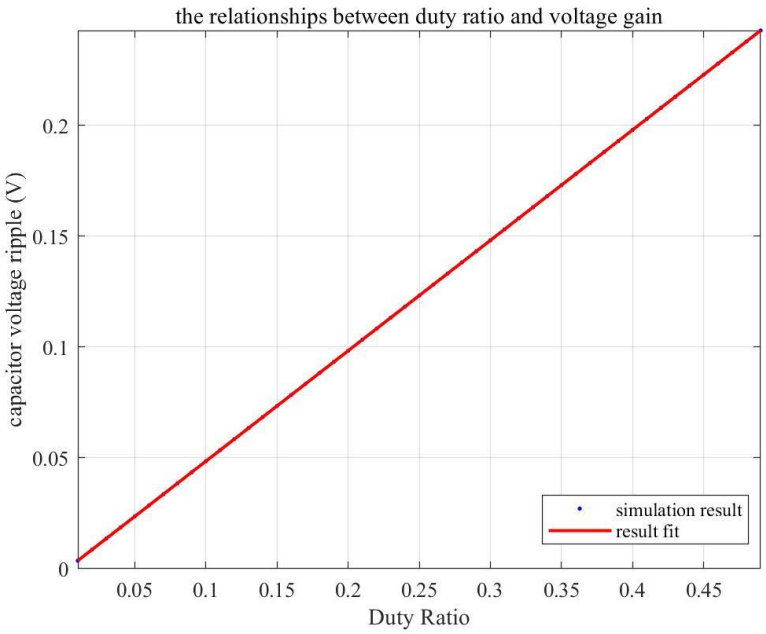

Fig. 2-15 Relationship between G and D

We can see the relationship between G and D is almost linear.
Actually, we have

$$G = \frac{V_o}{V_{in}} = \frac{2D}{k} = \frac{D}{2}$$

For our group, the ratio of transformation $T = 4$. Therefore, the slope of our curve should be 0.5 and from the simulation result we could conclude that the calculation result is almost the same as the simulation result.

2.4.3 Appendix

This part includes the analysis program and the figure program about the simulation. The file 'analysis.m' is to research the relationships between duty cycle D and voltage gain (G=Vo/Vin) with different duty ratio.

2.4.3.1 analysis2.m

```
clc;
clear;
close all;

%% parameter setup
j = 1; % 计数变量
Vin = 600; % 输入电压
Vo = 48; % 输出电压
RL = 10; % 负载电阻
f = 1e5; % 频率
T = 1./f; % 周期
C = 200e-6; % 电容
L = 300e-6; % 电感
step = 0.01; % 步长
D1 = [0.01:step:0.49]; % 占空比

%% calculate critical resistance
```

```
disp('Critical resistance is')
Ds = 0.16;
R_c = 2.*L.*Vo./((Vin./4-Vo)*Ds.*T);
disp(R_c)

%% result matrix initialization
num = length(D1);
Vin_result = zeros(1,num);
Vout_result = zeros(1,num);
G1 = zeros(1,num);

%% run simulation with different Duty ratio
for d = 1:100*step:49
    tem1 = d; % middle tem
    tem2 = d;
    set_param('Seminar4_topic2_2/PG1','PulseWidth','tem1'); % Set
up duty ratio
    set_param('Seminar4_topic2_2/PG2','PulseWidth','tem2'); % Set
up duty ratio
    sim('Seminar4_topic2_2',[0,0.1]); % Run simulation
    Vin_result(j) = Uin(end);
    Vout_result(j) = Uo(end);
    G1(j) = Vout_result(j)./Vin_result(j);
    % result check
    disp(['When Duty Ratio is ',num2str(d),'%']);
    disp(['Input Voltage is ',num2str(Vin_result(j)),'V']);
    disp(['Output Voltage is ',num2str(Vout_result(j)),'V']);
    disp(['Voltage Gain is ',num2str(G1(j))]);
    disp('~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~')
    j = j+1;
end

save SEMINAR4_DATA_TOPIC G1 D1
```