Seminar seven

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1. Topic :

1.1 The aim of topic :

1.1.1 For hard-switching Buck converter:

1) Observe the switching waveform of power switch Q

2) Plot loss curve

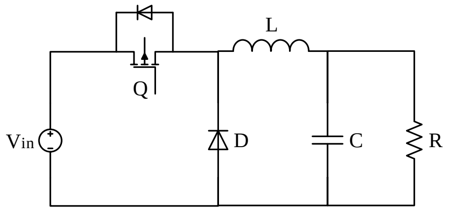

Figure.1 Hard-Switching Buck Converter

1.1.1 For ZVS QRC Buck converter:

1) Observe the switching waveform of power switch Q

2) Plot loss curve and compare with previous case

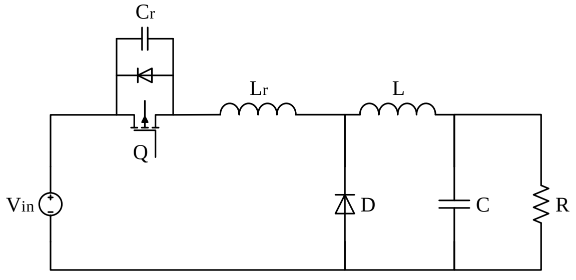

Figure.2 ZVS QRC Buck Converter

2. Simulation models and settings:

3.1 hard-switching buck converter:

We built simulation circuit shown below:

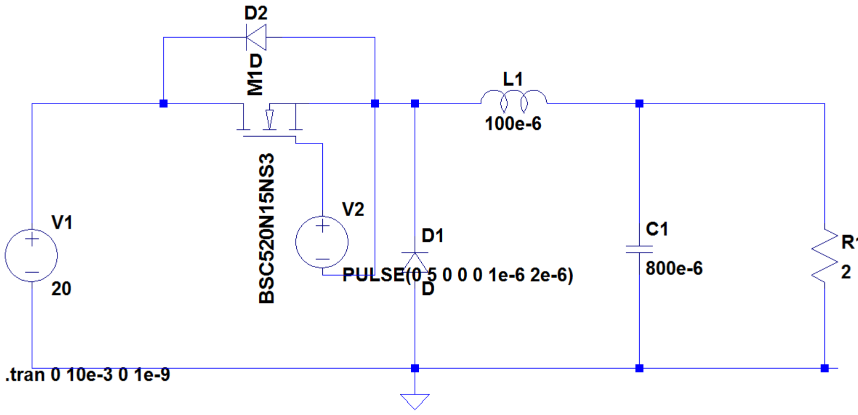

Figure3: simulation circuit of hard-switching buck converter.

The following table shows all the parameters we used in this simulation:

Table 1: parameters in the simulation of hard-switching buck converter

parameter	value	unit
V_1	20	V
L	100	μH
C	800	μF
R	2	Ω
D	0.5	
f_s	500	kHZ
MOSFET	BSC060N10NS3	

3.2 *ZVS QRC Buck converter:*

We built simulation circuit shown below:

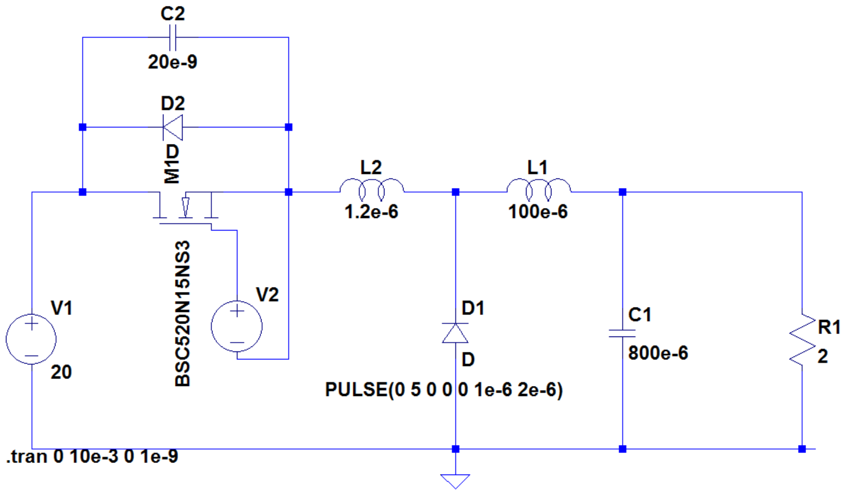

Figure 4: simulation circuit of ZVS QRC Buck converter

The following table shows all the parameters we used in this simulation:

Table 2: parameters in the simulation of ZVS QRC Buck converter

parameter	value	unit
V_1	20	V

L	100	μH
C	800	μF
Lr	1.2	μH
Cr	20	nF
R	2	Ω
D	0.5	
f_s	500	kHZ
MOSFET	BSC060N10NS3	

And since all the switching processes happen in nanoseconds, the maximum time step should be even smaller. In this simulation, we set the maximum time step as $5 \times 10^{-10} s$.

3. results and discussion:

4.1 hard-switching buck converter:

The switching waveform of the hard-switching buck converter is shown in the following figure. Since the switching process is really short time relative to the switching period, we divide it into two figure: the open waveform and the close waveform:

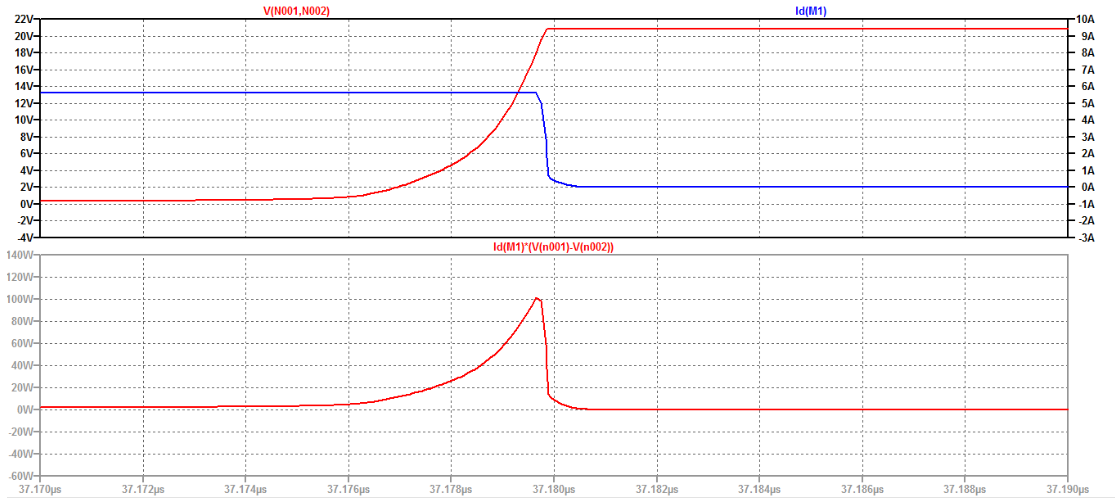

Figure 5: closing waveform and loss curve of the hard-switching buck convertor

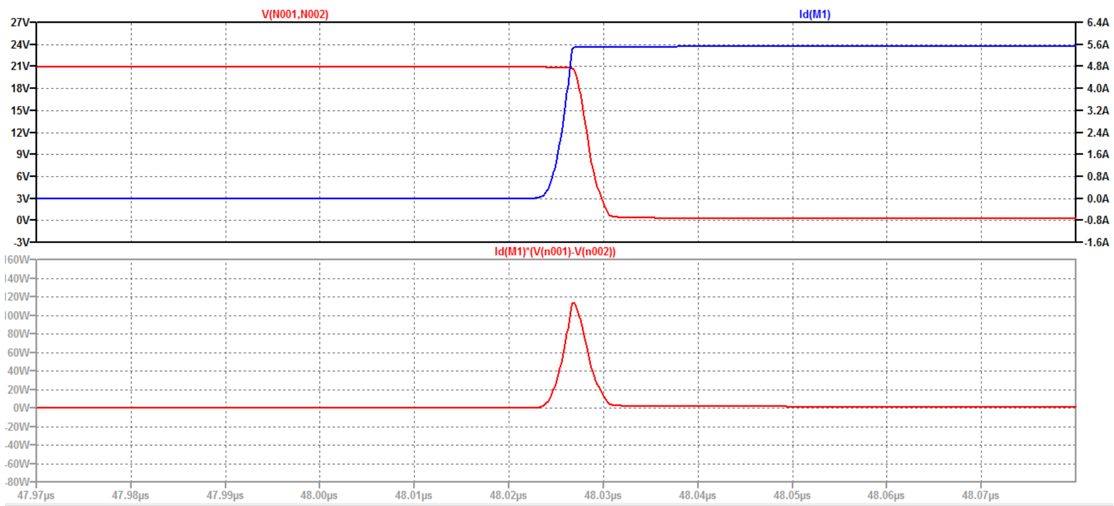

Figure 6: opening waveform and loss curve of the hard-switching buck convertor

It can be seen from the waveforms that the power and energy of the on and off losses are the most important. Compared with the on-state loss, the on-state loss and the off-state loss are relatively small, and the off-state loss is relatively small. The main reason is that when on and off overlap, the voltage and current are larger, while in the on and off states, the voltage and current are smaller. Moreover, since the resistance of the switch in the on state is also small, when the switch is in the off state, the voltage in the on state is greater than the leakage current, which causes the loss in the on state to be greater than the loss in the off state.

4.2 ZVS QRC Buck converter:

The switching waveform is shown in the following figure:

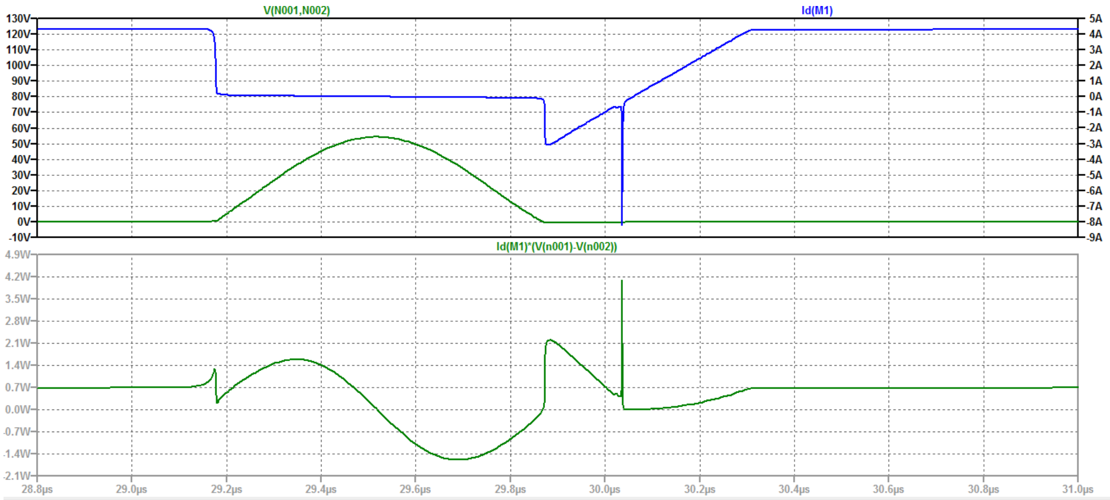

Figure 7: switching waveform and loss curve of ZVS QRC Buck converter.

The analysis is based on the off-time of the MOSFET as a starting point t_0. Before that, the MOSFET was on and the diode D1 was off. $u_{C_r} = 0$, $i_{C_r} = I_L$. I_L is the current of the inductor.

$t_0 \sim t_1$: The MOSFET is turned off, and the parallel capacitor Cr prevents the switching voltage from abruptly slowing down the switching voltage. After it is turned off, the diodes D1 and D2 are still under reverse voltage and are not turned on; the inductors Lr and L charge Cr at the same time. It can be regarded as a constant current source. Therefore, the Cr voltage rises linearly. The voltage between D1 reduce at the same time.

$t_2 \sim t_3$: Cr discharges to Lr, the current direction of Lr changes, the voltage of capacitor Cr continuously drops to Ui, the voltage of inductor Lr becomes zero, and its current reaches the reverse resonance peak.

$t_3 \sim t_4$: Lr charges Cr in the reverse direction, and the voltage of capacitor Cr continues to decrease until it decreases to zero. So far, diode D2 has not been turned on under reverse voltage.

$t_4 \sim t_5$: D2 is turned on, the voltage of capacitor Cr is clamped to zero by D2, and the voltage across Lr is Ui, and its current linearly decays to zero. The voltage across the switch is also 0 during this time, so it must be turned on during this time to reduce losses.

$t_5 \sim t_6$: The MOSFET has been turned on, the power supply voltage is added to Lr through the switch, the voltage across Lr is still Ui, and the current on it rises linearly until I_L, D1 is turned off, and the circuit returns to the on state.

4.3 *Loss data of both circuits:*

To compare the loss of both circuit, we measured the loss of different process in one cycle. The measured data is shown in the following table:

Table 2: loss of different process in one cycle

Process	Hard	Soft
Open	340.2nJ	280.5nJ
Close	145.4nJ	14.59nJ
Totol	1817nJ	882nJ

From the figure above, we can see that the loss of soft switching is smaller than the hard switching at all the process. It can be seen that various losses are basically reduced compared to hard switching. Because the voltage rises slowly when the switch is turned off, the product of the voltage and current overlap is small compared to the hard switch, and the power loss is also small; when the switch is turned on, the voltage drops to 0 in advance, and the voltage and current do not overlap. The natural loss is also very small; the reason for the increase in the off-state loss is that the switch contains a junction capacitor during the off-state, and the current is not 0. Although the capacitor itself is only performing reactive conversion, no loss will occur, but the current during the conversion The existence of the small resistor in the switch will still generate a certain loss, but the total loss is significantly smaller than the total loss of the hard switch, indicating that the soft switch has good loss reduction characteristics.