Dinesh Reddy

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Experience

CAD Design Engineer Jun 2019 - Jul 2021
Xilinx *Hyderabad, India*

- **Workspace Infrastructure**:
  - Migrated perforce workspace-utilities from Perl to Python and introduced new crucial features like **logging**.
  - Reduced DB rendering utilities run-times from **11 hours to 45 minutes**.
  - Implemented **regression infrastructure** scripts that automated bi-weekly CAD releases.
- **Seras**: An in-house Design Automation Platform.
  - A key team member in implementing **POC** of the platform's efficacy in PnR environment to support 100s of tasks.
  - Provided regular feedback and advise for the platform's development towards 'Synthesis Placement & Routing' (PnR) design flow.
  - Enabled the design teams to compare tools across vendors, Synopsys and Cadence.
- **Excite**: Automating project updates to dashboard
  - Extracted key design metrics in pre and post Synthesis and aggregated them into a MongoDB.
  - The metrics include parsing logs, scanning LEF/DEF files, sanity checking of blocks between runs.

Research Internship May 2018 - Jul 2018
Professor: Virendra Singh *CADSL, IIT Bombay*

- **IITB-RISC ISA in Verilog**: Implemented **Multicycle** and **Pipeline** micro-architectures.
- **Deep Learning Acceleration**: Analyzed Approximate Computing, Hybrid Memory Architecture, Systolic Array Matrix Multiplication techniques.

Teaching Experience Aug 2021 - now
Graduate Teaching Assistant *UT Austin*

- Introduction to Embedded Systems **(EE319K)**, Digital Logic Design **(EE316)**, Introduction to Scientific and Technical Computing **(SDS335)**

Skills Summary

Proficient: C++, Python, Tcl, Verilog, Git, Linux, Vim, Gdb.
Intermediate: Perl, Bash, Perforce, Vivado, LSF, Lynx, Synopsys' Design Compiler.

Projects

SOC Design: Darknet Yolo Deep Learning Application on FPGA UT Austin
Professor: Andreas Gerstlauer *Aug 2021 - Dec 2021*

- **Tiny-Yolo on PS**: Improved inference time from 11s to 6s with OpenMp and Fixed-Point computations.
- **HW-SW co-simulation in SystemC**: Integrated a simulated GEMM into QEMU-SystemC environment to run Tiny-yolo.
- **Vivado HLS**: Synthesized a memory-partitioned run-time-optimized GEMM accelerator.
- **HW-SW co-design on Zynq-ultra96**: Integrated the synthesized GEMM accelerator to run Tiny-yolo on ZynqUltra96. The design achieved an inference time of 16s.

Computer Architecture UT Austin
Professor: Dam Sunwoo *Aug 2021 - Dec 2021*

- **Labs**: Assembler for LC3B ISA, LC3B simulator, Cycle level simulator, Interrupts and Exception support, Virtual Memory support, Pipeline simulator.
- **Project**: Performance analysis of RRIP cache replacement policy in GEM5 simulator.

Technology for Embedded IOT UT Austin, TX
Professor: Jonathan Valvano *Aug 2021 - Nov 2021*

- **subGHz using the HC-12 with MSP432**: Implemented communication protocol in a static environment with multiple devices communicating.
- **TinyML on Arduino-nano**: Speech recognition was used to play Tic-tak-toe game on the board.

Awards and Achievements

- **Emerging Star** of FPGA product development department, Q4 2020, for Seras and Excite development.
- **Above and beyond** team-award, Q4 2021, for enabling Innovus integration into Seras.

Education

University of Texas at Austin Austin, USA
Masters in ECE *Aug 2021 - now*

- **Architecture Computer Systems and Embedded Systems** 3.66/4
  Relevant Courses: *Computer Architecture, System-On-Chip Design, Embedded and RTOS lab, Ml/Data Analytics for Edge AI*

Indian Institute of Technology Hyderabad Hyderabad, India
Bachelor of Technology *Aug 2015 - Apr 2019*

- **Electrical Engineering, Double major in Compuer Science Engineering** 8.65/10
  Relevant Courses: *FPGA Lab, Advanced Digital IC Design, Advanced Embedded Systems, Microprocessors, Advanced Computer Architecture, Data Structures, Algorithms, Applied Machine Learning, Operating Systems.*