Dinesh Reddy

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Experience

- **Xilinx** — Hyderabad, India
  CAD Design Engineer — *Jun 2019 - Jul 2021*
  - **Seras – An in-house Design Automation Platform**: Driven the development of the platform from early stages by validating new features, debugging and fixing issues to eventually support 'Synthesis Placement & Routing' design flow. The infrastructure enabled the design teams to compare tools across vendors.
  - **Excite: Automating project updates to dashboard**: Wrote TCL scripts to extract key design metrics in pre and post Synthesis from blocks and aggregated them in a MongoDB. The aggregated data was used to generate dashboards to track project progress by design teams and upper management.
  - **Infrastructure Development and Support**: Implemented and maintained Python, Perl, and TCL scripts for creating and managing Perforce work-space. The infrastructure was used by every PnR design engineer in a day-to-day environment. Implemented regression scripts in Python that eased the task of validating tools in our biweekly CAD releases.
- **CADSL lab, IIT Bombay** — Professor: Virendra Singh
  Research Internship - Computer Architecture — *May 2018 - Jul 2018*
  - **Processor Design in Verilog HDL**: Implemented Multicycle (Github link) and Pipeline (Github link) micro-architectures for IITB-RISC ISA.

Skills Summary

- **Languages**: C++, Python, Perl, Tcl, Verilog, Bash, Git, Perforce, Vivado, Linux, Vim, IBM Spectrum LSF, Docker, QEMU*, Lynx, Synopsys' Design Compiler*, (* beginner).

Projects

- **SOC Design: Darknet Yolo Deep Learning Application on FPGA (link)** — UT Austin
  Professor: Andreas Gerstlauer — *Aug 2021 - Dec 2021*
  - **Lab1 (link)**: Profiled Darknet-Yolo application for computationally expensive bottlenecks on ARM CPU in Zynq Ultra96 Xilinx board. Identified GEMM operations to be taking 90% of the compute resources. Optimized the application with OpenMp threads and Fixed-Point computations.
  - **Lab2 (link)**: Partitioned the Darknet application code into software on the ARM and external hardware accelerator. Prototyped the target design in a QEMU-SystemC environment.
  - **Lab3 (link)**: Used Xilinx's Vivado high-level synthesis (HLS) tool to synthesize and validate GEMM accelerator, and generated Verilog for FPGA deployment. Explored various architectural alternatives for HLS.
  - **Project (link)**: Integrated and optimized the Darknet-YOLO application on the ARM+FPGA board. Our design achieved performance comparable to that of CPU.
- **Computer Architecture (link)** — UT Austin
  Professor: Dam Sunwoo — *Aug 2021 - Dec 2021*
  - **Labs**: Assembler for LC3B ISA, LC3B simulator in C, Cycle level simulator for the ISA, Interrupts and Exception handling support, Virtual Memory support.
  - **Project**: Analyzed the RRIP cache replacement on different benchmarks in GEM5 simulator.
- **Tic-Tac-Toe game on FPGA (link)** — IIT Hyderabad
  Professor: GVV Sharma — *Jan 2019 - Mar 2019*
  - **Project**: Designed and implemented the game on ICO embedded FPGA board. A PCB was also interfaced for aesthetics.

Education

- **University of Texas at Austin** — Austin, USA
  Masters in ECE — *Aug 2021 - now*
  - **Architecture Computer Systems and Embedded Systems**
    Courses: *Computer Architecture, System-On-Chip Design, Technology for Embedded IOT, Embedded and RTOS lab, Advanced Algorithms*
- **Indian Institute of Technology Hyderabad** — Hyderabad, India
  Bachelor of Technology — *Aug 2015 - Apr 2019*
  - **Electrical Engineering, Double major in Compuer Science Engineering**
    Relevant Courses: *FPGA Lab, Advanced Digital IC Design, Advanced Embedded Systems, Microprocessors, Advanced Computer Architecture, Data Structures, Algorithms, Applied Machine Learning, Operating Systems.*

Achievements

- **Xilinx**: Emerging Star of FPGA product development department, 2020, for Seras and Excite development.
- **Xilinx**: Above and beyond team-award, 2021, for enabling Innovus integration into Seras.

Teaching Experience

- Teaching Assistant: Introduction to Embedded Systems, Digital Logic Design, and Introduction to Scientific and Technical Computing.