Dinesh Reddy

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Experience

- **CAD Design Engineer** — Jun 2019 - Jul 2021
  Xilinx — *Hyderabad, India*
  - **Seras**: An in-house Design Automation Platform.
    - Sole person in validating new features.
    - Driven the development debugging issues to eventually support 'Synthesis Placement & Routing' design flow.
    - Enabled the design teams to compare tools across vendors, Synopsys and Cadance.
  - **Excite**: Automating project updates to dashboard
    - extracted key design metrics in pre and post Synthesis and aggregated them into a MongoDB.
    - The metrics include parsing logs for errors, scanning LEF/DEF files, sanity checking of blocks between runs.
  - **Work-space Infrastructure**:
    - Upgraded utilities for creating and managing workspaces from Perl to Python.
    - The new logging mechanism proved effective among the multiday run-time environment.
    - Identified issues and improved the run-times of the utilities by 10-fold.
    - Around 200 PnR design engineers use the utilities.
  - **Regression Infrastructure**:
    - Implemented regression scripts in Python.
- **Research Internship** — May 2018 - Jul 2018
  Professor: Virendra Singh — *CADSL, IIT Bombay*
  - **IITB-RISC ISA in Verilog**: Implemented Multicycle and Pipeline micro-architectures.
  - **Deep Learning Acceleration**: Studied Approximate Computing, Hybrid Memory Architecture, Systolic Array Matrix Multiplication techniques.

Skills Summary

- **Proficient**: C++, Python, Tcl, Verilog, Git, Linux, Vim.
- **Intermediate**: Perl, Bash, Perforce, Vivado, LSF, Lynx.
- **Beginner**: Docker, QEMU, Synopsys' Design Compiler.

Projects

- **SOC Design: Darknet Yolo Deep Learning Application on FPGA** — UT Austin
  Professor: Andreas Gerstlauer — *Aug 2021 - Dec 2021*
  - **Lab1**: Optimized Darknet's tiny-Yolo with OpenMp threads and Fixed-Point GEMM computations took 6s (11s is the benchmark time).
  - **Lab2**: Implemented SW-HW co-design in a QEMU-SystemC environment.
  - **Lab3**: Synthesized a run-time-optimized GEMM accelerator using Xilinx's Vivado-hls.
  - **Project**: Integrated and optimized the Darknet-YOLO application on the ARM+FPGA board. Our design achieved performance comparable to that of CPU.
- **Computer Architecture** — UT Austin
  Professor: Dam Sunwoo — *Aug 2021 - Dec 2021*
  - **Labs**: Assembler for LC3B ISA, LC3B simulator, Cycle level simulator, Interrupts and Exception support, Virtual Memory support.
  - **Project**: Performance analysis of RRIP cache replacement in GEM5 simulator.
- **Tic-Tac-Toe game on FPGA** — IIT Hyderabad
  Professor: GVV Sharma — *Jan 2019 - Mar 2019*
  - **Project**: Designed and implemented the game on ICO embedded FPGA board. Among the two projects selected for extension to real product.

Industry Achievements

- **Emerging Star** of FPGA product development department, Q4 2020, for Seras and Excite development.
- **Above and beyond** team-award, Q4 2021, for enabling Innovus integration into Seras.

Education

- **University of Texas at Austin** — Austin, USA
  Masters in ECE — *Aug 2021 - now*
  - **Architecture Computer Systems and Embedded Systems**
    Relevant Courses: *Computer Architecture, System-On-Chip Design, Embedded and RTOS lab, Ml/Data Analytics for Edge AI*
- **Indian Institute of Technology Hyderabad** — Hyderabad, India
  Bachelor of Technology — *Aug 2015 - Apr 2019*
  - **Electrical Engineering, Double major in Compuer Science Engineering**
    Relevant Courses: *FPGA Lab, Advanced Digital IC Design, Advanced Embedded Systems, Microprocessors, Advanced Computer Architecture, Data Structures, Algorithms, Applied Machine Learning, Operating Systems.*

Teaching Experience

- Teaching Assistant at UT: Introduction to Embedded Systems **(EE319K)**, Digital Logic Design **(EE316)**, and Introduction to Scientific and Technical Computing **(SDS335)**.