2EC501-VLSI DESIGN

SPECIAL ASSIGNMENT

TOPIC: 2 Bit binary to Gray code converter

Submitted by:

NAME	ROLL NO.
CHIRAG RAJWANI	*21BEC021*

Submitted to:

Prof. Usha Mehta

Prof. Jayesh Patel

Department of Electronics &Communications Engineering, IT-NU

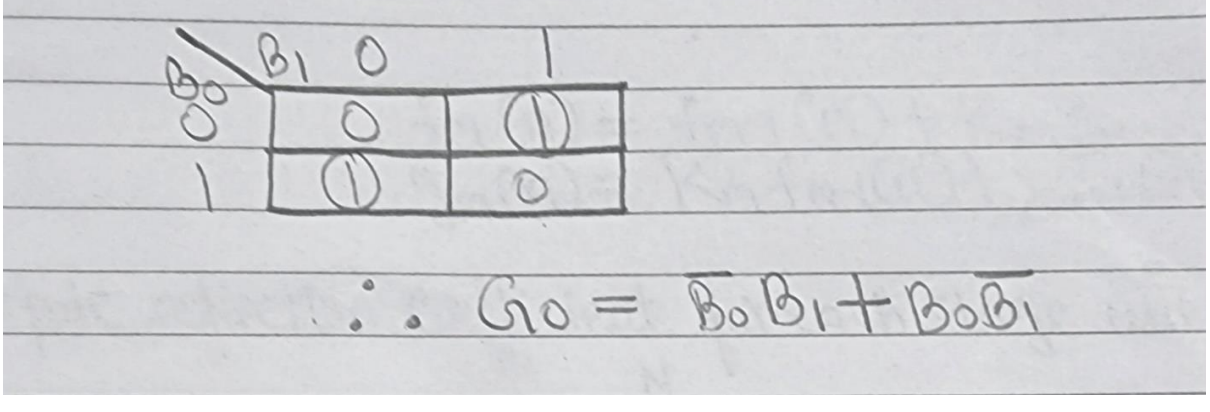
❖GATE LEVEL circuit diagram & Boolean equation for 2 bit binary to Gray code converter:-

Binary	Gray

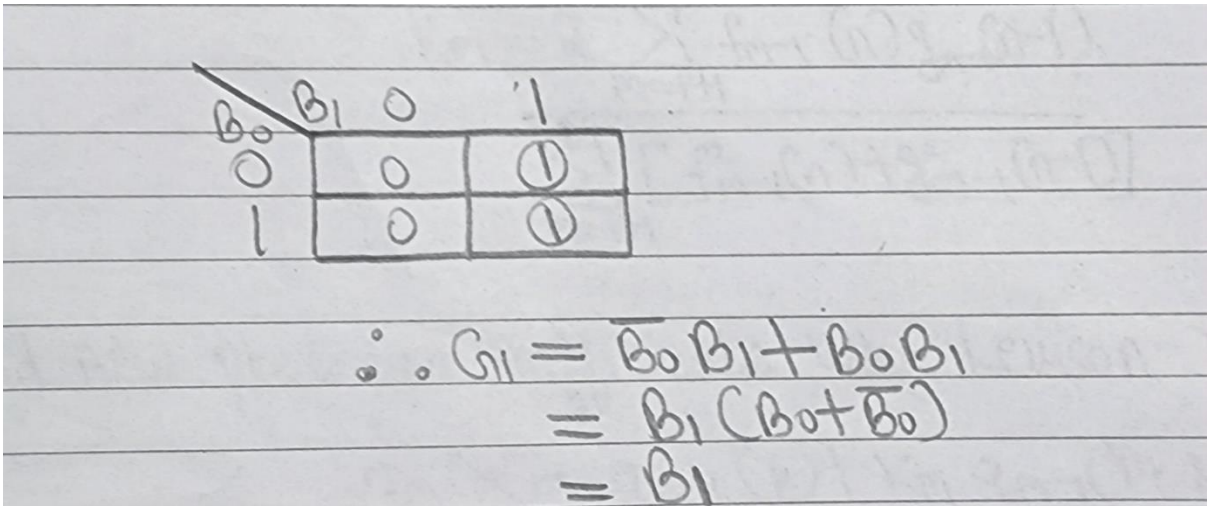
B0	B1	G0	G1
0	0	0	0
1	0	1	0
0	1	1	1
1	1	0	1

❖ To find the corresponding digital circuit, I will use the K-Map technique for each of the Gray code bits as output with all of the binary bits as input;

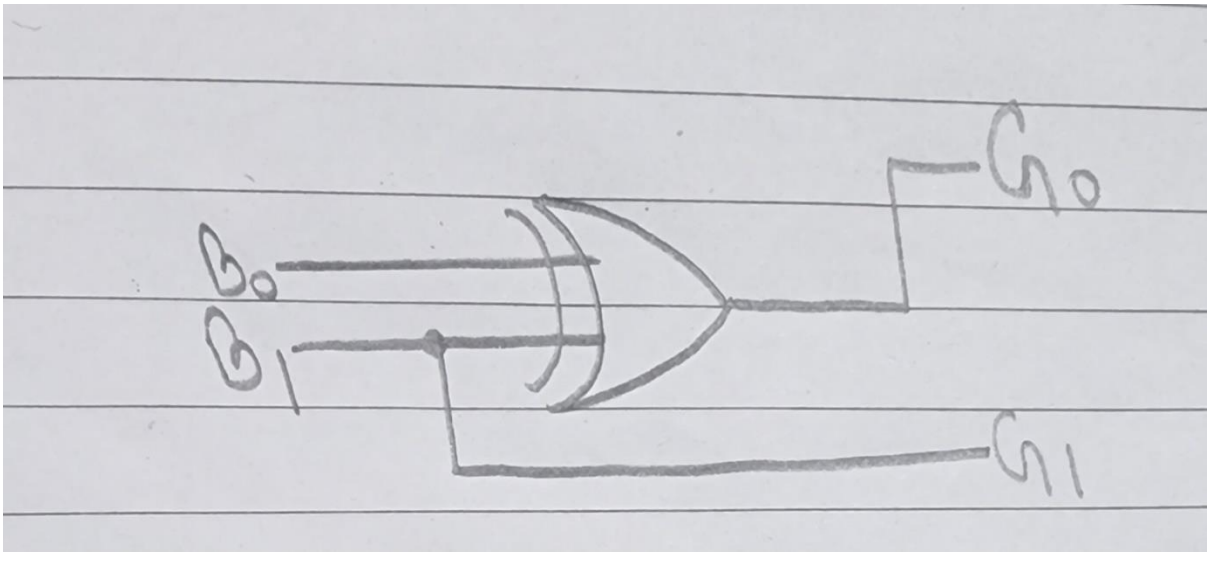
For G0→



For G1→



Therefore the optimized gate level circuit diagram obtained is:-



- Now the transistor level schematic diagram for a CMOS inverter circuit implementation is to be drawn, requiring;
  - Optimized calculation for total no. of transistors to be used:

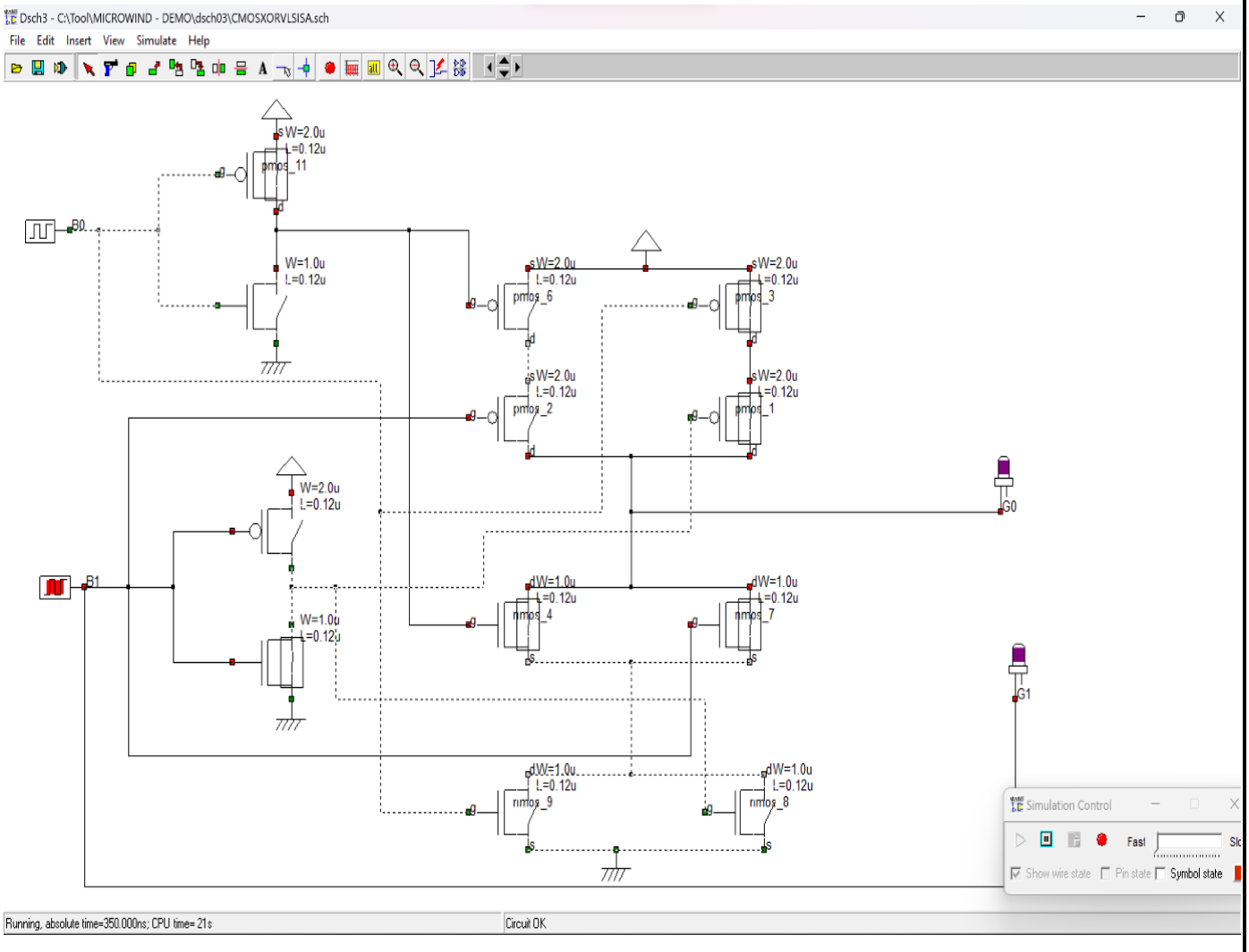
Total number of inputs to be given into the circuit;

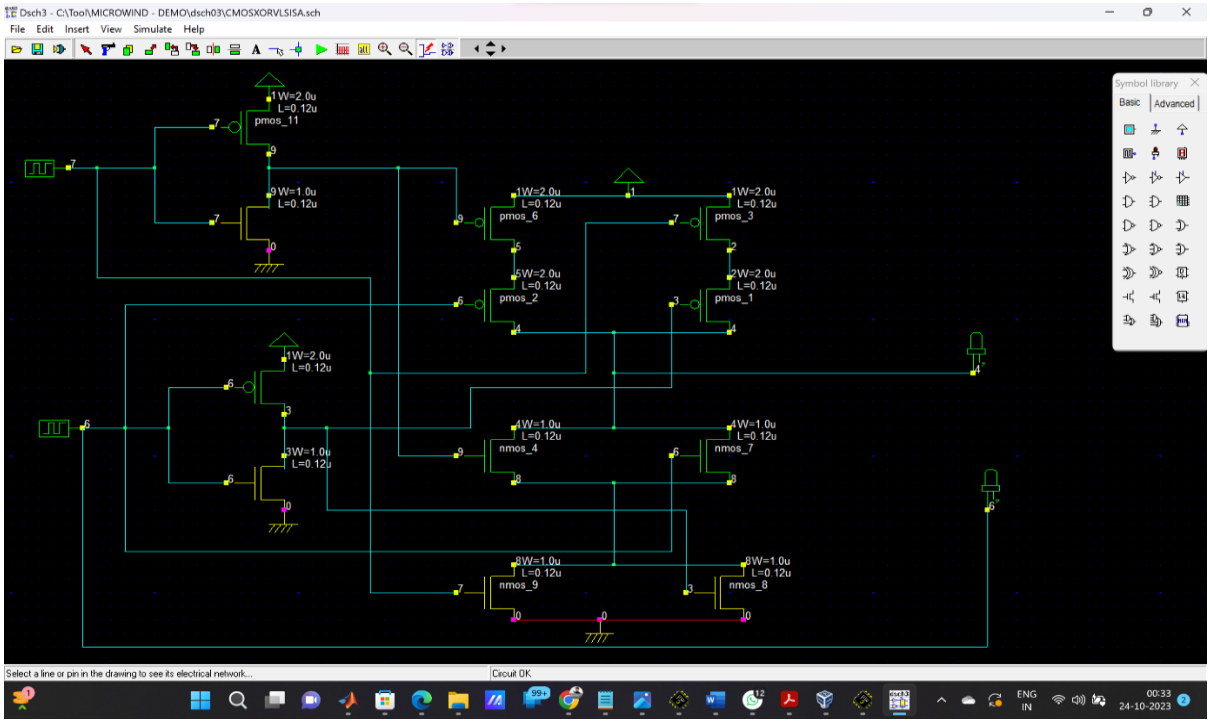
- B0
- B1
- B0
- B1

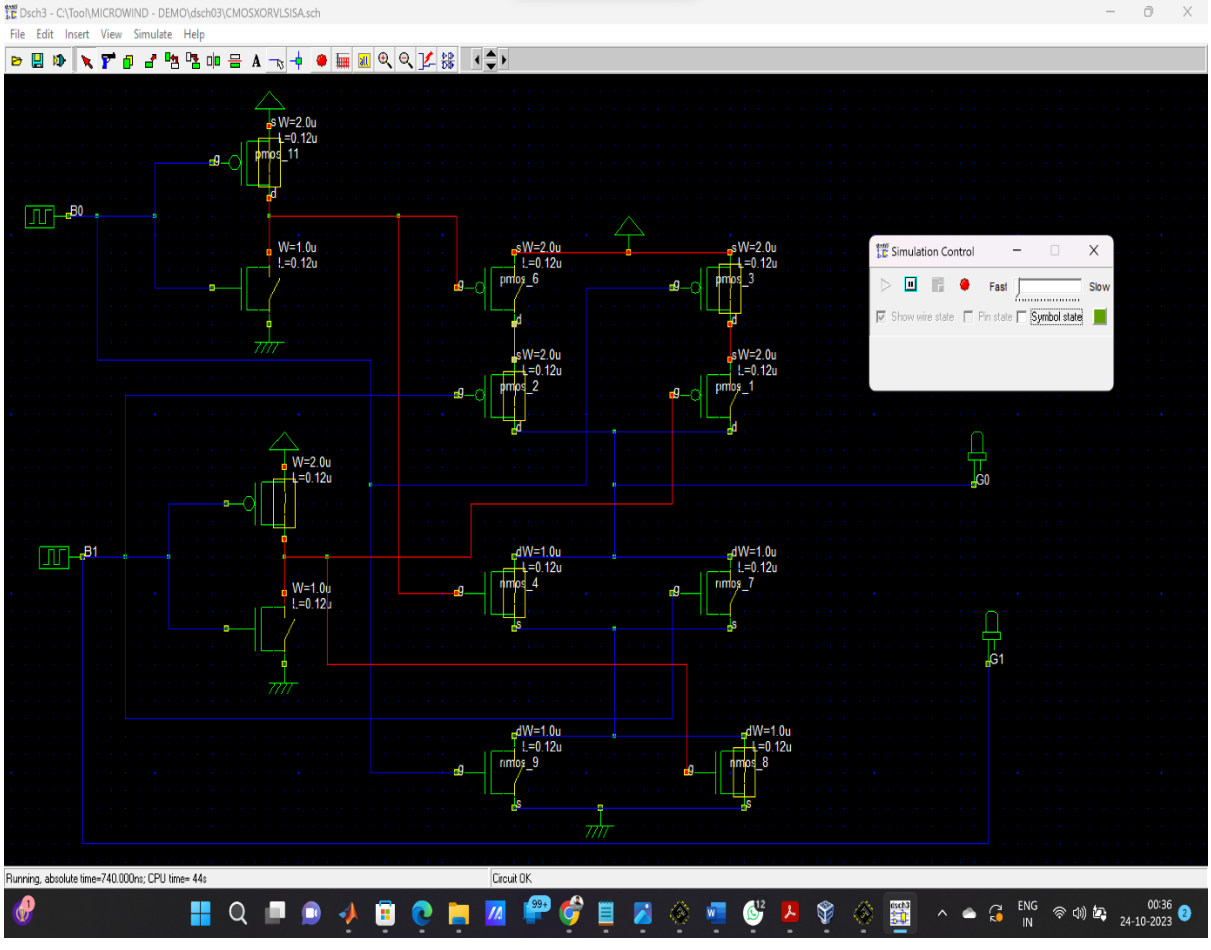
And also assuming that both the inputs are only available in normal form and none is available in complement form.

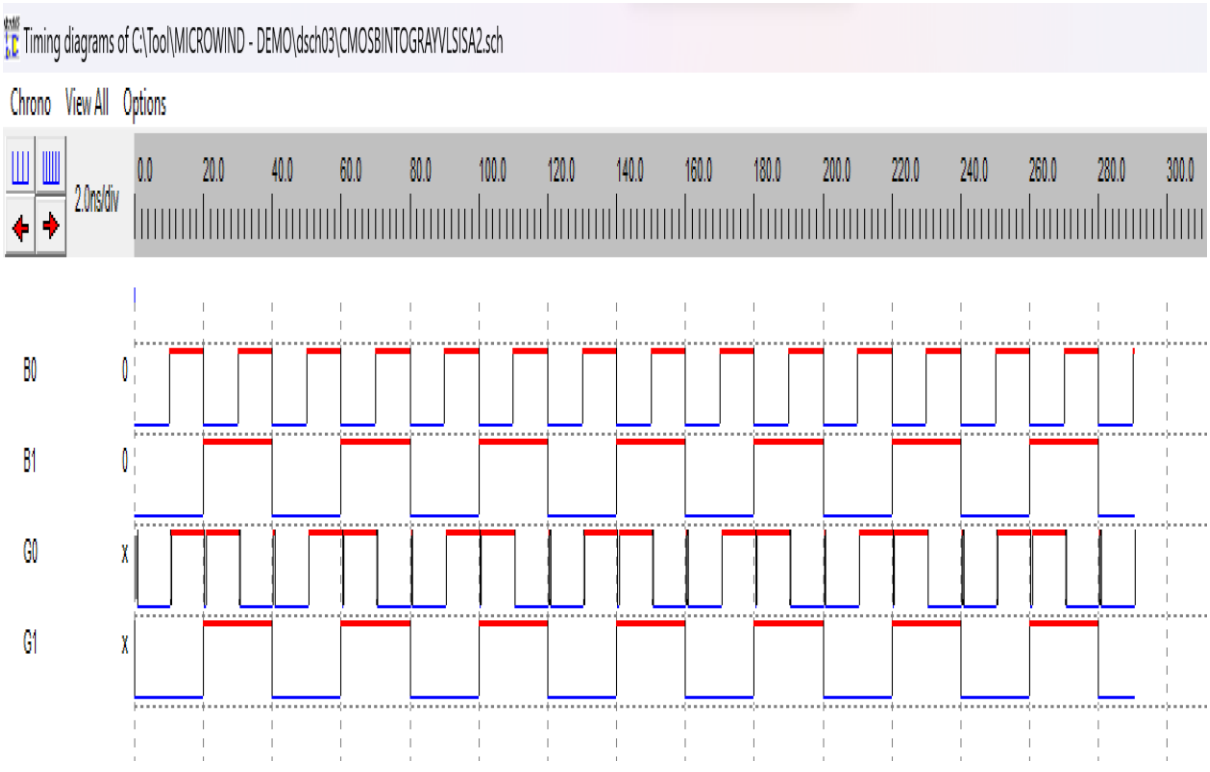
Thus, 4 transistors are required for the mentioned four inputs each in pull up & pull down network, alongside which 4 extra transistors are required as to form an inverter for attaining the complemented form.

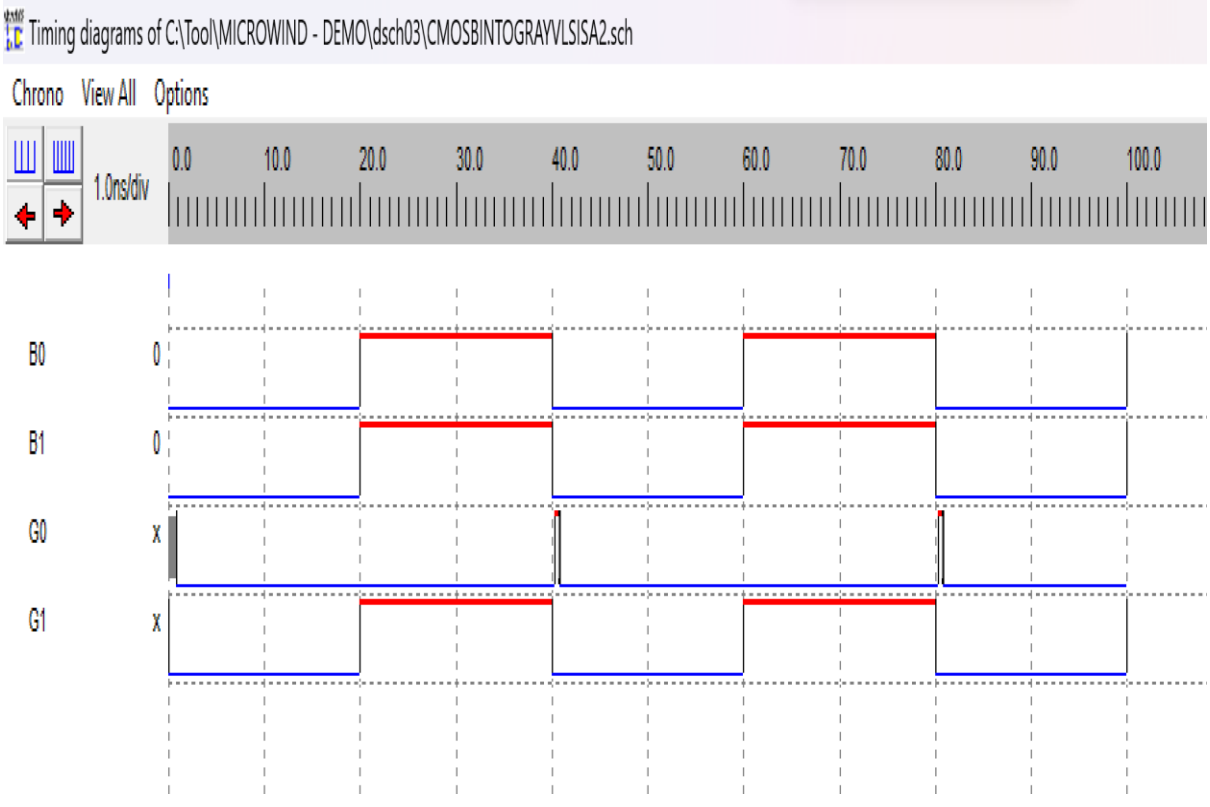
Therefore, 12 transistors are required in total to fabricate the transistor level schematic, such as;




Dsch3 - C:\Tool\MICROWIND - DEMO\dsch03\CMOSXORVLSISA.sch
File Edit Insert View Simulate Help
Symbol library
Basic Advanced
pmos_11
pmos_6
pmos_3
pmos_2
pmos_1
nmos_4
nmos_7
nmos_9
nmos_8
Select a line or pin in the drawing to see its electrical network...
Circuit OK
ENG IN
00:33
24-10-2023


Dsch3 - C:\Tool\MICROWIND - DEMO\dsch03\CMOSXORVLSISA.sch
File Edit Insert View Simulate Help
Simulation Control
Fast
Slow
Show wire state
Pin state
Symbol state
B0
B1
G0
G1
pmos_11
pmos_6
pmos_3
pmos_2
pmos_1
nmos_4
nmos_7
nmos_9
nmos_8
Running, absolute time=740.000ns; CPU time= 44s
Circuit OK
ENG IN
00:36
24-10-2023

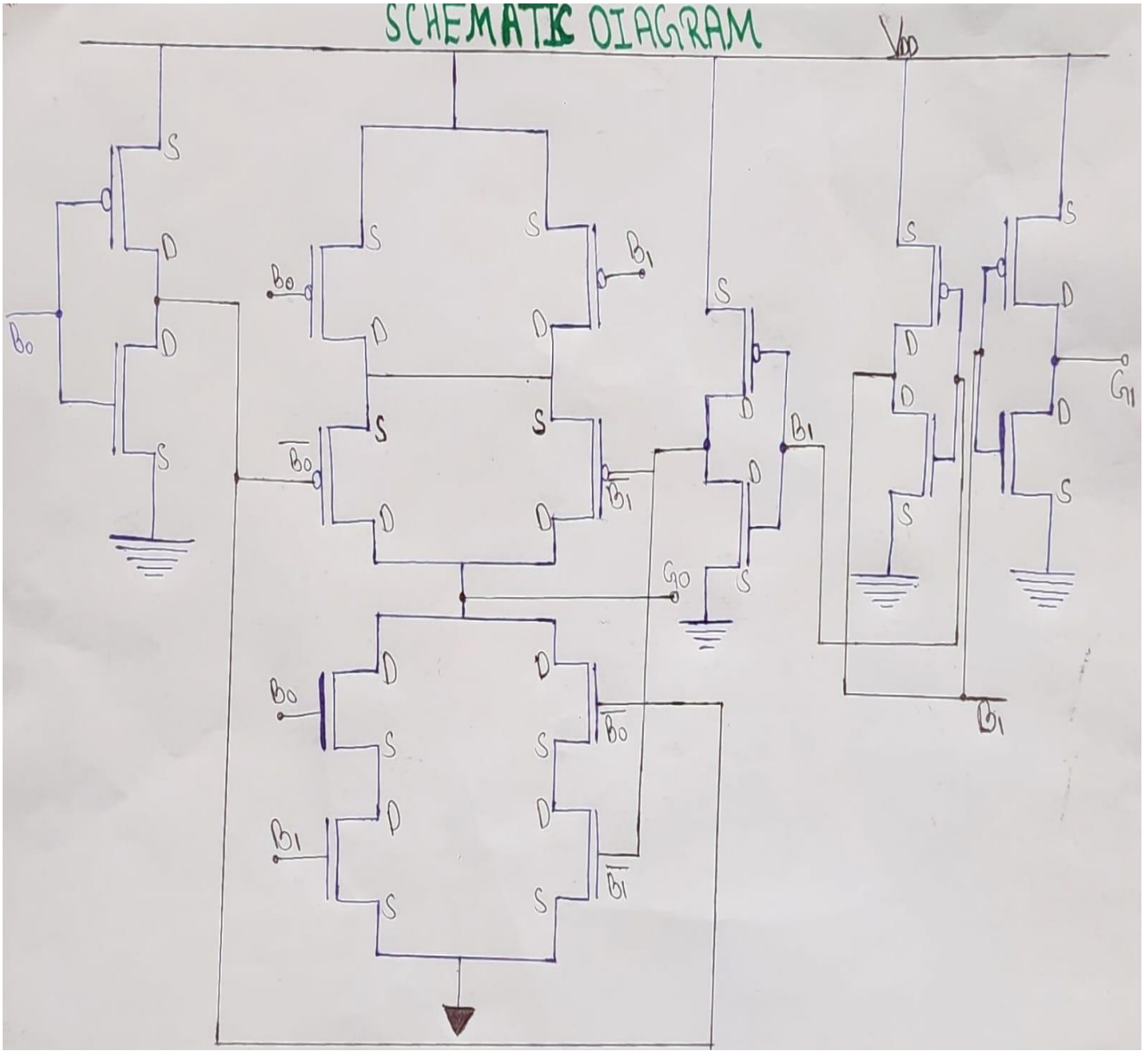

Timing diagrams of C:\Tool\MICROWIND - DEMO\dsch03\CMOSBINTOGRAYVLSISA2.sch
Chrono View All Options
2.0ns/div
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 180.0 200.0 220.0 240.0 260.0 280.0 300.0
B0
B1
G0
G1
0
0
x
x


Timing diagrams of C:\Tool\MICROWIND - DEMO\dsch03\CMOSBINTOGRAYVLSISA2.sch
Chrono View All Options
1.0ns/div
0.0 10.0 20.0 30.0 40.0 50.0 60.0 70.0 80.0 90.0 100.0
B0
B1
G0
G1
0
0
x
x

❖ Stick diagram for the same could be drawn out in the following manner :-

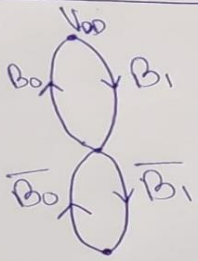
Colour code being followed is as shown below→

Part	Color
PMOS	Yellow
NMOS	Green
GND, *V*dd	Blue
Inputs	Red
Connectors	Dot



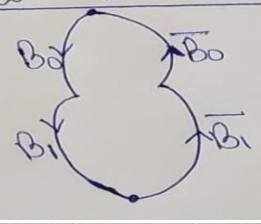
EULER'S PATH

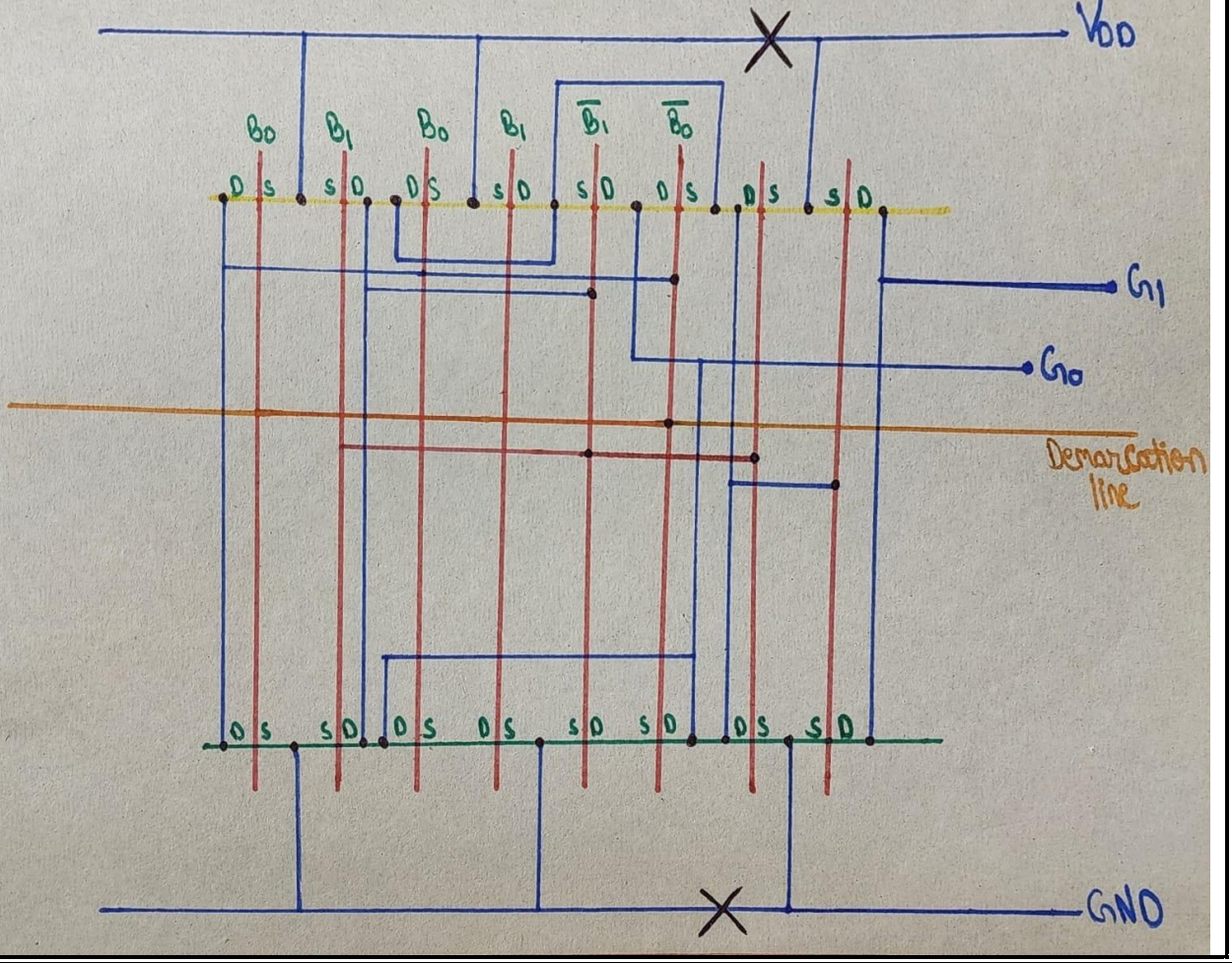
Pull up Network



COMMON PATH :- $B_0 B_1 \overline{B_1} \overline{B_0}$

Pull down Network





❖ State the various levels of $\boldsymbol{VOL}$ corresponding to various transistor states.

ANS. The levels of voltage (VOH and VOL) for each transistor state would depend on the specific technology used, but generally, they would correspond to logical high (1) and logical low (0) levels for the binary and Gray code values. Here is a basic representation of the transistor states for a 2-bit binary to Gray code converter:

Binary input	Gray output	Transistor 1	Transistor 2
00	00	OFF (Vol)	OFF(Vol)
01	01	ON(Voh)	OFF(Vol)
10	11	OFF(Vol)	ON(Voh)
11	10	ON(Voh)	ON(Voh)

Here, Vol is the low voltage level (logical 0). When Transistor 1 is ON, it represents a binary 1, and when it's OFF, it represents a binary 0. Similarly, Transistor 2 represents the second bit's state in the binary code.

❖ Find the equivalent CMOS inverter circuit.

→In the circuit which I have designed; for the optimum output, the (W/L)equivalents for PMOS & NMOS are as follows respectively:-

(W/L)eq.=(140λ/6 λ)=(14*0.600/6*0.06) μm

(W/L)pmos=(78λ/6 λ)=(7.8*0.600/6*0.06)μm

(W/L)nmos=(62λ/6 λ)=(6.2*0.600/6*0.06)μm

Therefore, (W/L)pmos=**0.5571**(W/L)eq.
(W/L)nmos=**0.4428**(W/L)eq.

❖ For CMOS/MOS implementation, which input patterns give the lowest output resistance when output is low? What is the value of that resistance?

ANS. For the following input patterns output is low:-

B0	B1	G0
1	1	0
0	0	0

Here, in both the cases assuming that the transistors have been sized to give a worst-case output resistance of 20 KΩ; the lowest output resistance turns out to be **80KΩ**.
And, in case of G1; the lowest output resistance turns out to be **20KΩ**
for the input pattern of B1=0, for which G1 is low.

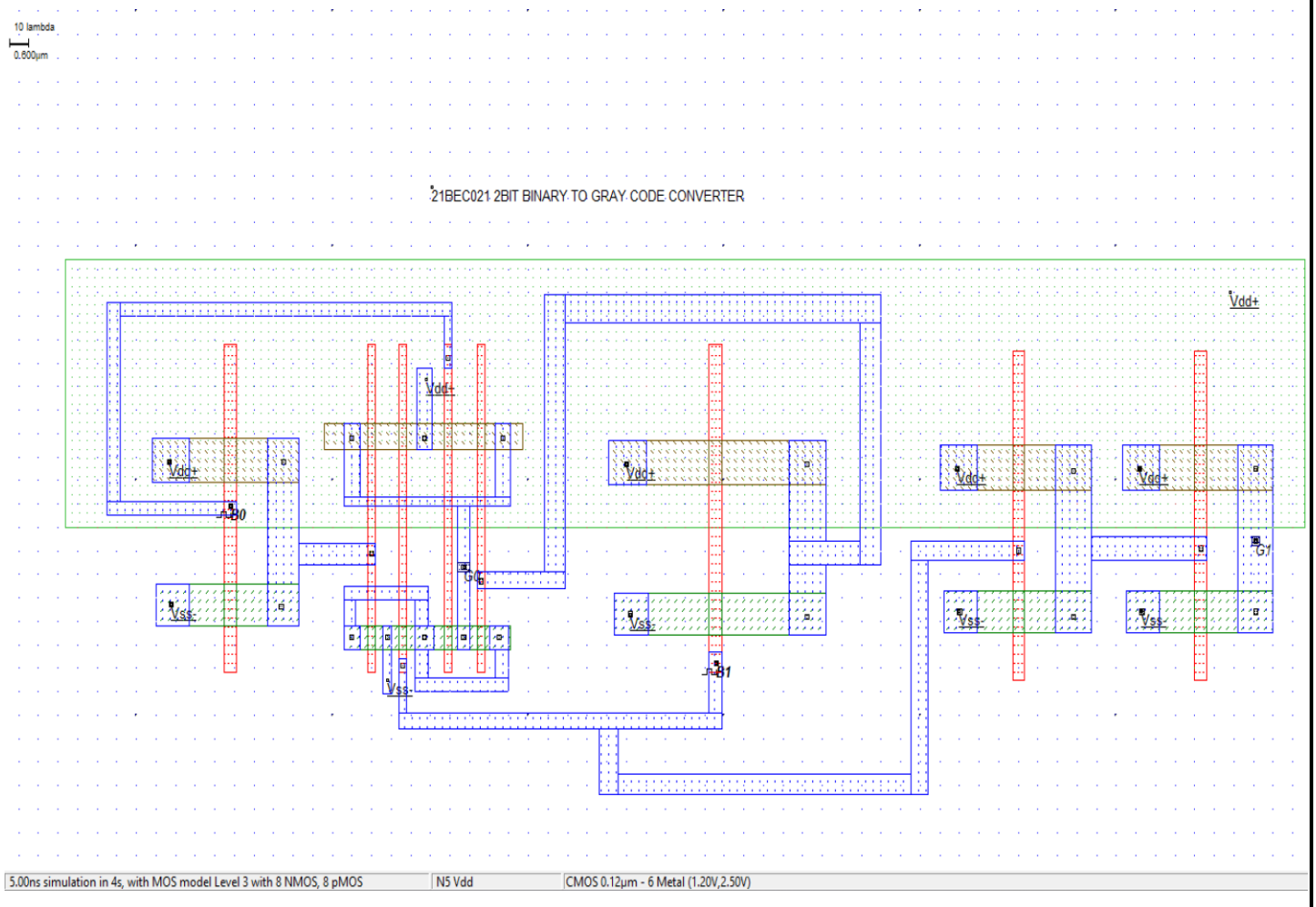
❖ For CMOS/MOS implementation, which input patterns give the lowest output resistance when output is low? What is the value of that resistance?

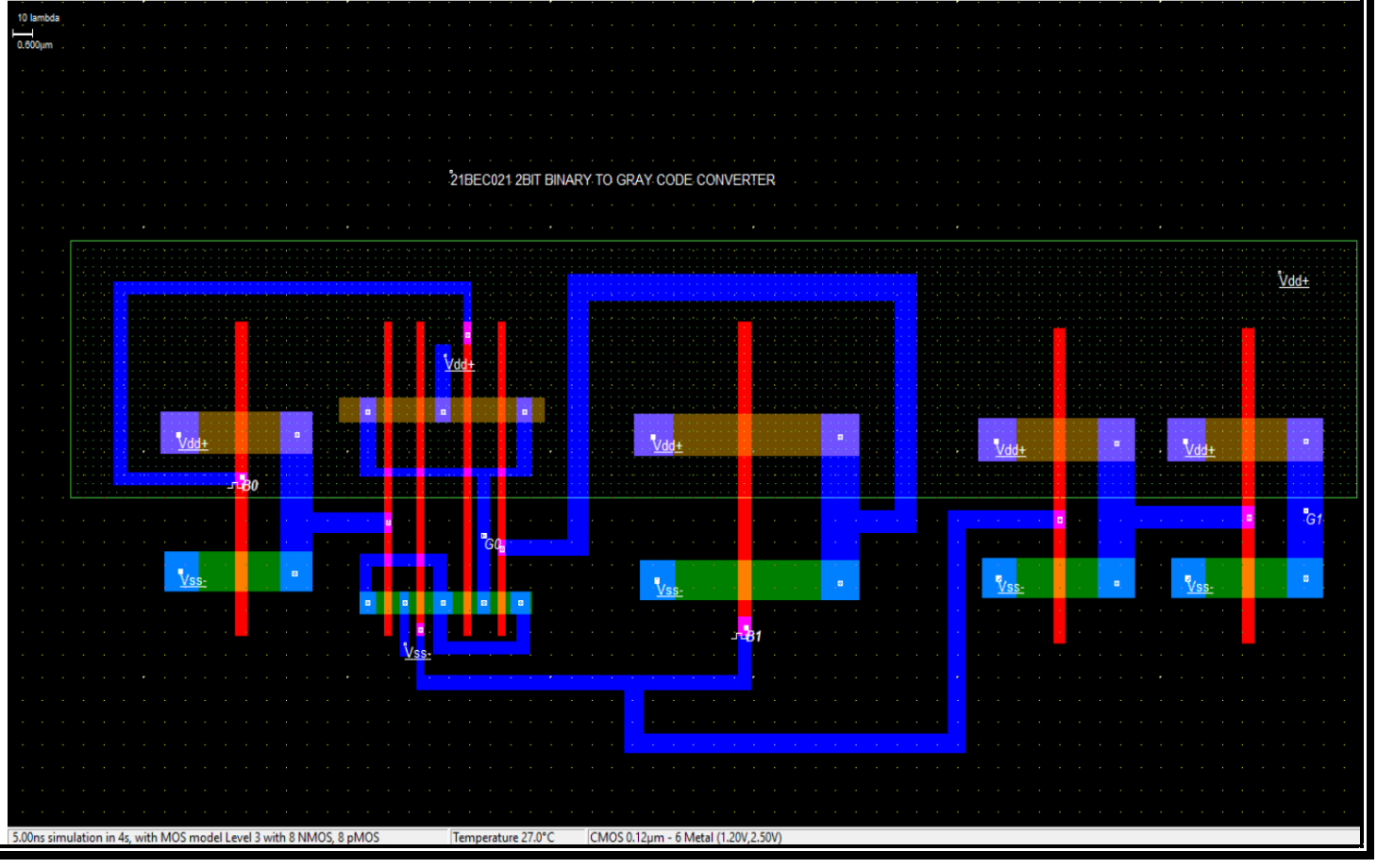
ANS. For the following input patterns output is high :-

B0	B1	G0
1	0	1
0	1	1

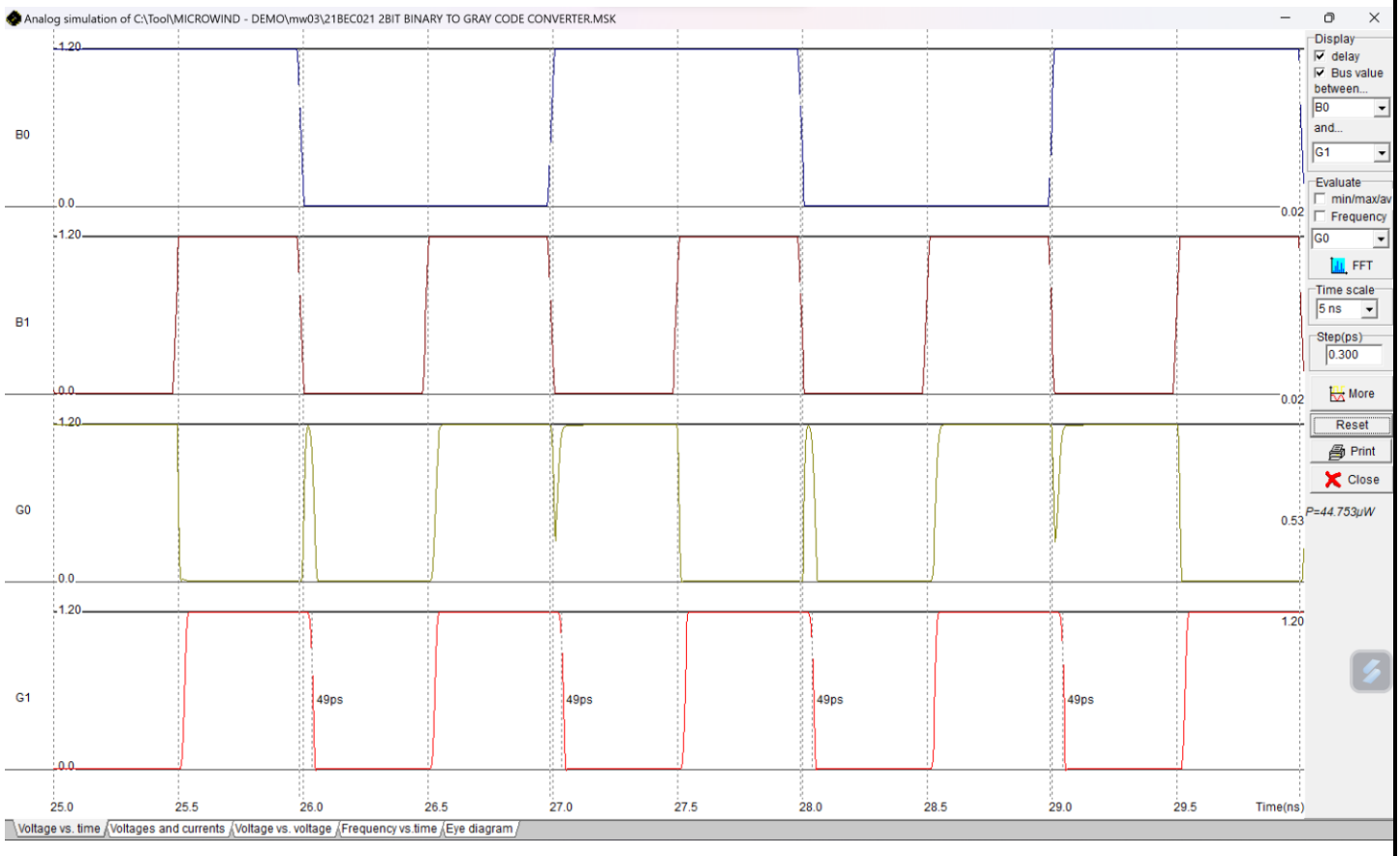
Here, in both the cases assuming that the transistors have been sized to give a worst-case output resistance of 20 KΩ; the lowest output resistance turns out to be **20KΩ.**
And, in case of G1 also; the lowest output resistance turns out to be **20KΩ**
for the input pattern of B1=1, for which G1 is high.

❖ Prepare the layout using MICROWIND tool.

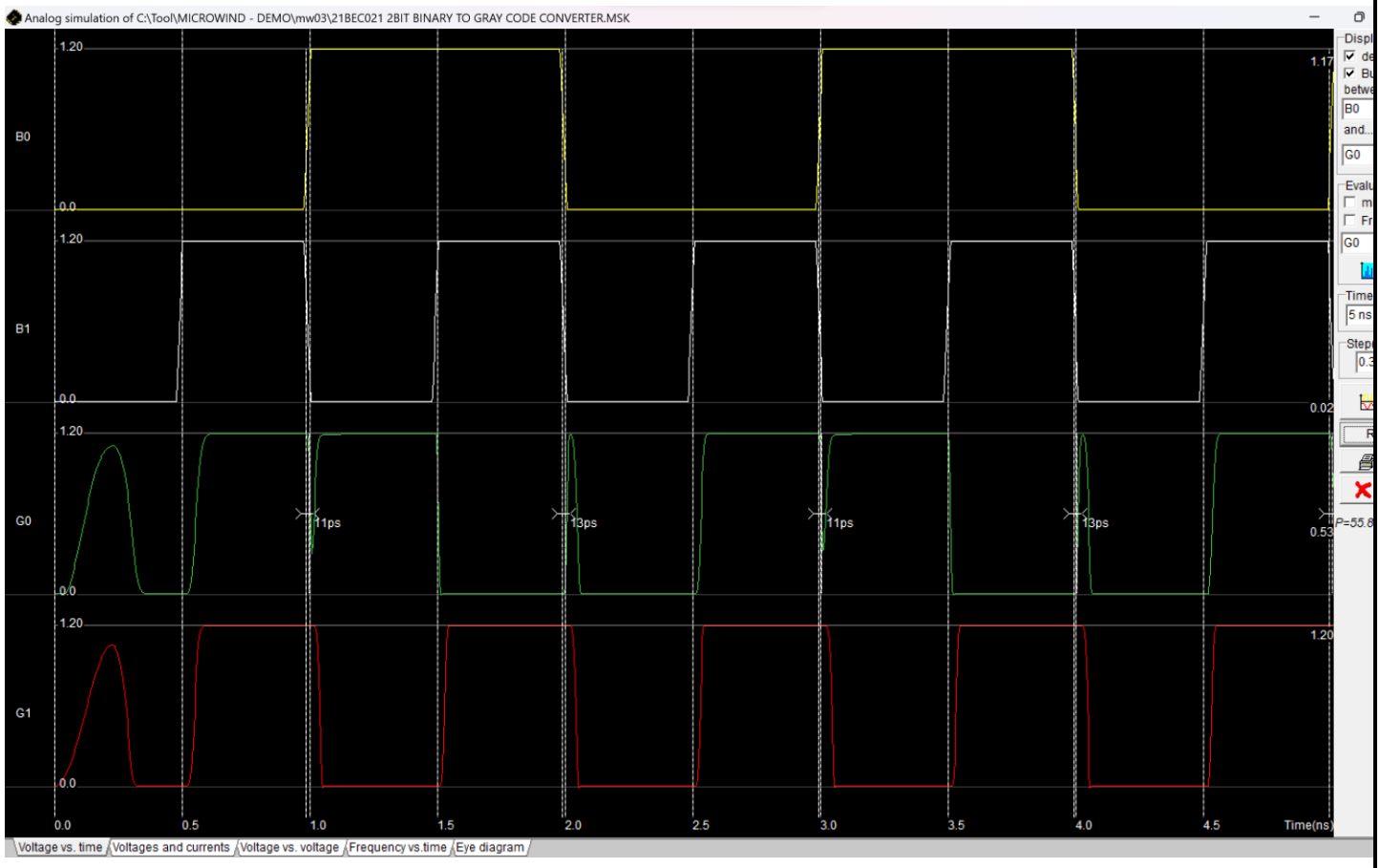




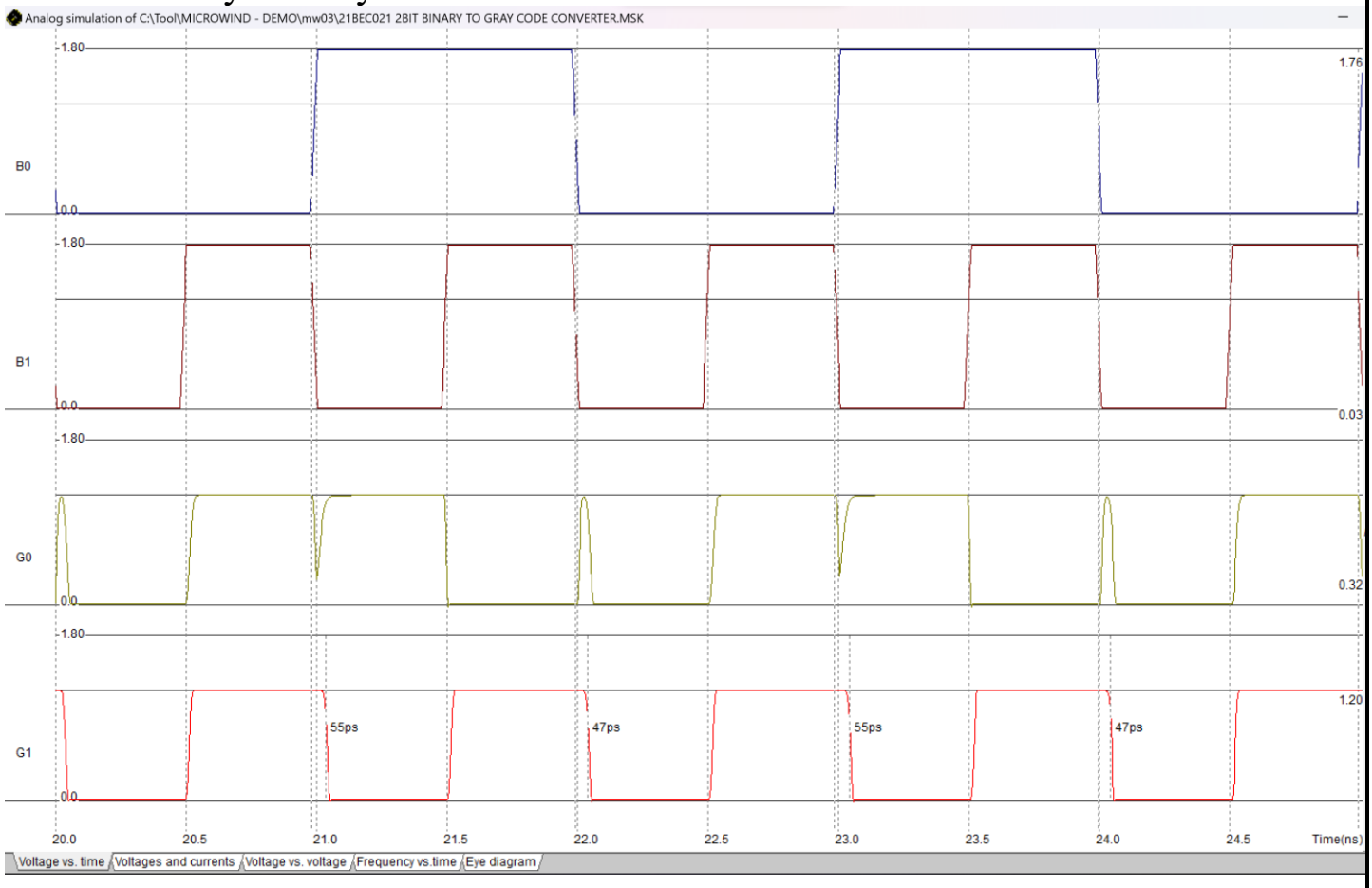
❖ Simulate it for various combinations of inputs.

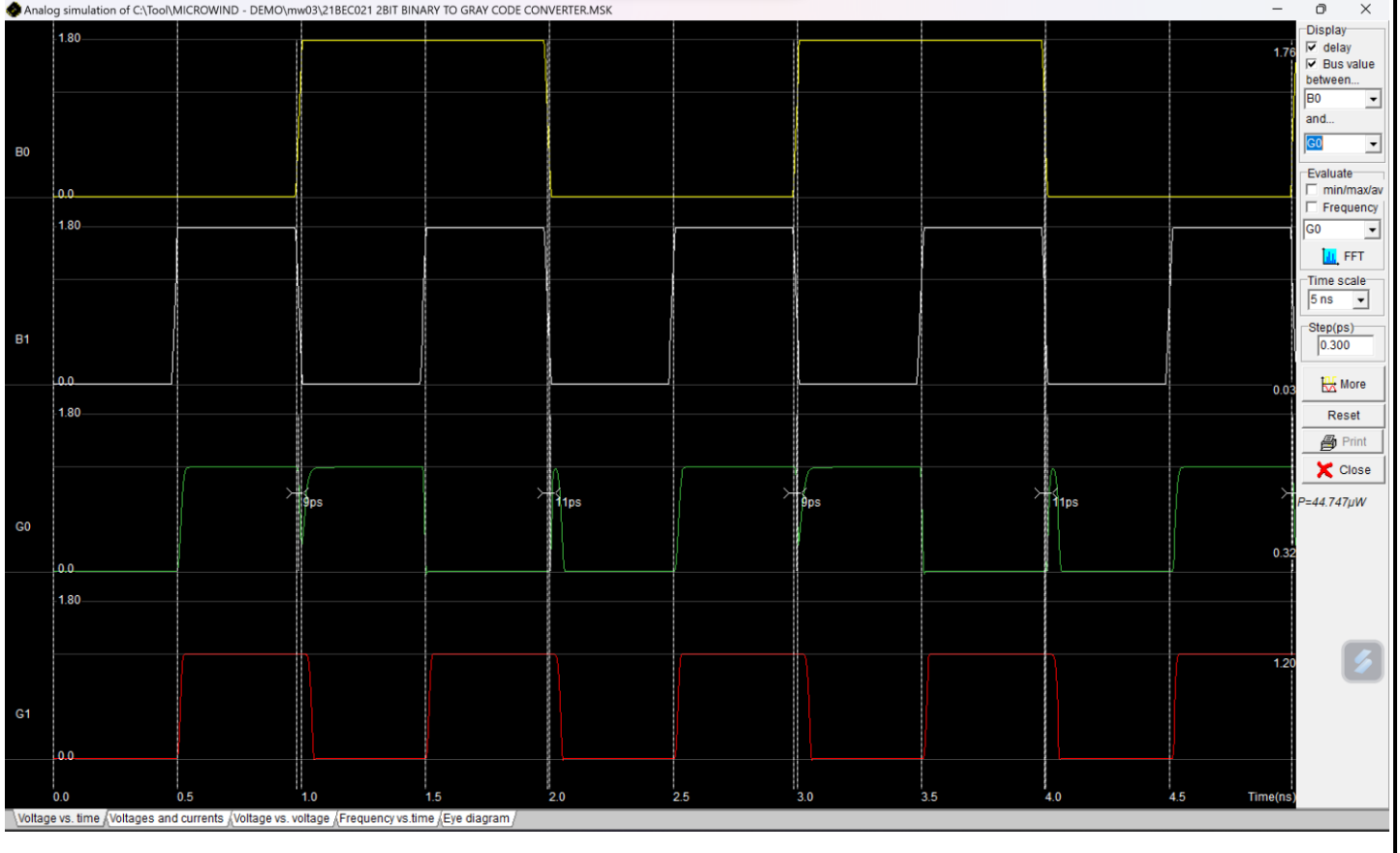


2 bit Binary to Gray code converter for Vin=1.2V

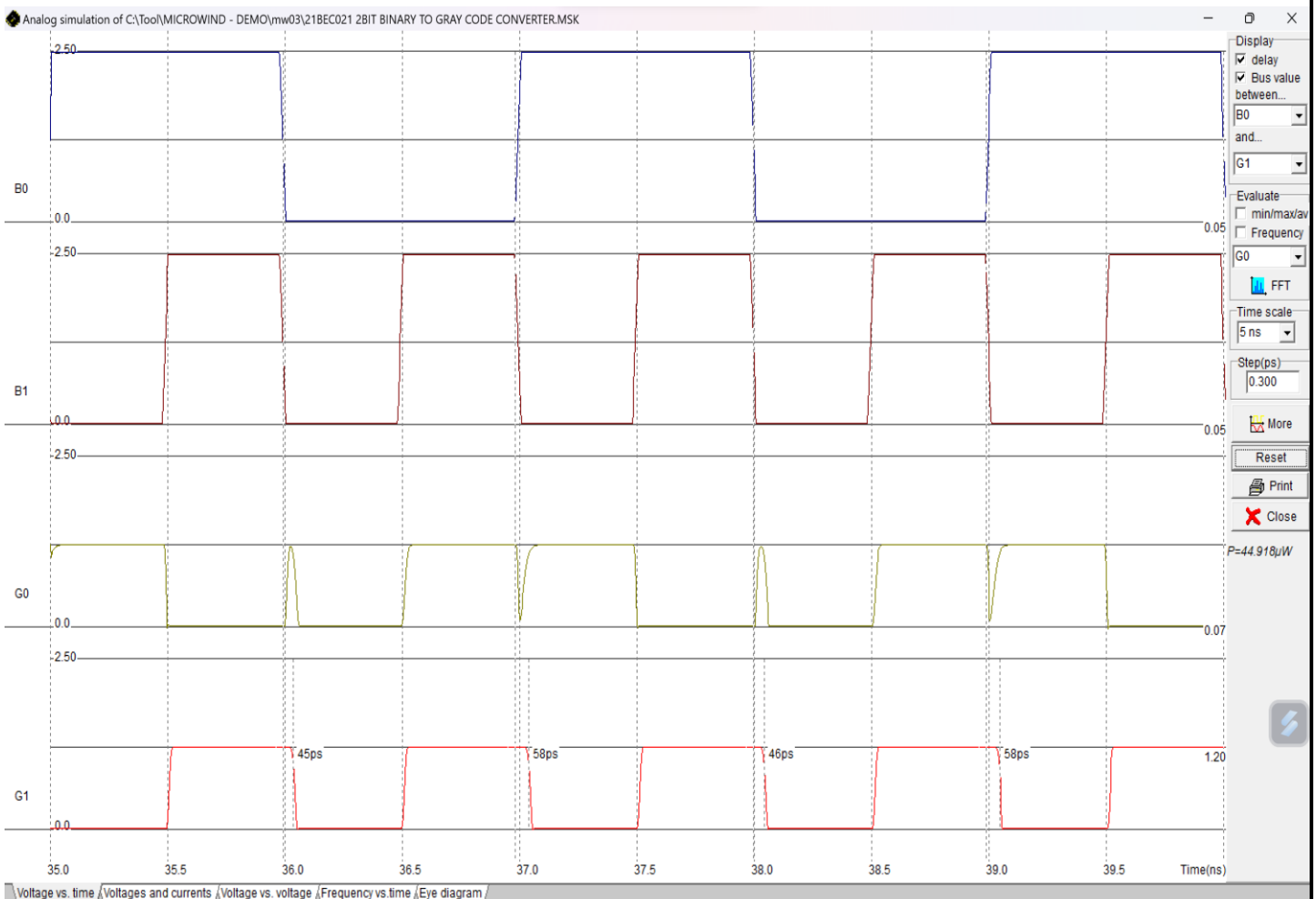


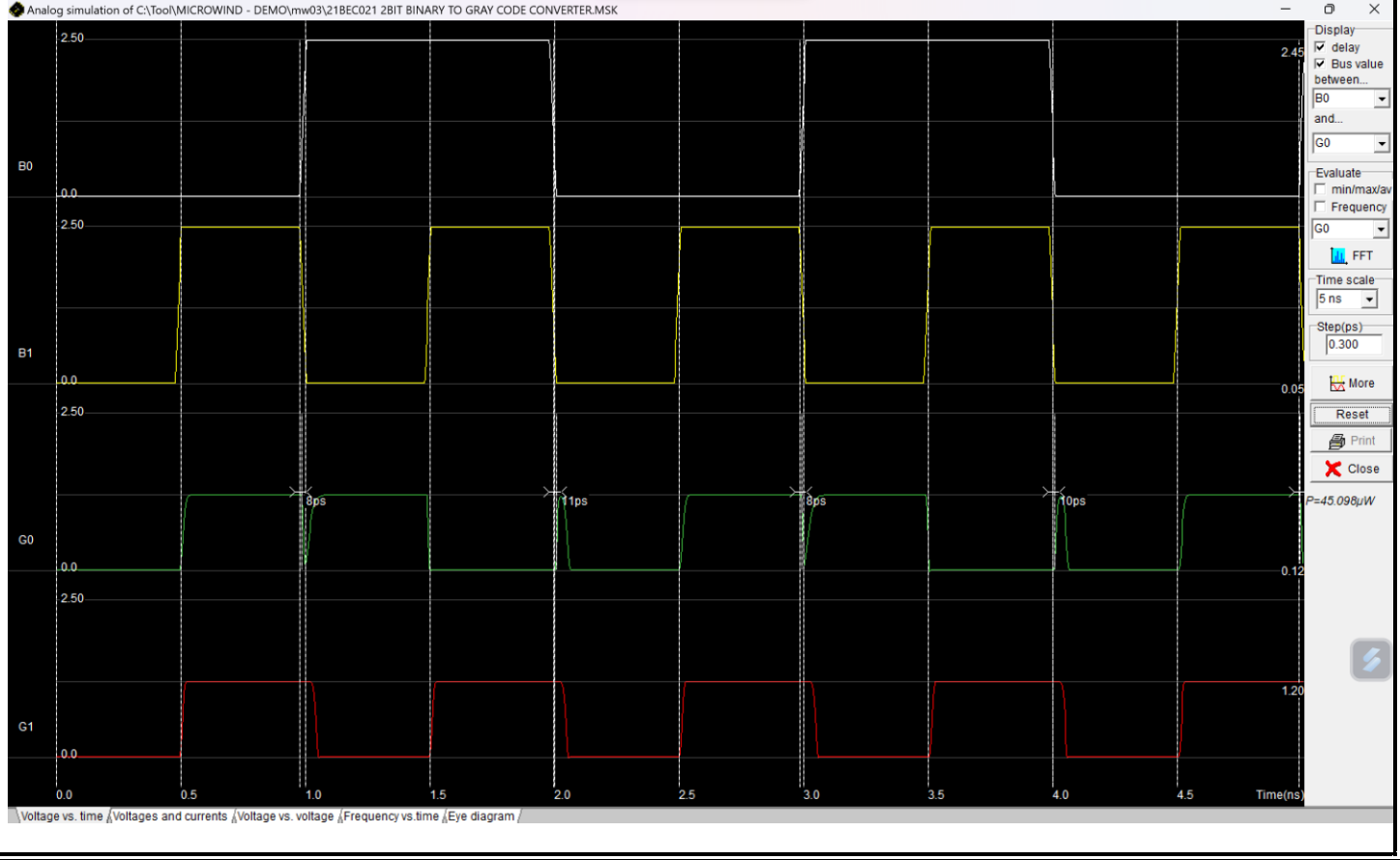
2 bit Binary to Gray code converter for Vin = 1.8V





2bit Binary to Gray code converter for Vin = 2.5V





❖ Measure the rise time, fall time, propagation delay and other parameters.

For V = 1.2V

W/L PMOS (µm)	W/L NMOS (µm)	τpHL (ps)	τpLH (ps)
0.78	0.62	11	13

For V = 1.8V

W/L PMOS (µm)	W/L NMOS (µm)	τpHL (ps)	τpLH (ps)
0.78	0.62	9	11

For V = 2.5V

W/L PMOS (µm)	W/L NMOS (µm)	τpHL (ps)	τpLH (ps)
0.78	0.62	8	11

❖ CONCLUSION :-

- Gray Code system is a binary number system in which every successive pair of numbers differs in only one bit. It is used in applications in which the normal sequence of binary numbers generated by the hardware may produce an error or ambiguity during the transition from one number to the next bit and from here, the significance of a Binary to Gray code converter could be derived.

- The different V values for different input patterns were observed, and it was noticed that the path including the NMOS offers the least resistance. Furthermore, the higher the input source voltage, the better the obtained characteristics.

- Some of the furthermore applications of the developed circuit in this report includes;
  - Rotary Encoders:
    Rotary encoders are sensors used to measure the position of a rotating object. Gray code is often employed in rotary encoders because it reduces the chance of errors when transitioning between values.
  - Robotics and Motion Control:
    In applications where precise motion control is essential, such as robotics, Gray code is used to represent positions.
  - Digital Signal Processing (DSP):
    In certain DSP applications, Gray code is used for signal processing or encoding. A binary-to-gray code converter can be integrated into DSP systems to handle data in Gray code format.
  - Telecommunications:
    In digital communication systems, Gray code is used in certain modulation and encoding techniques.

- Using the MICROWIND and DSCH software, a combination of CMOS was assembled to form an XOR gate, which in turn by combination with two inverters formed a triumphant working model of a 2 bit Binary to Gray code converter through successful and optimum utilization of its' truth table, gate level and transistor level schematic diagram and a stick diagram for an efficient CMOS implementation which would provide an unordered series of Gray encoded bits in result as a output of four possible combination of binary bits.