# HMC Controller IP

## Altera Stratix V® and Xilinx UltraScale® FPGAs

## OVERVIEW

Hybrid Memory Cube (HMC) is a high-performance memory solution that delivers unprecedented levels of bandwidth, power efficiency, and reliability. Pico Computing's innovative HMC controller IP—designed specifically for, and in collaboration with, Micron—unlocks the HMC's power, providing tremendous benefits to memory-bound applications, and particularly those that require high bandwidth and fast random access. And because Pico Computing's HMC controller core was engineered for designers familiar with DDR3 memory, it's easy to use.

## APPLICATIONS

Pico Computing's high-performance systems solutions dramatically accelerate algorithms with 100 to >1,000X speedups. But when those applications require large amounts of random access memory, performance hits a wall. The HMC solution changes that equation, effectively knocking down the memory wall. When managed by Pico Computing's powerful HMC Controller IP, the new memory technology enables a huge leap forward for high-performance computing, opening up new applications, markets, and business models. With a 15x speedup over DDR memory, massive performance improvements are realized immediately in packet processing, waveform processing, bioinformatics, image and video processing, and other memory/bandwidth-bound applications.

## FEATURES

- Fully-compliant HMC Rev 1.1 specification, Micron tested and validated
- Supports Altera Stratix V, Xilinx UltraScale®, and Xilinx Virtex-7 series devices
- 10Gbp/s (250MHz core); 12.5Gbp/s (312 MHz core); 15Gbp/s (375 MHz core) SerDes I/O interfaces
- 8- (half-width) or 16-lane (full-width) full duplex serialized links
- Packet-based data/command interface
- Multiple interface options for maximum flexibility:
  - Full custom interface
  - AXI-4 interface
  - 640 bit-wide "native" interface
  - Pico Computing's High-performance (intelligent multiport) interface
- Up to 240 GB/s of total interface bandwidth
- Parameterized number of user interface ports
- Flexible datapath widths
- Link layer and transaction layer
- Packet sizes of 16b to 128b requests
- Atomic commands supported
- Power-on initialization
- Power state management (per link)
- Poisoned packets, CRC/packet integrity, tagging
- JTAG
- Device chaining
- Configuration and status registers
- Error detection and automatic retry
- Warm reset
- Link Retry
- Link retraining
- Token-based flow control
- Bit error injection mechanisms to support testability and characterization

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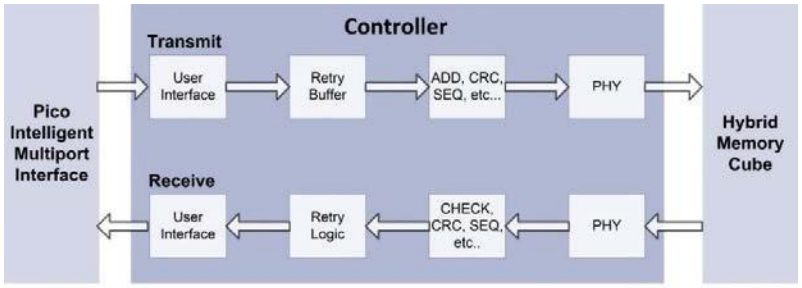
## IP Block Diagram

Designed for those already familiar with DDR memory architecture, integration of Pico Computing's HMC Controller is made easy and seamless via multiple interface options (shown at right) that provide data throughput sufficient to satisfy the high memory bandwidths possible with HMC technology.




## Interface Options

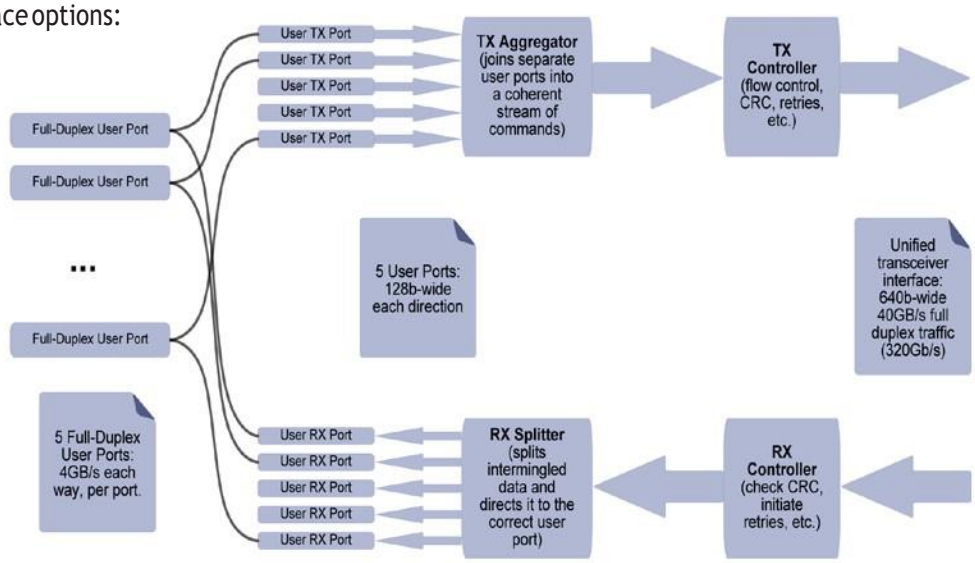
The HMC IP is available with four user interface options:

1 Full custom interface.

2 640 bit-wide "native" interface.

3 AXI-4 interface.

4 Pico Computing's High-performance (intelligent multiport) interface. As shown at right, this option breaks the 640 bit- wide native interface into a more manageable set of five 128 bit-wide interfaces, which are similar in operation to a conventional DDR interface. It is low overhead, generates transmit and receive pipelines, handles all send/receive data requests, and makes using the HMC seamless and without adding latency.




*HMC block diagram shown with Pico Computing's High-performance Interface option.*

## Fully Configurable IP

Pico Computing's HMC controller is highly parameterized to yield truly optimized system configurations to meet specific design objectives. The number of HMC links addressed, the number and width of internal ports, clock speeds, power, performance, area, and other parameters can be "dialed in" to yield precisely the characteristics required.

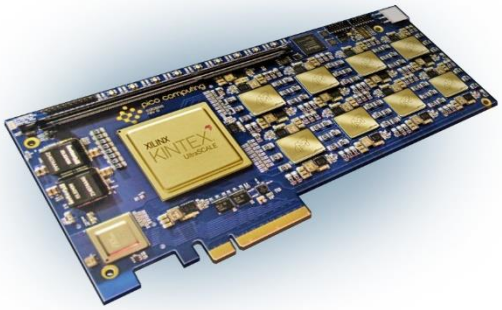
## Deliverables & Support

Pico Computing offers a complete solution for the HMC Controller, including:

- The complete HMC Controller 1.1 specification in IP, ready for implementation
- RTL
- Test bench with simulation model
- Documentation
- Examples
- Built-in analysis features that allow the evaluation, test, and characterization of the HMC in the context of the system
- The Pico Computing Framework
- (PCIe, DMA engine, APIs, etc.)
- Training and application support

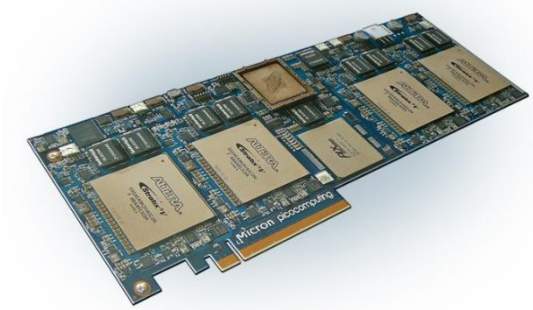
## Xilinx-based Evaluation & Development Board (SB-850)

- GPU-sized PCI Express board
- Configured for either Virtex or Kintex UltraScale devices
- 2-link 4GB HMC chains configured as follows:
  - One x16 lane (full width) with up to four HMCs chained
  - Two x8 lanes (half-width) with two HMCs accessed independently or chained, with the option to chain up to four HMCs
- 8GB dual-rank DIMM
- Gen3 PCIe
- 8 Transceivers for off-board communications

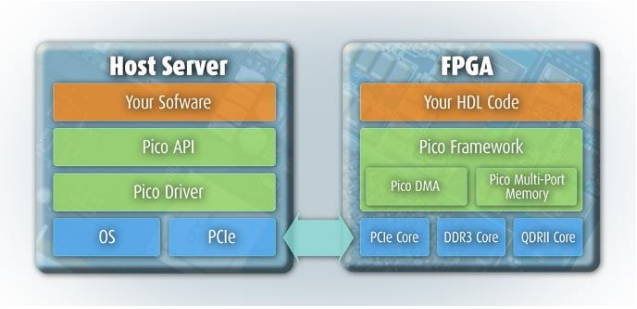


## Altera-based Evaluation & Development Board (SB-801)

- Full height, full length, PCI Express board
- Array of four Stratix V devices and a single HMC
- Each Stratix V device has a x8 PCI Express Gen 3 link to an onboard PEX8780 PCI Express switch
- The upstream connection of the PEX8780 is a x16 PCI Express Gen 3 edge connector
- In addition to the HMC, the SB-801 features a total of 16GB of DDR3L SDRAM
- High-speed FPGA-to-FPGA interconnect



## Simple Design Framework




Implementation of the HMC controller is made easy by virtue of Pico Computing's framework, a Linux-based design utility/runtime environment that provides the vital link between your application software running on a host computer and the hardware algorithm, or firmware, implemented in the FPGA. Think of it as the "Ghost in the Machine"—a powerful but invisible and active intelligence that runs and governs the board-level implementation of FPGA designs, as well as data flow, memory management, system communication, monitoring/debug, and more in ways that make life easy for the FPGA design engineer using vendor tool flows. In short, it's everything you need to get up and running right away.

- Automatically loads the HMC controller and other FPGA bitfiles over PCIe
- Includes all drivers including host-side (Unix), interface to host (PCI Express)
- Pico API (C++)
- Integrated firmware test suite
- Automates all reading and writing to the FPGAs' off-chip memory (firmware memory interfaces automate all memory systems arbitration)
- Actively monitors FPGA(s) temperature, current, and voltage to enhance system performance and reliability