I/O Power Estimation and Analysis of High-speed Channels in Through-Silicon Via (TSV)-based 3D IC

Joohee Kim, Jonghyun Cho, Jun So Pak, Taigon Song and Joungho Kim
Department of Electrical Engineering
KAIST
Daejeon, South Korea
joohee@eeinfo.kaist.ac.kr

Hyungdong Lee, Junho Lee and Kunwoo Park
Advanced Design Team
Hynix Semiconductor Inc.
Icheon-si, Gyeonggi-do, South Korea
hyungdong.lee@hynix.com

***Abstract* — In today's integrated circuits, power consumption has become the most important factor, and must be seriously investigated among the various performance metrics. In this study, power estimations for various through-silicon via (TSV)-based three-dimensional integrated circuit (3D IC) designs were conducted in efforts to realize low-power-consumption 3D IC. In addition, the dominant power-consuming factor was found among the TSV-based interconnect components by a power comparison analysis based on the proposed model.**

Keywords-dynamic power consumption; through-silicon via (TSV); three-dimensional integrated circuit (3D IC); re-distribution layer (RDL); interposer

I. INTRODUCTION

Currently, through-silicon via (TSV)-based three-dimensional integrated circuits (3D IC) are the leading technology for further miniaturization and higher system performance. With the reduced interconnection length made possible by using a TSV as a vertical interconnection method among the stacked dies, the TSV-based 3D IC has become the key solution to reducing power consumption.

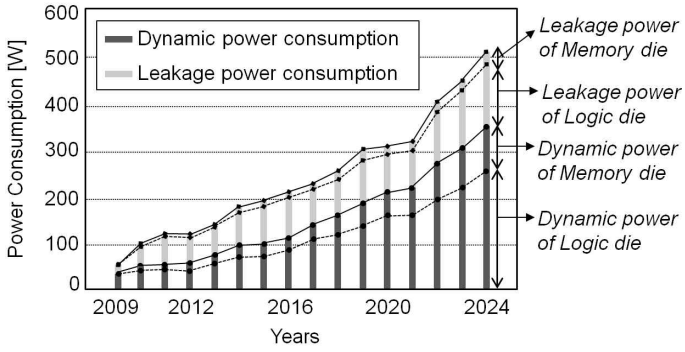

Figure 1. Dynamic and leakage power consumption trends of system-on-chip (SOC) in cases of integration with memory and logic dies [1].

According to ITRS 2009 [1], power management has become one of the most important design issues to consider in advanced system design. In addition, dynamic power consumption has become a more serious issue as data rates increased every year up to several GHz, as shown in Figure 1. In the TSV-based 3D IC design, the fraction of dynamic power consumption due to the interconnect is still considerable even with the shortened interconnection length. In practical 3D integration of heterogeneous dies into one package, horizontal interconnections such as a redistribution layer (RDL) and an interposer metal are necessary. Thus, a wide RDL and a long interposer metal increase the loading capacitance of the overall TSV-based I/O channel, which can strain the limited I/O power budget of a 3D IC system. In addition, the TSV has a capacitive characteristic due to a thin insulating layer between the TSV and the conductive silicon substrate; this can also increase dynamic power consumption. Furthermore, while the 3D IC has the advantage of enabling a wide I/O system with a TSV, the power dissipation required for I/O switching on the order of several thousands becomes considerable and must be seriously investigated. Thus, to save the power, it must be determined which component consumes the most power in a TSV-based I/O channel. Many studies have analytically estimated the amount of power consumption of other systems [2-3]; however, the analysis of the power consumption of a TSV-based 3D IC has not been adequately conducted yet.

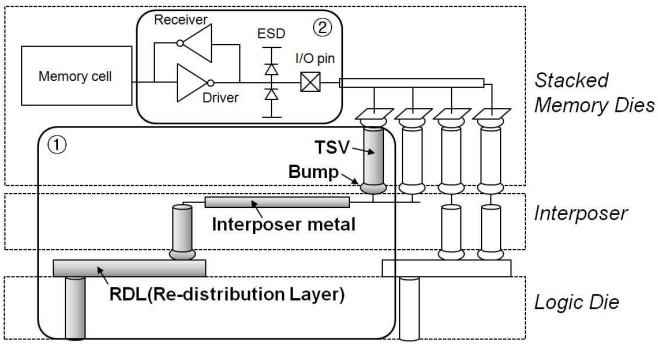

Figure 2. Power consumption in a 3D IC; ①dynamic power consumption of TSV-based interconnect, ②dynamic/static power consumption of I/O circuitry.

In this study, we estimated the power dissipation of the TSV-based I/O channel in a 3D IC. As shown in Figure 2, there are two main factors to be considered in power management of a TSV-based I/O channel in a 3D IC: the TSV-based interconnect and the I/O circuitry. Because the I/O driver must be optimized by considering the channel characteristics and signal integrity issues such as reflection, termination, etc., the dynamic and leakage power consumptions due to the I/O driver were not considered in this work. Instead, we focused on the

dynamic power consumption of the TSV-based I/O channel. To estimate the dynamic power consumption of the TSV-based I/O channel, analytic models were proposed for calculating loading capacitances. Based on the proposed capacitance models, we estimated the dynamic power consumption of the TSV-based I/O channel and compared it for various 3D IC designs such as TSV arrays with different ground TSV counts, TSV and RDL/interposer metal dimension and various 3D architectures.

II. Proposed Model for Power Estimation of the TSV-based I/O Channel

A. Capacitance Model of the Through-Silicon Via (TSV)

With the thin insulating layer between the TSV and the conductive silicon substrate, the TSV capacitance becomes one of major sources of the loading capacitance of the TSV-based I/O channel. To calculate the equivalent capacitance of the TSV, an analytical TSV capacitance model is proposed.

As shown in Figure 2, the equivalent capacitance of a TSV, C_{TSV}, is proposed based on the equivalent-circuit model of TSV [4]. In this equivalent-circuit model, the bump effect is included as it is a necessary component for TSV connection between stacked dies. Due to the conductance of the silicon substrate between signal and ground TSVs, G_2, the equivalent capacitance of the TSV changes depending on frequency, which results in a slow-mode effect. In addition, G_2 can be expressed with C_2 and material properties such as an electrical permittivity of the silicon substrate, ϵ, and a conductivity of the silicon substrate, σ. Thus, the equivalent capacitance of the TSV, $C_{TSV(1S1G)}$, can be derived as a function of C_1, C_2, C_3 and material properties of the silicon substrate, which has a one-signal and one-ground TSV configuration (1S1G).

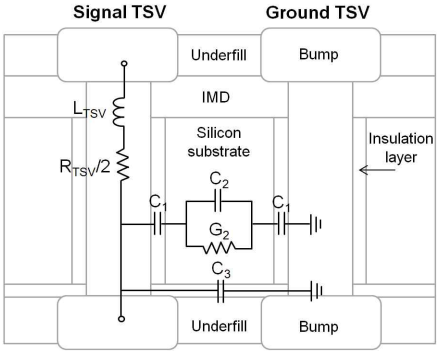

Figure 3. A cross-sectional structure with the simplified equivalent-circuit model of a TSV, including a signal TSV, a ground TSV and bumps.

However, as the number of ground TSVs changes, the equivalent capacitance of the TSV array also changes. As the ground TSV count (n), near a signal TSV increases from 1(1S1G) to 8(1S8G), the equivalent capacitance, $C_{TSV(1SnG)}$, was modeled by extracting the coefficients α and β in Eq. (1), as shown in Table 1. The proposed equations with different ground TSV counts were verified by simulation using a 3D field solver (Ansoft HFSS). Because Eq. (1) is a function of frequency, the loading capacitance of TSV changes depending on operating frequency.

$$C_{TSV\,(1sng)}(\omega) = \frac{\alpha_n \cdot C_1 C_2 \left(\beta_n + \frac{\sigma}{\beta_n \cdot \varepsilon\omega} \right)}{\alpha_n \cdot C_1 + (\alpha_n + 1) \cdot C_2 \left(\beta_n + \frac{\sigma}{\beta_n \cdot \varepsilon\omega} \right)} + \alpha_n \cdot C_3 \quad (1)$$

TABLE I. Coefficients for the Equivalent Capacitance of TSVs with Different Numbers of Ground TSVs.

n (the number of ground TSV)	Coefficients for the equivalent capacitance of TSV array	
	α_n	β_n
1	1	1
2	2	3/2
4	5/2	17/10
8	27/10	172/100

With the proposed equation and coefficients, the equivalent capacitances of TSVs with different TSV array configurations and frequencies were calculated and are listed in Table 2. As shown in here, $C_{TSV(1s8g)}$ decreased as the frequency was increased, going from 105.4 fF at 100 MHz to 27.4 fF at 10 GHz. In addition, as the number of ground TSV (n) surrounding a signal TSV was increased from 1 to 8, $C_{1s1g} > C_{1s2g} > C_{1s4g} > C_{1s8g}$ under 1 GHz. However, over 1 GHz, C_{1s8g} began to exceed C_{1s1g}, C_{1s2g} and C_{1s4g}. At frequencies under 1 GHz, C_{TSV} was dominantly determined by C_1, which is the insulator capacitance of a TSV; however, over 1 GHz, C_{TSV} increased as the ground TSV count was increased because the effect of the increased silicon-substrate capacitance, C_2, became dominant, as expressed by the increased β. Thus, at 20 GHz, $C_{1s1g} < C_{1s2g} < C_{1s4g} < C_{1s8g}$,

TABLE II. Equivalent Capacitance of TSV, C_{TSV}, Depending on the Ground TSV Count When Varied from One (1S1G) to Eight (1S8G).

Frequency (Hz)	Equivalent capacitance of TSV, C_{TSV}, with TSV array configurations (fF)			
	1s1g	*1s2g*	*1s4g*	*1s8g*
100 M	121.3	109	104	105.4
1 G	87.1	74.5	70.9	71.5
2 G	67.2	56.9	54.6	55
10 G	27.6	26.3	26.9	27.4
20 G	18.5	20.1	21.4	21.9

B. Capacitance Model of RDL/Interposer metal

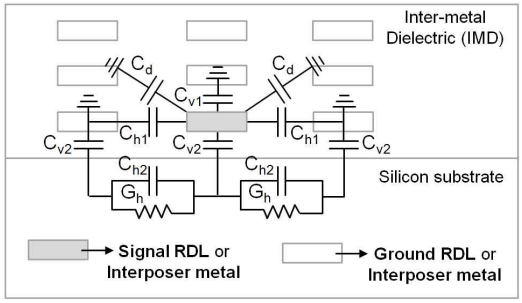

Figure 4. A cross-sectional structure of the RDL or interposer metal and its parasitic capacitances when signal propagates through the bottom metal layer, which is the closest layer to the silicon substrate.

Because heterogeneous dies have different design rules and scales, such as the TSV-based I/O pin count and their locations, horizontal interconnections such as RDL and interposer metal are necessary for 3D integration of heterogeneous dies. Thus, the loading capacitances from the routed RDL and interposer metal must be considered for the dynamic power estimation of a TSV-based I/O channel. As shown in Eq. (2), the loading capacitance of the RDL or interposer metal can be calculated based on the equivalent-circuit model [5]. Because the RDL or interposer metal layer is formed on the silicon substrate, the electromagnetic field can permeate into the silicon substrate when signal propagates on the bottom RDL, as shown in Figure 4. Therefore, the conductance of the silicon substrate, G_h, affects the total loading capacitance of RDL and interposer metal, resulting in a frequency-dependent capacitance.

$$C_{RDL,bottom}(\omega) = \frac{2C_{v2}C_{h2}\left(2+\frac{\sigma}{2\cdot\varepsilon\omega}\right)}{2C_{v2}+3C_{h2}\left(2+\frac{\sigma}{2\cdot\varepsilon\omega}\right)} + C_{v1} + 2\left(C_d + C_{h1}\right) \quad (2)$$

In case of signal propagation on the top or middle layer, the loading capacitances, $C_{RDL,top}$ and $C_{RDL,middle}$, respectively, are calculated by Eq. (3). These capacitances are calculated by assuming that there is no field penetration into the silicon substrate when signal propagates through the top and middle layers of the metal. Thus, they are not dependent on frequency. In addition, $C_{RDL,bottom}$ is larger than $C_{RDL,top}$ and $C_{RDL,middle}$. Thus, as the signal propagates on the farther metal layer from the silicon substrate, more loading capacitance can be reduced.

$$\begin{aligned} C_{RDL,top} &= C_{v1} + 2\cdot\left(C_d + C_{h1}\right) \\ C_{RDL,middle} &= 2\cdot\left(C_{v1} + C_d + C_{h1}\right) \end{aligned} \quad (3)$$

III. Power Estimation/Comparison with the Proposed Model of TSV-based I/O Channel

Using the proposed capacitance models of the TSV, RDL and interposer metal, the estimation and comparison of the dynamic power consumption of the TSV-based I/O channel are described here.

A. Ground-TSV Count Variation

As the loading capacitance of the TSV changes with the number of ground TSVs surrounding a signal TSV, the dynamic power consumption changes depending on ground TSV count. For the different ground TSV counts, the dynamic power consumption of the TSV array was calculated by the following equation.

$$P_{d,TSV}(\omega) = AF \cdot C_{TSV}(\omega) \cdot V^2 \cdot f \quad (4)$$

As shown in Figure 5, dynamic power consumption, $P_{d,TSV}$ changed as ground TSV count, n, was changed. In the same manner as the consideration of loading capacitance depending on TSV-array configurations in the previous section, $P_{d,TSV}$ with a 1s1g configuration is bigger than $P_{d,TSV}$ with 1s8g configuration under 10 GHz. However, over 10 GHz, $P_{d,TSV}$ with a 1s8g configuration became larger because the effect of the increased silicon-substrate capacitance became dominant.

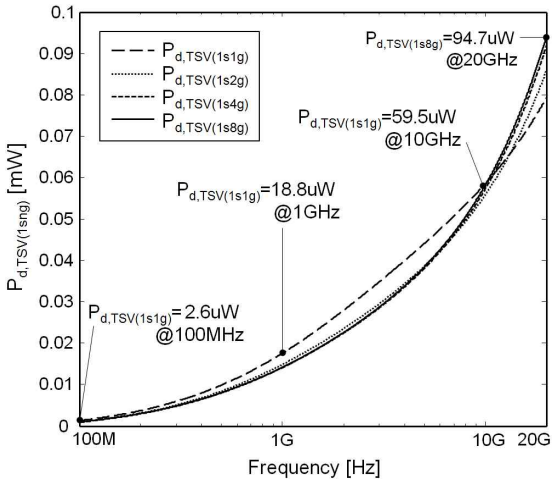

Figure 5. Dynamic power consumption of TSV array depending on ground-TSV count with an activity factor of 0.15 and a supply voltage of 1.2 V. The baseline TSV dimensions (d_{TSV}, p_{TSV}, h_{TSV} and t_{ox}) were assumed to be 10 μm, 35 μm, 50 μm and 0.5 μm, respectively.

B. TSV Dimensional Variation

With the 1s8g configuration, the changes in dynamic power consumptions with TSV dimension variation were calculated; here, TSV diameter (d_{TSV}), TSV pitch (p_{TSV}) and insulation layer thickness (t_{ox}) were the main design parameters for dimension variation of the TSV. As shown in Figure 6, $P_{d,TSV}$ increased as d_{TSV} was increased and as p_{TSV} and t_{ox} was decreased. Because C_1 and C_2 in Figure 2 both increased as d_{TSV} was increased. In addition, C_2 and C_3 increased as p_{TSV} was decreased and C1 increased as t_{ox} was decreased, causing $P_{d,TSV}$ to increase.

Thus, to decrease d_{TSV} and to increase p_{TSV} and t_{ox} are the ways to reduce the dynamic power dissipation from the TSV, since they can reduce the equivalent capacitance of TSV, C_{TSV}.

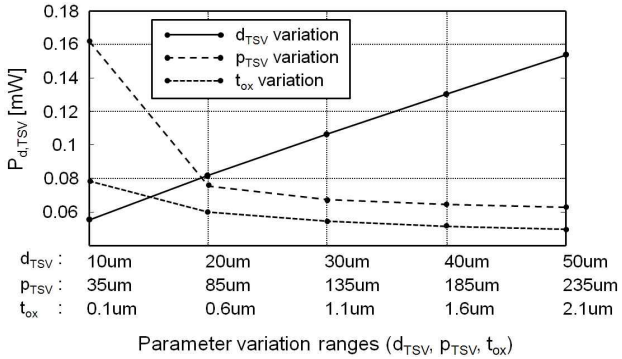

Figure 6. Dynamic power consumption of TSV with d_{TSV} variation (p_{TSV}=135 μm, t_{ox}=0.5 μm), p_{TSV} variation(d_{TSV}=10 μm, t_{ox}=0.5 μm), t_{ox} variation (d_{TSV}=10 μm, p_{TSV}=35 μm) with the activity factor, supply voltage and operating frequency assumed to be 0.15, 1.2 V and 800 MHz, respectively.

C. RDL/Interposer metal Dimensional Variation

To redistribute the I/O signals horizontally, RDL and interposer metal routing must be done within design parameters such as metal width (W), space (S), thickness (T), inter-layer dielectric (ILD) height (H), and length (L). Here, we estimated and compared the dynamic power consumption with variations in these parameters. As shown in Figure 7, the dynamic power consumption was more significantly influenced by width variation rather than space variation between RDLs. This is because the parasitic capacitance of an RDL is dominantly formed by the vertically confronting faces between RDLs or between the RDL and the silicon substrate, i.e., C_{v1} or C_{v2}, respectively, in Figure 4. In the case of the interposer metal, power consumption was also more strongly affected by width than by space in the same manner as in the RDL case. This conclusion is only valid when the aspect ratio (W/T) is larger than 1. If not, S becomes more dominant in the dynamic power consumption rather than W. Thus, to decrease W and to increase S are the ways to reduce the dynamic power consumption from the RDL/interposer metal.

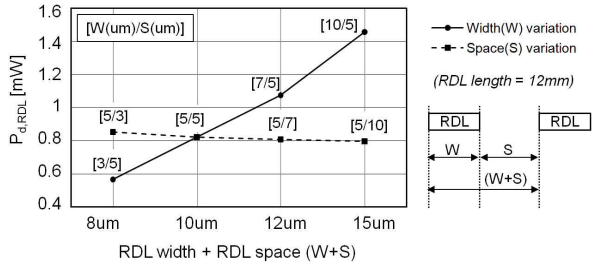

Figure 7. Comparison of the dynamic power consumption of RDL, $P_{d,RDL}$, depending on width(W) and space(S) variation with the activity factor, supply voltage and operating frequency assumed to be 0.15, 1.2 V and 800 MHz.

D. 3D Architecture Variation

Depending on the various 3D architectures used to integrate homo- or heterogeneous dies, the routed interconnect lengths and TSV count vary, changing the dynamic power consumption. We assume two representative 3D architectures, each integrating four memory dies and a processor, using an interposer, i.e., vertical-stack and planar-stack architectures. RDL is assumed to be formed on the back-side of the processor and interposer metal is an inner-metal of the interposer.

As shown in Figure 8, planar-stack architecture consumed less dynamic power, as this architecture reduces the horizontal interconnection length due to the closer I/O pad locations between stacked-memory dies and the logic die. With planar-stack architecture, the length of RDL and interposer metal can be reduced by 30% and 50%, respectively. For an I/O count of 2000, the total dynamic power consumptions of vertical- and planar-stack architectures due to TSV-based I/O channel were about 3 W and 1.64 W, respectively. In addition, the RDL was the dominant power-consuming component among the TSV-based I/O channel components due to its wide width, which was assumed to be 5 µm in this paper. The RDL consumes over 70% of the total dynamic power in both architectures. Due to the short height of the TSV, it did not consume a major fraction of the total dynamic power dissipation, even with a thin insulating layer. Thus, the best ways to design low-power-consuming TSV-based I/O channels in 3D IC systems would be to decrease the RDL/interposer metal width, shorten the interconnect length and choose the 3D architecture having the shortest routed interconnect lengths possible.

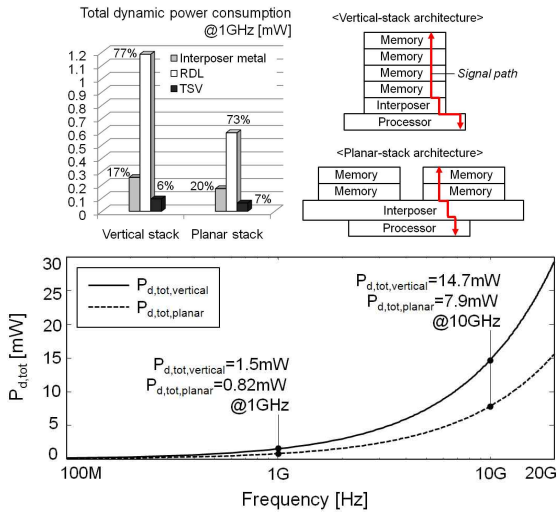

Figure 8. Comparison of the total dynamic power consumption of a TSV-based I/O channel, $P_{d,tot}$, depending on different 3D architectures (vertical-stack and planar-stack architectures). W/S of RDL and interposer metal were assumed to be 5 µm/5 µm and 0.8 µm/0.7 µm, respectively.

IV. Conclusion

In this work, we proposed a capacitance model for a TSV-based I/O channel including TSVs, bumps, the RDL and interposer metal to estimate dynamic power consumption of a TSV-based I/O channel in a 3D IC. With the proposed model, we estimated and compared dynamic power consumption depending on ground TSV count, TSV/RDL/interposer metal dimensional variations and different 3D architectures. Among the TSV-based I/O channel components, the dynamic power consumption was dominated by the RDL, and design guides of each component to save power were proposed.

Acknowledgment

This work was partly supported by the IT R&D program of MKE/KEIT. [KI002134, Wafer Level 3D IC Design and Integration]

References

[1] *The International Technology Roadmap for Semiconductors* (ITRS), 2009. Available: http://www.itrs.net

[2] N. Margen, *et al*, "Interconnect-Power Dissipation in a Microprocessor," *Proc. of the 2004 international workshop on System level interconnect prediction, February 14-15, 2004, Paris, France, pp.7–13.*

[3] L. Shang, *et al*, "Dynamic Power Consumption in Virtex™-2 FRPGQ Family," *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, February 2002, pp. 157-164.*

[4] J. Kim, *et al*, "Through Silicon Via (TSV) Equalizer," *Proc. 18th conference on Electrical Performance of Electronic Packaging and Systems, Portland (Tigard), Oregon, 2009, pp. 13-16.*

[5] F. Stellari, *et al*, "New Formulas of Interconnect Capacitances Based on Results of Conformal Mapping Method," *IEEE Trans. Electron Devices, vol. 47, pp. 222-231, Jan. 2000.*