National Science Foundation's Industry/University Cooperative Research (I/UCRC) Program

VANTAGE

Visual And Neuromorphic Tracking And Geosensing Experiment

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

Mission Overview

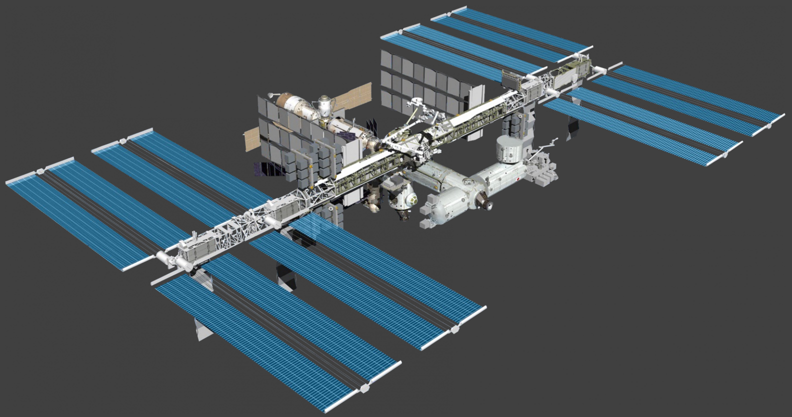
Dr. Alan D. George
Mickle Chair Professor of ECE

Michael Cannizzaro
Payload Manager
Research Student
University of Pittsburgh

University of Pittsburgh
BYU BRIGHAM YOUNG UNIVERSITY
VIRGINIA TECH
UF UNIVERSITY of FLORIDA

Outline

- Introduction
- Technologies
- Mission Design
- Hardware
- Apps and Services
- Timeline
- Conclusions



Introduction

Acknowledgments

DEPARTMENT OF DEFENSE
UNITED STATES OF AMERICA

NASA

Air Force Research Laboratory

Sandia National Laboratories

APL
Johns Hopkins
Applied Physics Laboratory

University of Pittsburgh®

Tokina

Space Test Program

BYU
Brigham Young University

AMD
XILINX®

U.S. Naval Research Laboratory

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Lockheed Martin

Introduction

- **VANTAGE is an NSF SHREC Research Mission**
  - NSF Center for Space, High-Performance, and Resilient Computing
    - Founded in 2017
    - Formerly CHREC (2007-2017)
    - Comprised of four universities and 25+ industry and government partners
  - Four Major Universities:
    - University of Pittsburgh (lead)
    - Brigham Young University (partner)
    - University of Florida (partner)
    - Virginia Tech (partner)
- **VANTAGE Builds Upon Past Success**
  - STP-H5-CSP, STP-H6-SSIVP, and STP-H7-CASPR

University of Pittsburgh

UF UNIVERSITY of FLORIDA

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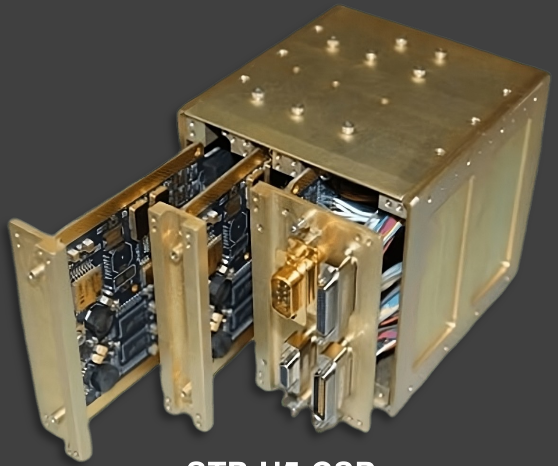
VT

Space Test Program

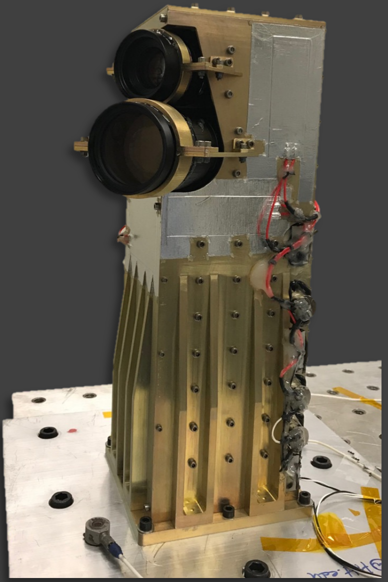
- **Space Test Program – Houston (STP-Hx)**
  - Managed by United States Space Force
  - “Driving force in DoD space technology advancement”
  - Sole interface to NASA for all DoD payloads on International Space Station (ISS)
  - Provides:
    - Spaceflight opportunities (payloads and launches)
    - Readiness assistance (documentation, reviews, etc.)
    - Management (operations infrastructure)
    - Technical support

SHREC Mission Heritage

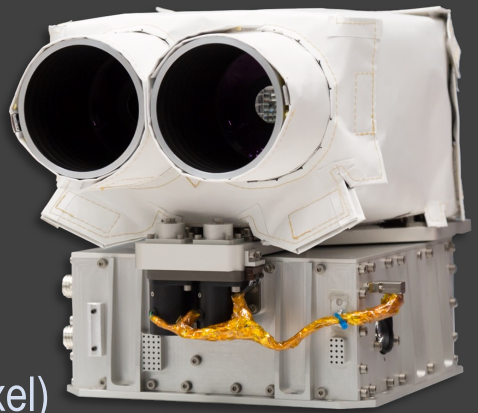
- **Three Successful Missions**
  - STP-H5-CSP
    - <u>C</u>HREC <u>S</u>pace <u>P</u>rocessor
    - Demonstration of CSP and hybrid COTS + rad-hard architecture
    - 5 MP Sony camera for Earth observation
  - STP-H6-SSIVP
    - <u>S</u>pacecraft <u>S</u>upercomputing for <u>I</u>mage and <u>V</u>ideo <u>P</u>rocessing
    - Parallel and distributed computing with CSP cluster
    - Two 5 MP cameras (differing field-of-view) for Earth observation
  - STP-H7-CASPR
    - <u>C</u>onfigurable and <u>A</u>utonomous <u>S</u>ensor <u>P</u>rocessing <u>R</u>esearch
    - Enable onboard processing for next-generation sensors and apps
    - Satlantis iSIM-90 high-resolution, hyperspectral imager (GRD ~3.0 meters/pixel)



STP-H5-CSP



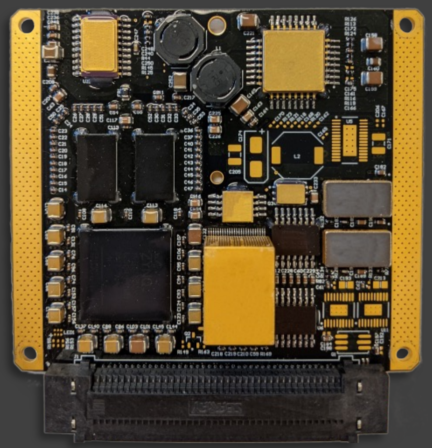
STP-H6-SSIVP



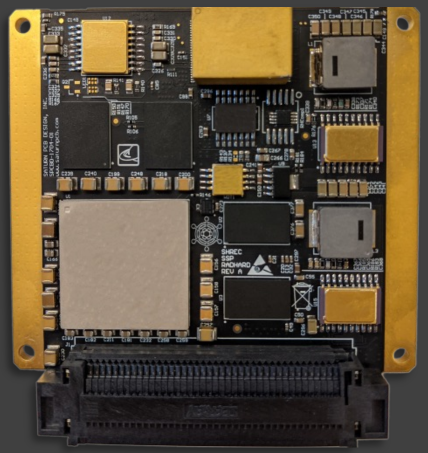
STP-H7-CASPR

STP-H12-VANTAGE

- **In-House Expertise**
  - Earth-observation datasets, classifiers, and compression tools
  - Novel edge computing through hybrid (rad-hard + COTS) processing
  - Reliable flight hardware, FPGA apps, and software

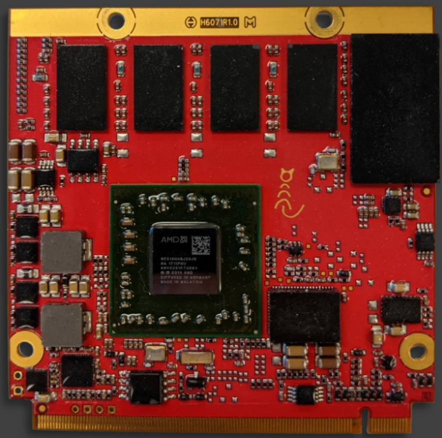


CSP



SSP

- **SHREC Flight Computers**
  - CHREC Space Processor (CSP) – 22.5+ years of flight heritage (7 devices + 3 missions)
  - SHREC Space Processor (SSP) – 4 years of flight heritage (2 devices + 1 mission)
  - Space GPU (SGPU) – Accelerate compression, checksums, and image processing



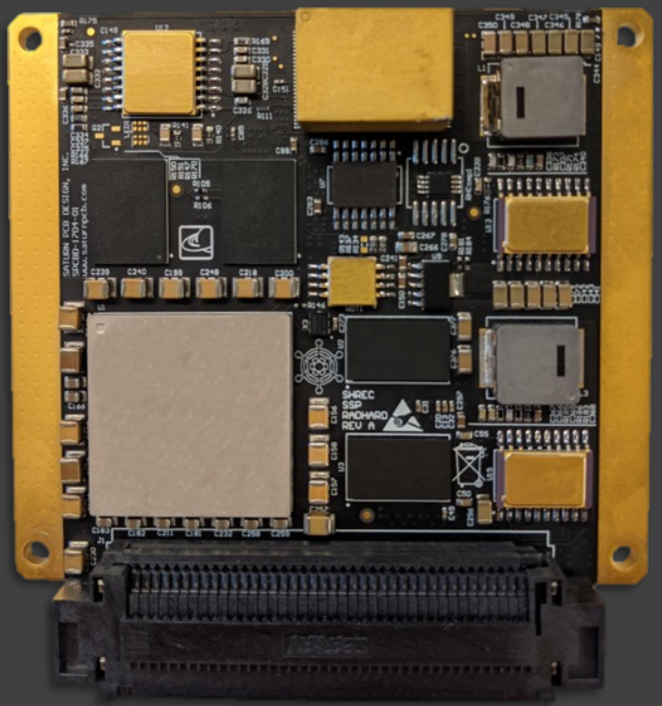
AMD GX-216 SoM

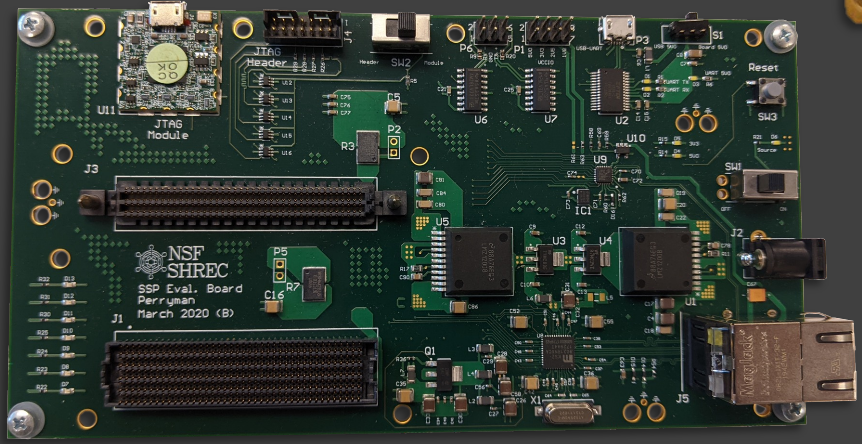
- **Proposed Fourth STP Mission: STP-H12-VANTAGE**
  - Leverage SHREC's existing Earth-observation, processing, and system-development expertise
  - Introduce overlap of visual and neuromorphic data for novel perception and autonomy research

Technologies

SHREC Space Processor (SSP)

- **Hybrid (COTS + Rad-Hard) Single-Board Computer**
- **Leverages Xilinx Zynq-7045 FPGA SoC**
  - Dual-core ARM Cortex-A9 @ 667 MHz
  - Kintex-7 FPGA
- **Additional Specifications:**
  - Radiation-tolerant NAND flash (1 – 4 GB)
  - COTS DDR3 (1 GB PS and 4 GB PL)
  - Dedicated watchdog circuitry
  - Onboard power regulation
  - 28 ARM GPIO pins
  - 62 FPGA I/O pins
  - 8 multi-gigabit transceivers
- **Extensive Mission Heritage on STP-H7-CASPR**



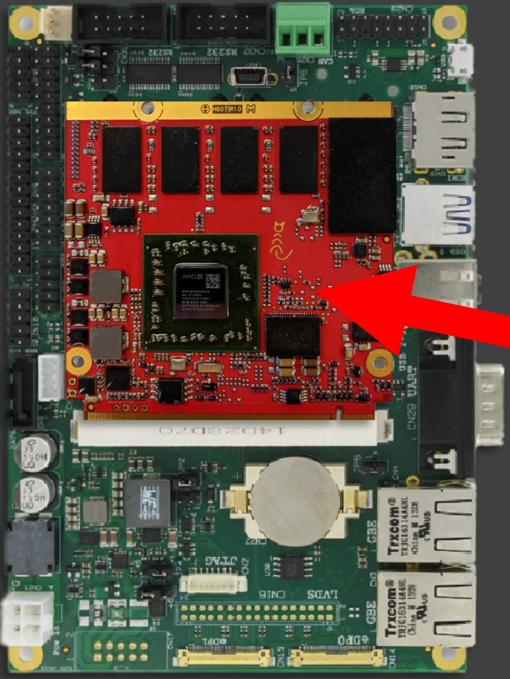


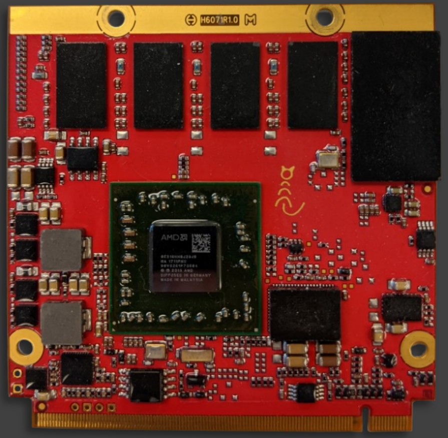
SSP Active Eval Board

System-on-Module Solutions for Space

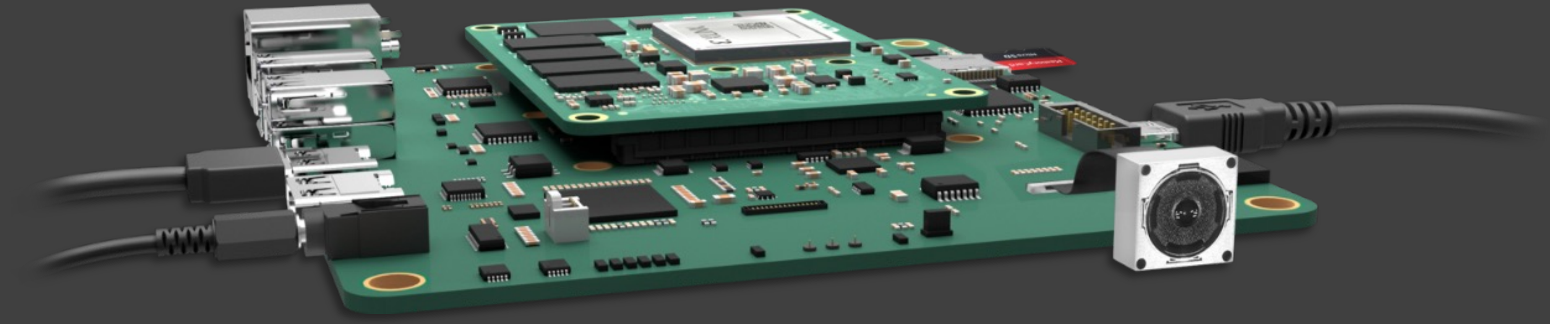
- **System-on-Modules (SoMs)**
  - Commercially-available PCB
    - COTS processor, communications interfaces, memory, etc.
    - High-density board connector(s)
  - Vertically mounted to SoM carrier board
    - Carrier provides connection breakouts/other supporting circuitry
  - Successful flight on STP-H7-CASPR!
    - AMD GX-216HC GPU
    - Custom COTS carrier card with Ethernet communication

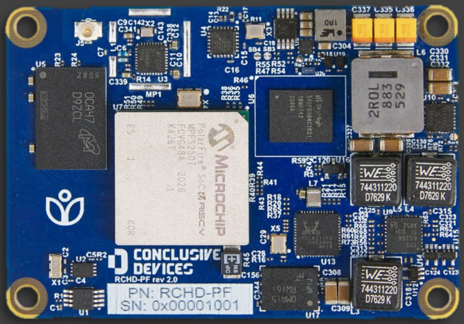
Carrier Board Example





AMD GX-216 SoM

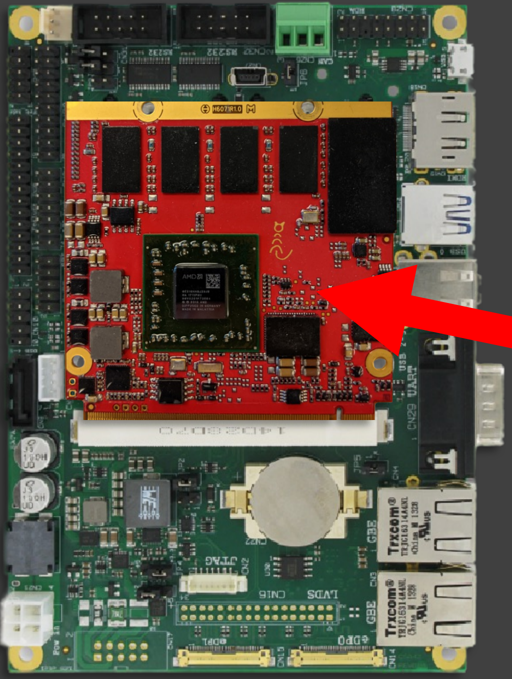


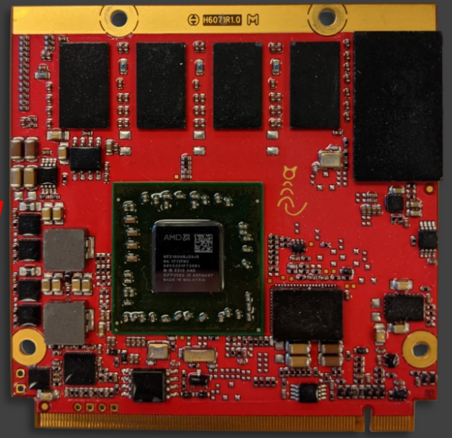


System-on-Module Solutions for Space

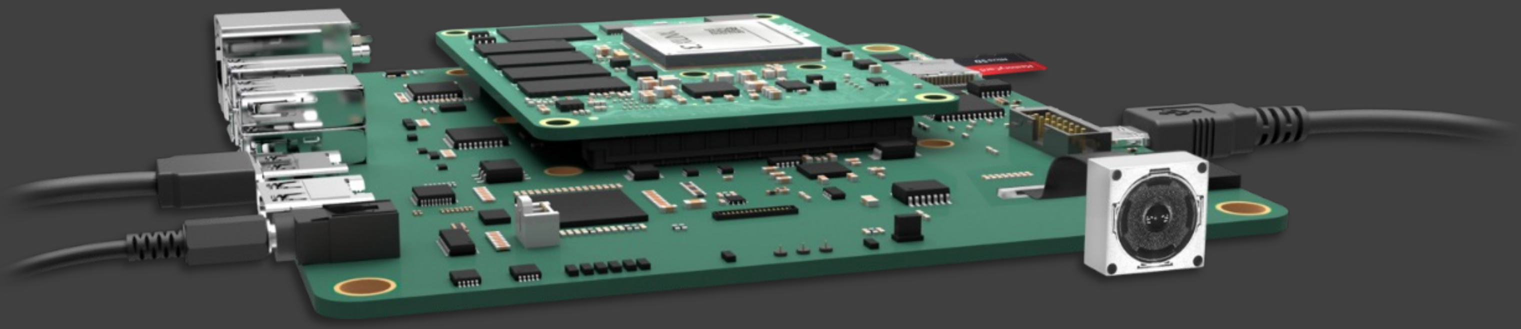
- ***NEW*** **– Hybrid Architectures for SoM Carriers**
  - COTS SoM enables high performance with desired SoC at minimal cost
  - Custom SoM arrier contains rad-hard supporting components
    - Power, data storage, watchdog timing, etc.
  - Enables low-cost prototyping and iterative design
  - Maximizes system dependability
  - Minimizes time to deployment

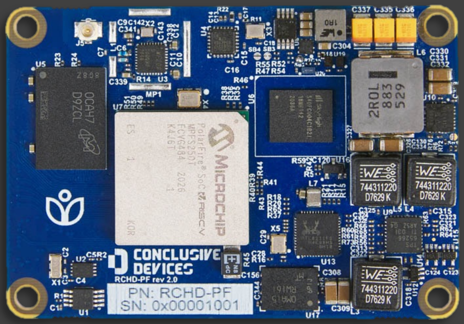
Carrier Board Example





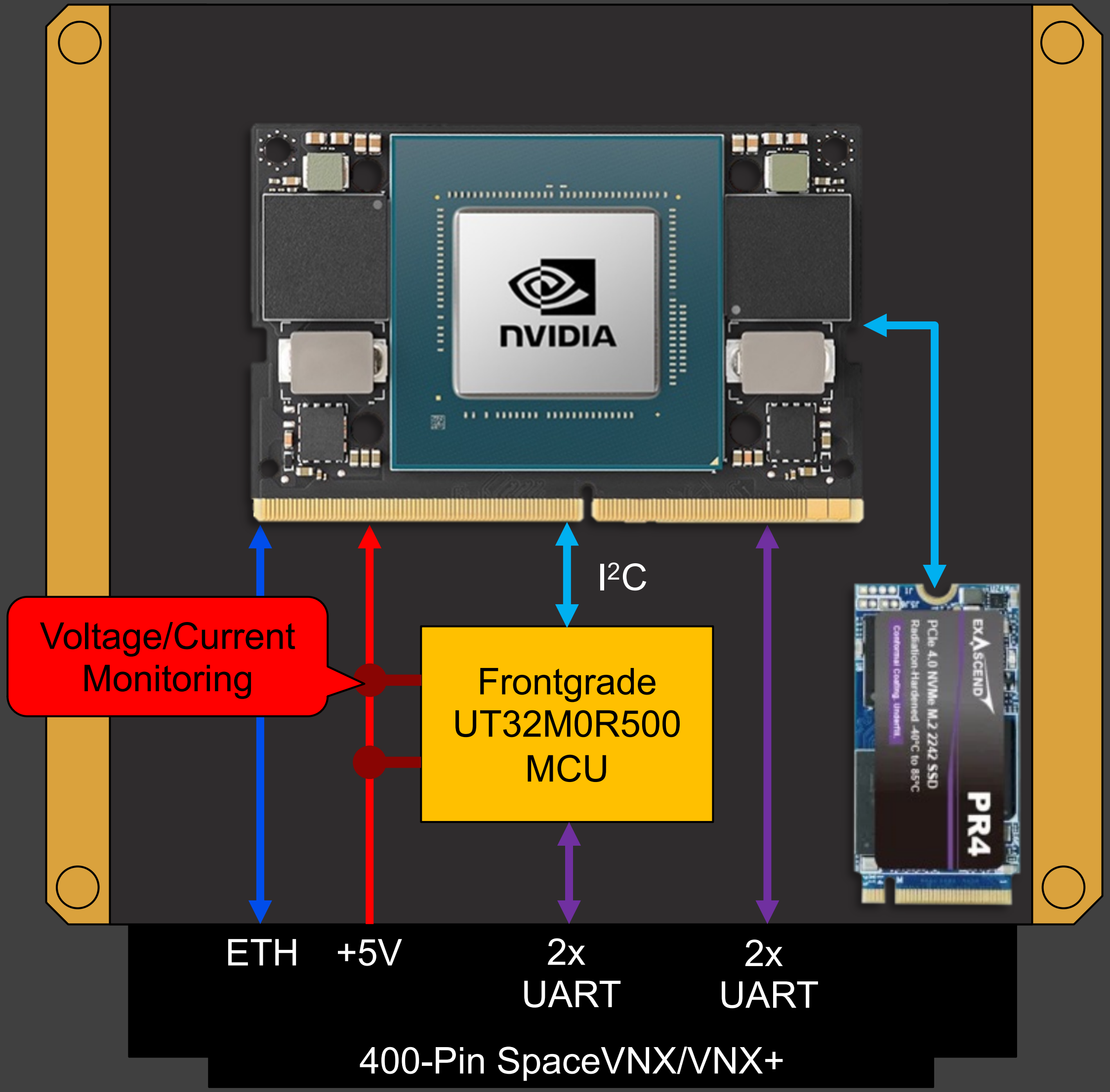
AMD GX-216 SoM





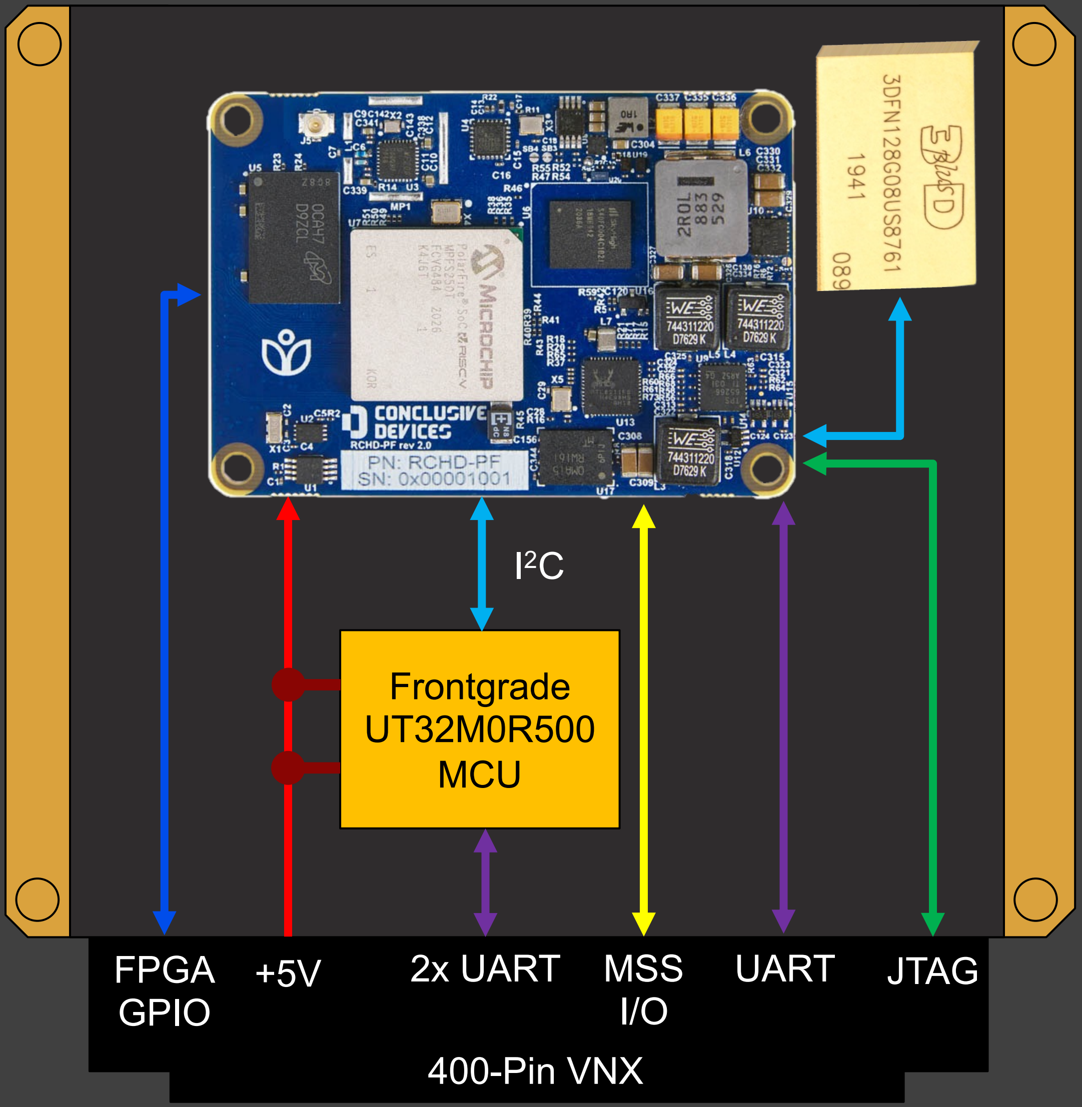
System-on-Module Solutions for Space

- **Hybrid NVIDIA GPU SoM Carrier**
- **COTS NVIDIA Jetson Orin NX 16GB SoM**
  - 1024-core NVIDIA Ampere GPU architecture @ 918 MHz
  - 8-core 64-bit ARM Cortex-A78AE CPU @ 2.2 GHz
  - 16 GB COTS LPDDR5
- **SoM Carrier Incorporates:**
  - Standardized VNX form-factor and pinout
  - UART and Ethernet communications
  - Fault-tolerant Exascend PR4 NVMe non-volatile storage
  - Radiation-tolerant microcontroller
    - Intelligent voltage and current monitoring
    - SoM health and status monitoring
    - Onboard troubleshooting entry point



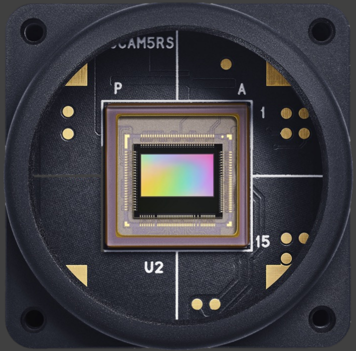
System-on-Module Solutions for Space

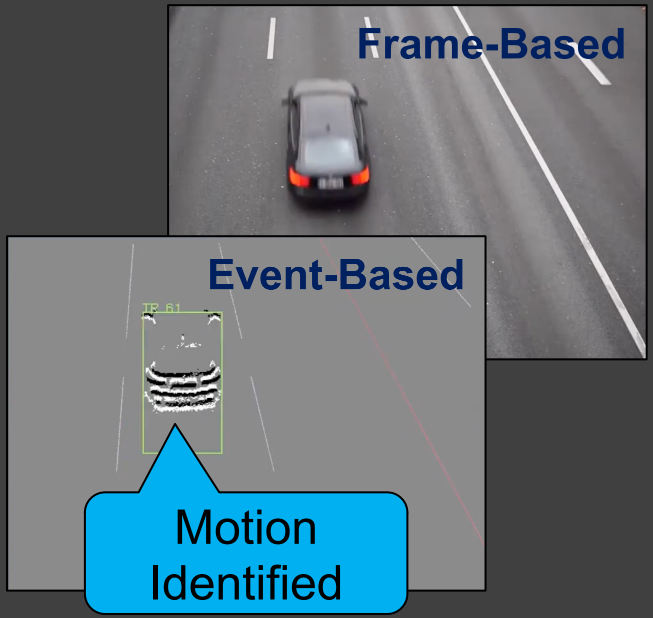
- **Hybrid Microchip PolarFire SoC SoM Carrier**
- **COTS Microchip PolarFire SoC (MPFS250T) SoM**
  - 4-core 64-bit RISC-V GC (SiFive U54) CPU @ 600 MHz
  - PolarFire FPGA fabric
    - 254K logic elements (4-input LUT + DFF)
    - 784 math blocks (18x18 MACC)
- **SoM Carrier Incorporates:**
  - Radiation-tolerant NAND flash
  - Processor I/O (UART, Ethernet, etc.) and FPGA I/O
  - Radiation-tolerant microcontroller
    - Intelligent voltage and current monitoring
    - SoM health and status monitoring
    - Onboard troubleshooting entry point



Neuromorphic Event-Based Sensing

- **Mimics Function and Efficiency of Biological Eye**
  - Only responds when changes ("events") detected
  - Low data rate → data is only produced if events occur
  - Efficient output → Only changes in scene are transmitted
- **High Temporal Resolution**
  - Beneficial for counting/measuring objects, calculating trajectories, identifying onboard vibrations, and more
- **Prophesee + Sony IMX636 Event-Based Sensor**
  - High-definition (1280 x 720 pixels)
  - Sensor peak power consumption <100mW





COTS Catadioptric Lenses

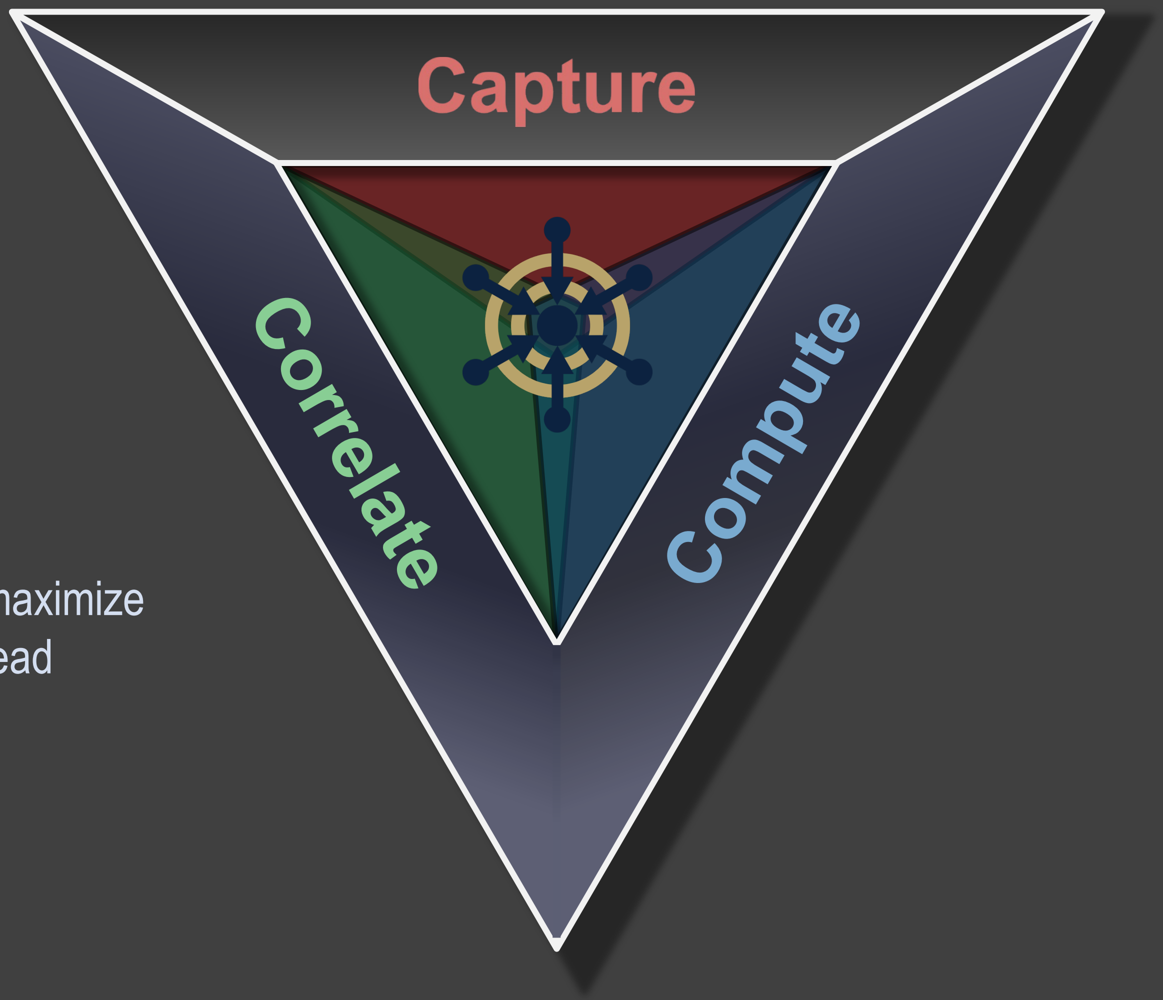
- **Compact and Cost-Effective Telescope-Like Design**
  - Cluster of mirrors and glass lenses place long focal lengths into small and lightweight package
  - Most lenses available for <$500
- **Low-GRD Imaging Opportunities**
  - Estimated ~2.5 meter/pixel imaging with 500mm lens and 4K Sony industrial sensor
  - Lens on neuromorphic sensor will have differing GRD to ensure sufficient swath coverage for data acquisition and triggering
- **Some Challenges**
  - COTS lenses will require either environmental and mechanical testing, or custom mechanical modification, for flight assurance

Tokina SZ SUPER TELE 500mm (Candidate)

Mission Design

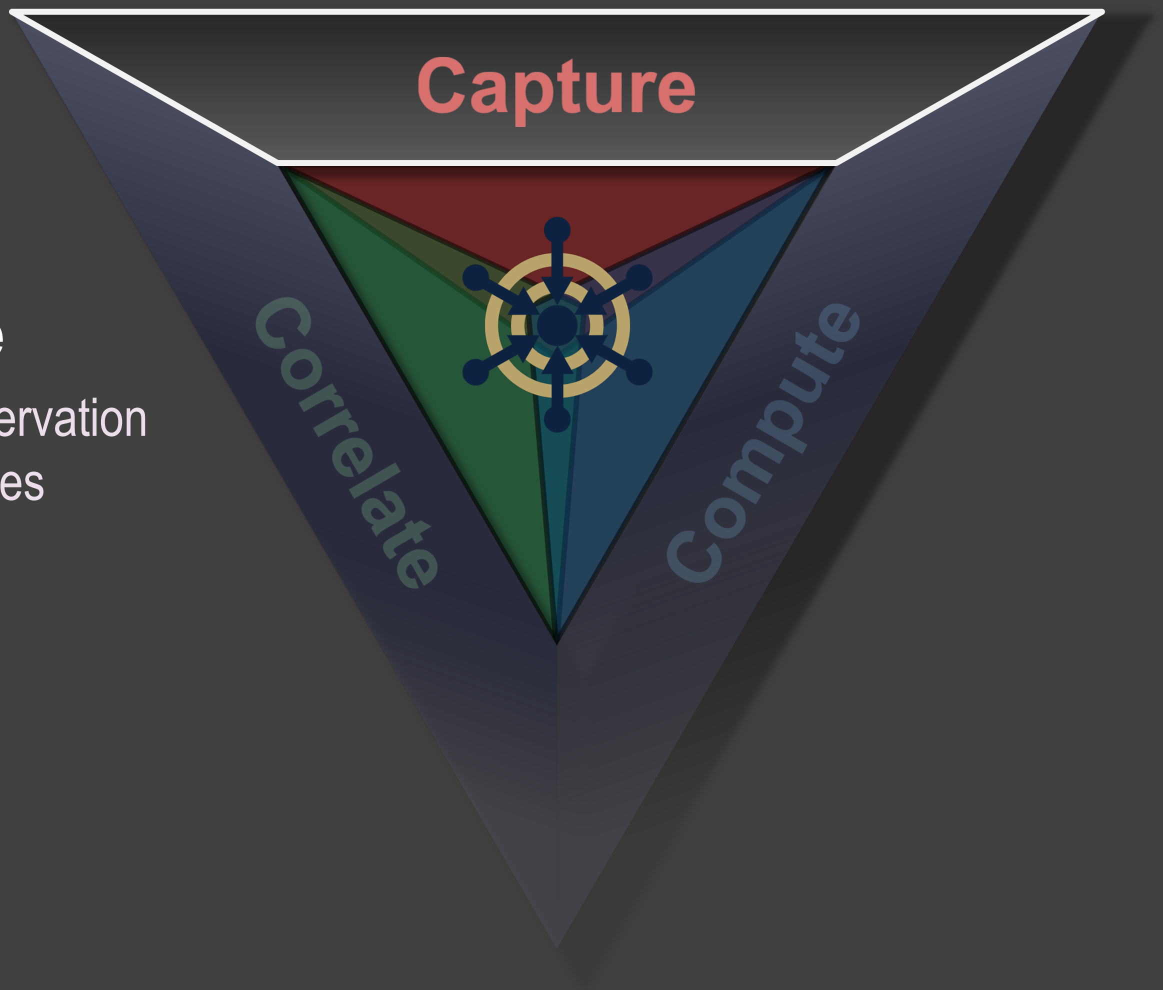
Mission Objectives

- **Three Key Objective Categories**
  - Capture
    - Demonstrate core onboard sensor features and capabilities for Earth observation data capture
  - Correlate
    - Verify sensor correlation operations and begin identification, tracking, and additional science
  - Compute
    - Leverage next-generation hybrid space computing systems to maximize system performance and reliability with minimal cost and overhead



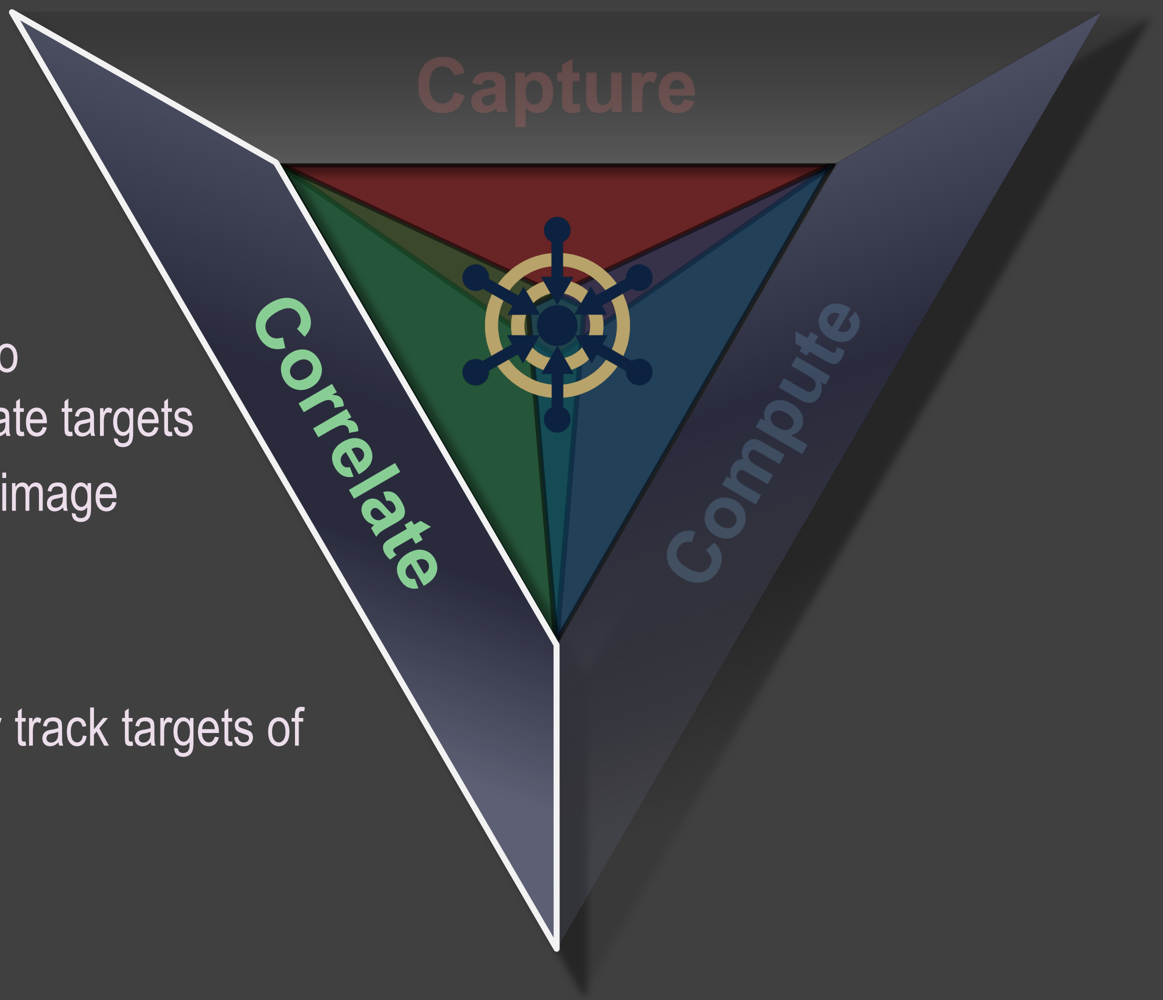
Mission Objectives

- **Mission Objective #1: Low-GRD Image Capture**
  - Experiment with industrial cameras and low-cost optics for low-GRD Earth observation image capture and onboard processing
- **Mission Objective #2: Event-Based Data Capture**
  - Leverage neuromorphic event-based sensors for Earth observation applications and demonstrate onboard processing capabilities



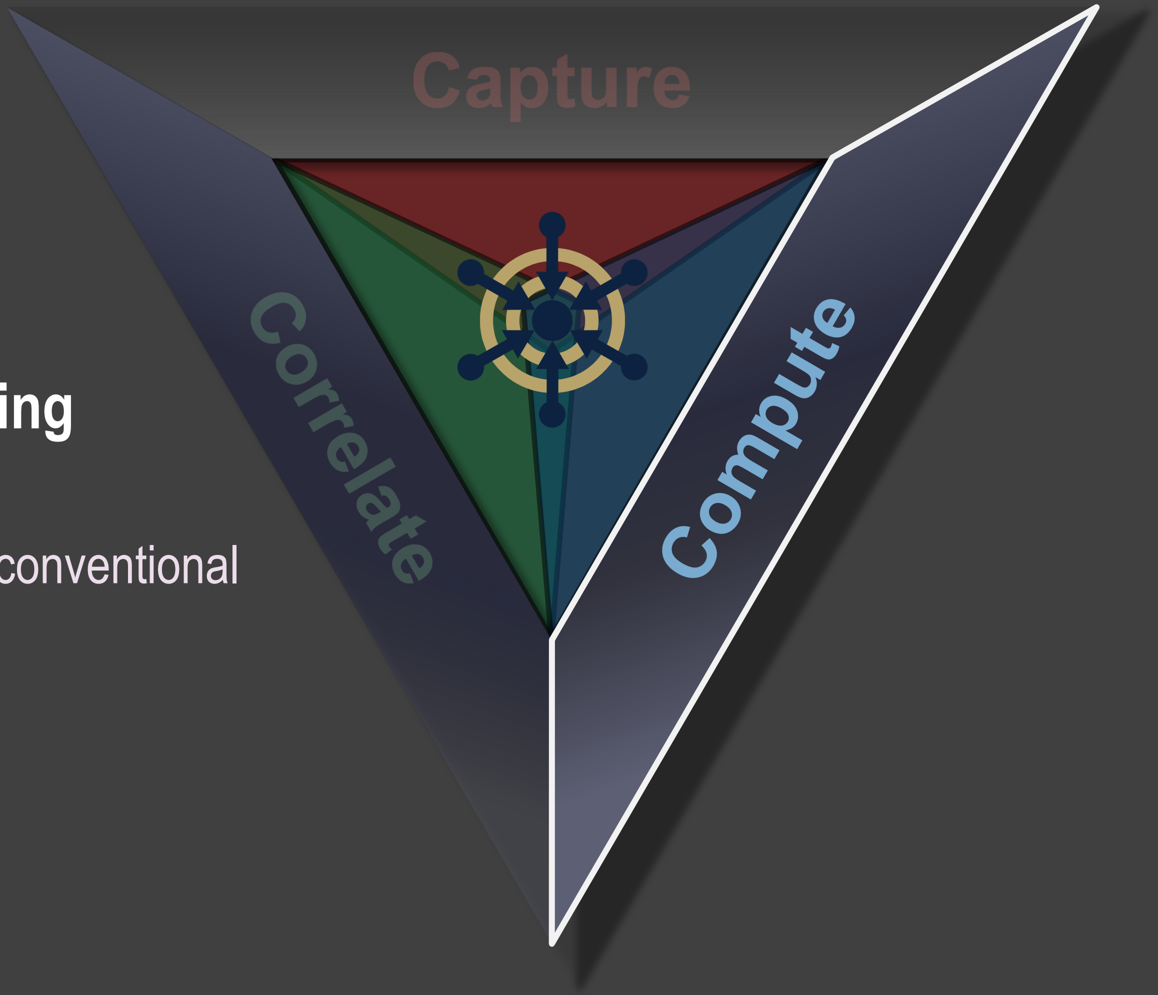
Mission Objectives

- **Mission Objective #3: Sensor Correlation**
  - Demonstrate simultaneous image and neuromorphic data captures and verify overlapping sensor fields of view
- **Mission Objective #4: Intelligent Target Capture**
  - Experiment with overlapping fields of view of both sensors to intelligently trigger the capture of images featuring appropriate targets
  - Record and downlink data to create dataset with correlated image and neuromorphic event-based data
- **Mission Objective #5: Effective Target Tracking**
  - Using onboard sensor suite, enable system to automatically track targets of interest and capture and downlink relevant data



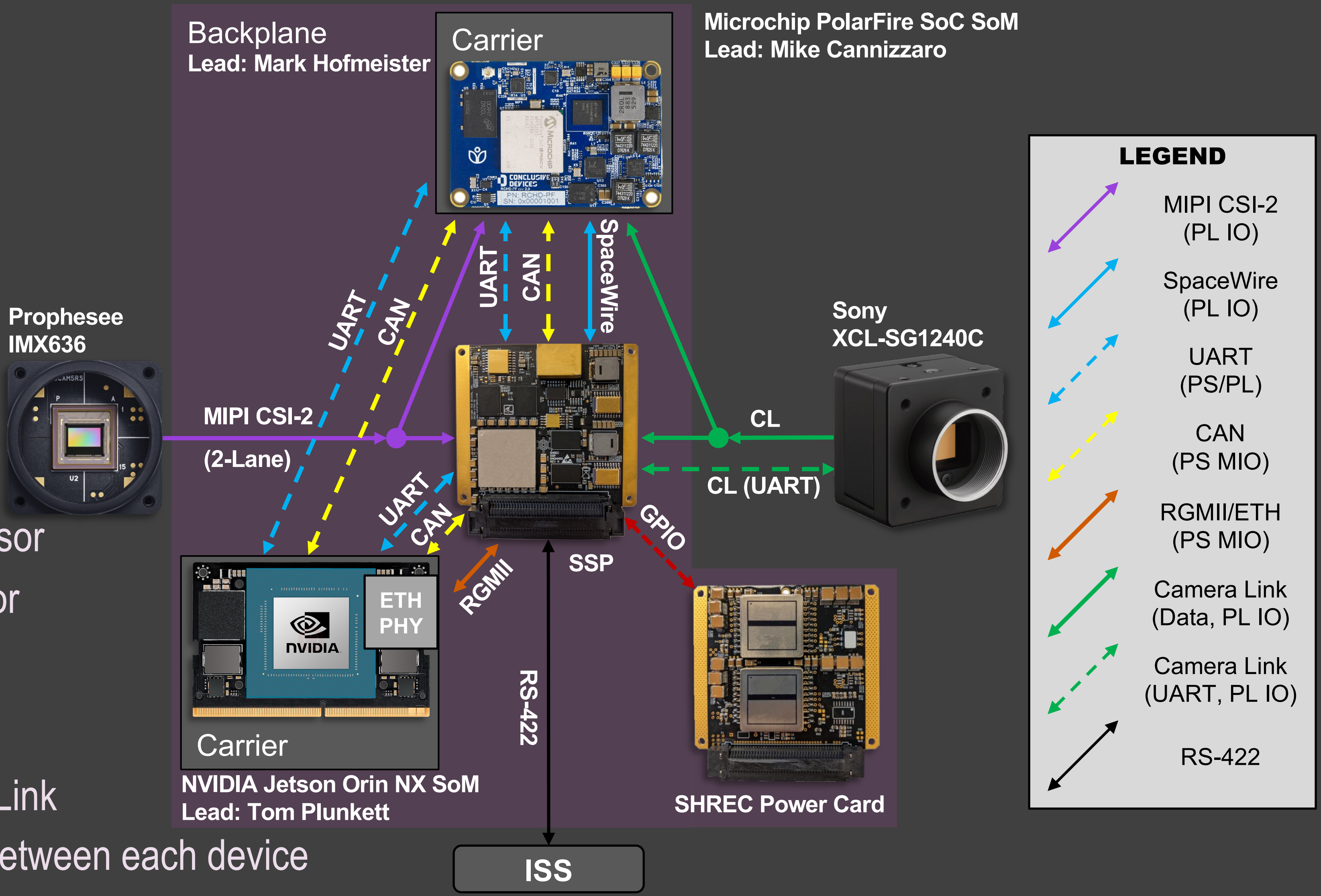
Mission Objectives

- **Mission Objective #6: Accelerated Computer Vision and Machine Learning**
  - Investigate computer vision and machine learning apps on COTS FPGAs, GPUs, and multicore CPUs to evaluate onboard processing capabilities
- **Mission Objective #7: End-to-End Onboard Sensing and Intelligent Processing**
  - Demonstrate end-to-end enterprise capability with onboard conventional and event-based sensing via COTS processing



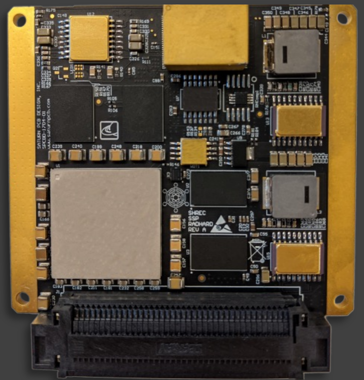
VANTAGE System Architecture

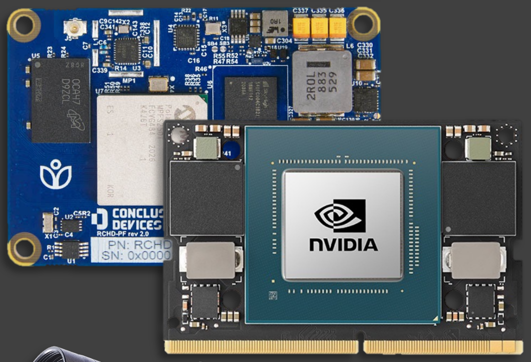
- **Computing Chassis**
  - 1x SSP (main node)
  - 2x Hybrid SoM carriers
    - NVIDIA Jetson SoM
    - PolarFire SoC SoM
  - 1x SHREC power card
- **Dual-Sensor System**
  - 1x Sony IMX636 neuromorphic sensor
  - 1x Sony XCL-SG1240C RGB sensor
- **Data Connections**
  - Ethernet, SpaceWire, and Camera Link
  - Redundant UART communication between each device



Hardware

Electrical Hardware Specifications

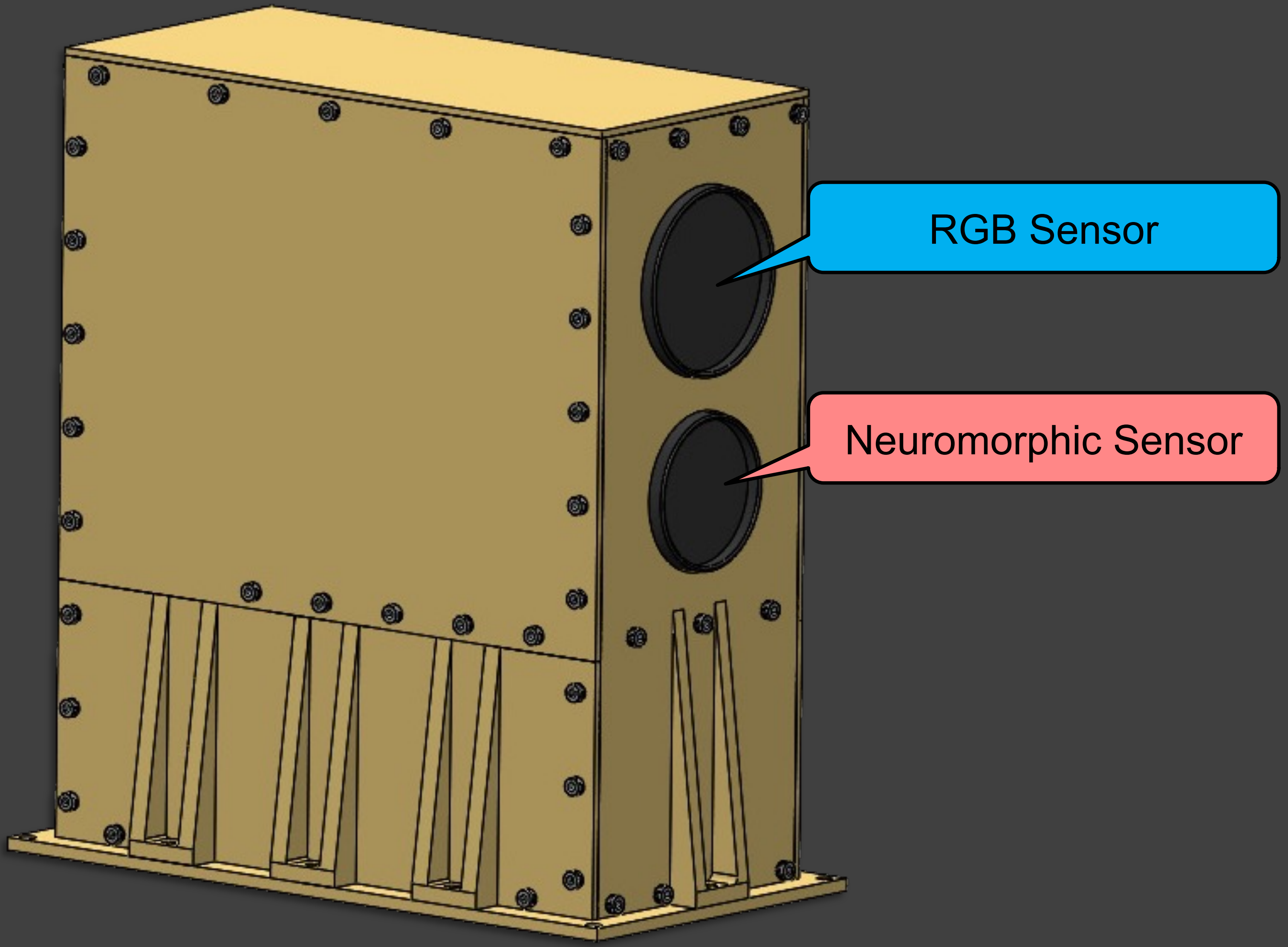




Node	Size	Nominal Power	Peak Power	General Specifications	Processor Specifications	FPGA Specifications
SSP (Xilinx Zynq-7045) (Main Node)	1U	~4 W	~14 W	–	2x 32-bit ARM Cortex-A9 @ 667 MHz PS RAM: 1 GB DDR3	350K Logic Cells PL RAM: 4 GB
PolarFire SoC MPFS250T (Compute SoM)	1U (Estimated)	~7.5 W	Unknown ~14.0 W Est.	–	4x 64-bit RISC-V @ 625 MHz PS RAM: Up to 4 GB DDR4	254K Logic Cells PL RAM: Up to 4 GB DDR4
NVIDIA Jetson Orin NX 16 GB (GPU SoM)	1U (Estimated)	10 W	25 W	16 GB LPDDR5	8x 64-bit ARM Cortex-A78 @ 2 GHz (Max) 1024x NVIDIA Ampere @ 918 MHz (Max)	N/A
Prophesee CCAM5 (Neuromorphic Sensor)	1U (Estimated) (Includes Optics)	~0.5 W	1.5 W	Sony IMX636 1280 x 720 Event-Based Sensor	N/A	N/A
Sony XCL-SG1240C (Visual Sensor)	1U (Estimated) (Includes Optics)	Unknown	3.8 W	12 MP RGB Sensor	N/A	N/A

Peak Power
~60 W

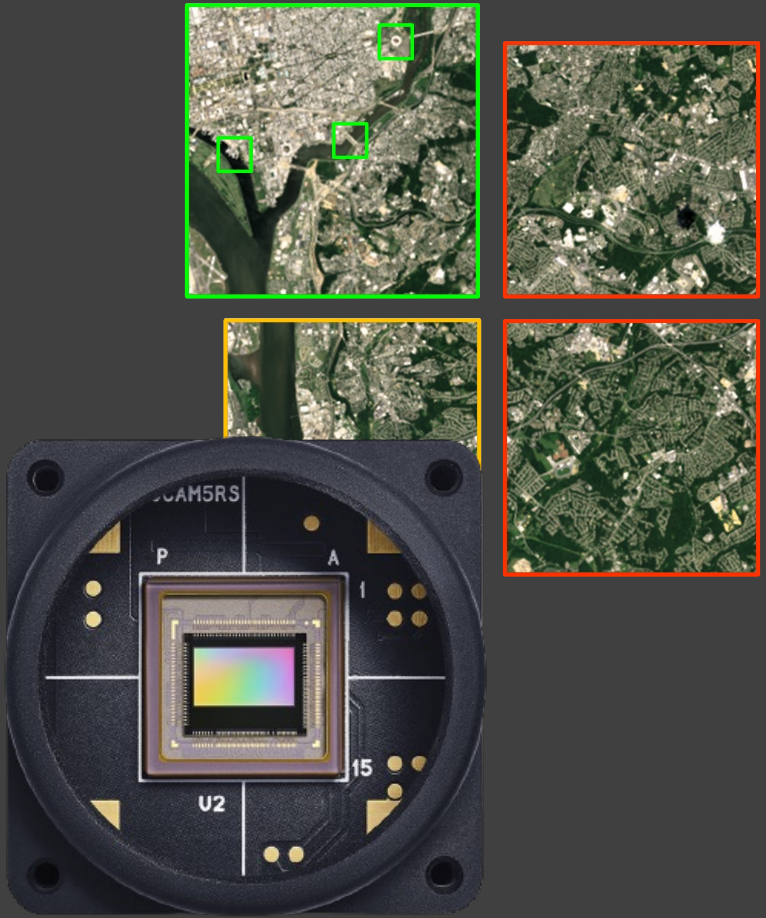
Mechanical Model



Apps and Services

Apps and Services

- **Next-Generation Autonomous Imaging Pipeline**
  - Tile classification, semantic segmentation, and other deep-learning models
  - CNNJPEG compression, further autonomous app calls, downlink, and storage
- **SHREC Neuromorphic App Suite**
  - Event-based tracking
  - hARMS event-based optical flow algorithms
  - Spiking neural-network framework implemented on FPGA
- **Shared Field of View for Visual and Neuromorphic Sensors**
  - Track objects with neuromorphic sensor and capture visuals at ideal time
  - Gather unique dataset combining advantages of neuro and visual



Timeline

Schedule

Flight Request
Spring 2024
COMPLETED

SERB Presentations
Spring 2024
COMPLETED

STP-H12 Kickoff
April 2025

STP-H12 PDR
September 2025

STP-H12 CDR
April 2026

STP-H12 FCA
June 2026

STP-H12 On-Dock
July 2026

Conclusions

- **Computing Focus with Scientific Impact**
  - Leverage SHREC expertise in hybrid space computing architectures
  - Integrate ongoing Earth observation and neuromorphic research

- **Simplified Design Without Compromise**
  - Reduced complexity and power compared to CASPR
  - Novel SoM approach enables doing more with less

- **Next Steps**
  - Secure additional funding for parts and manufacturing
  - Complete prototype designs and begin initial fabrication
  - Conduct in-house validation of optical hardware

Want More Information?

Dr. Alan D. George (PI), Department Chair, R&H Mickle Endowed Chair, Professor of ECE, and NSF SHREC Center Director

NSF Center for Space, High-Performance, and Resilient Computing (SHREC)
ECE Department, University of Pittsburgh
1238D Benedum Hall, 3700 O'Hara Street Pittsburgh, PA 15261 (412) 624-9664
Email: alan.george@pitt.edu

Mike Cannizzaro, VANTAGE Payload Manager

Email: mjc153@pitt.edu

Visit the VANTAGE Website!
http://www.shrec-vantage.space

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