Contribution: Yitong Li mainly finish the exercise 1 and Guoqing Liang mainly finish the exercise 2. Code Link：[CHU-2002/DD2360HT23 (github.com)](https://github.com/CHU-2002/DD2360HT23)

#### Exercise 1

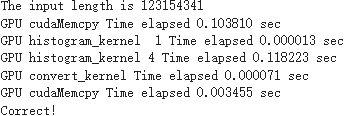
1. **Describe all optimizations you tried regardless of whether you committed to them or abandoned them and whether they improved or hurt performance**
2. I tried use shard memory in kernel fuction, but there’s no obvious effect.

As far as I’m concerned, the reason is the kernel cost only little time, even in the following example, 123154341, the kernel only cost 0.000013s. So Even the shared memory accelerate the computation, it is hard to detect.

I test 5 times for each method, here is the results(length = 123156789,time of kernal):

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| shared | 0.000024s | 0.000014 | 0.000013 | 0.000022 | 0.000018 |
| golobal | 0.000014 | 0.000016 | 0.000012 | 0.000015 | 0.000012 |

On average, 0.000004 seconds faster with shared memory.



1. I tried use streams, but because of the time cost in memory copy, it is hard to detect optimazation. As shown in FIG. The time kernel cost is ignorable.
2. **Which optimizations you chose in the end and why?**

Although the effect is not obvious, I still chose the above two optimizations. The reasons refer to the above description. In theory, these two optimizations are effective but little.

1. **How many global memory reads are being performed by your kernel? Explain**

For each data, read 1 time. To sum the results, each block read MUN\_BINS times. So the number of reads of global memory is inputLength + MUM\_BINS \* MUM\_Block = inputLength + 4,194,304.

1. **How many atomic operations are being performed by your kernel? Explain**

For each data, once. To sum the results, each block atinucAdd MUN\_BINS times. So the number of reads of global memory is inputLength + MUM\_BINS \* MUM\_Block = inputLength + 4,194,304.

1. **How much shared memory is used in your code? Explain**

For each Block, 4096 \* 4bytes. So MUM\_Block \* 4096\* 4bytes =16.78MB

T4 provide 49152bytes per block, which is Sufficient for it.

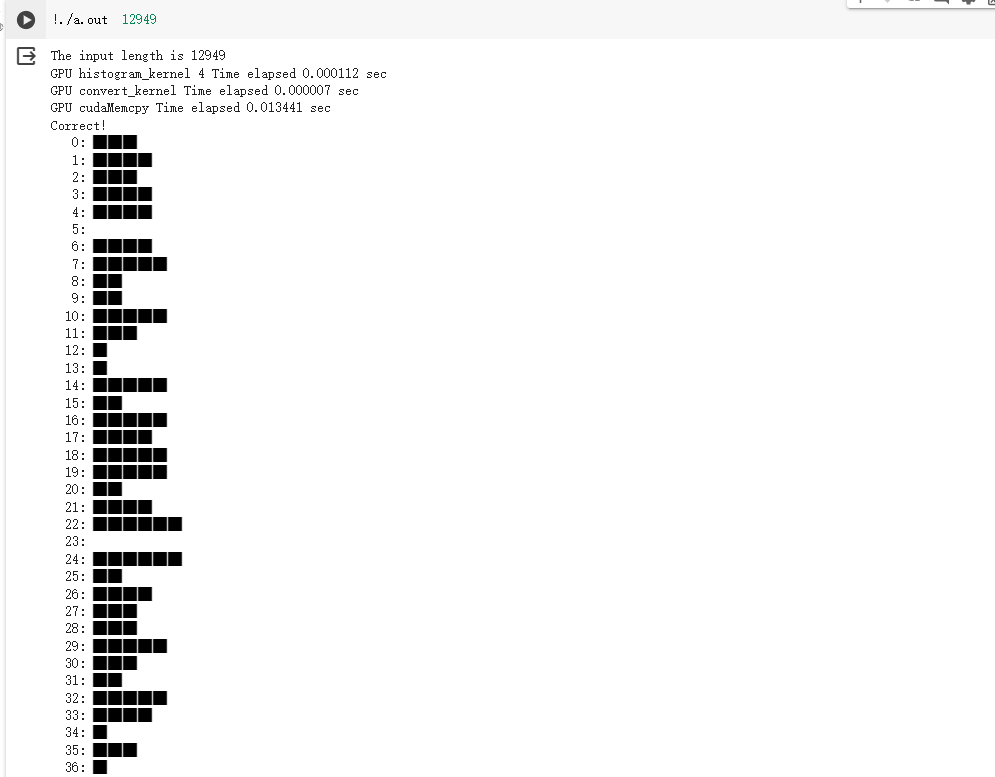
1. **How would the value distribution of the input array affect the contention among threads? For instance, what contentions would you expect if every element in the array has the same value?**

The more concentrated the distribution, the more severe the contention. Because of the atomic operation, if two threads add to one bin, the contention occurred. So if every element in the array has the same value, contention will occur in each thread.

1. **Plot a histogram generated by your code and specify your input length, thread block and grid.**

Input length is 12949, gird is 1024 and block is 1024.

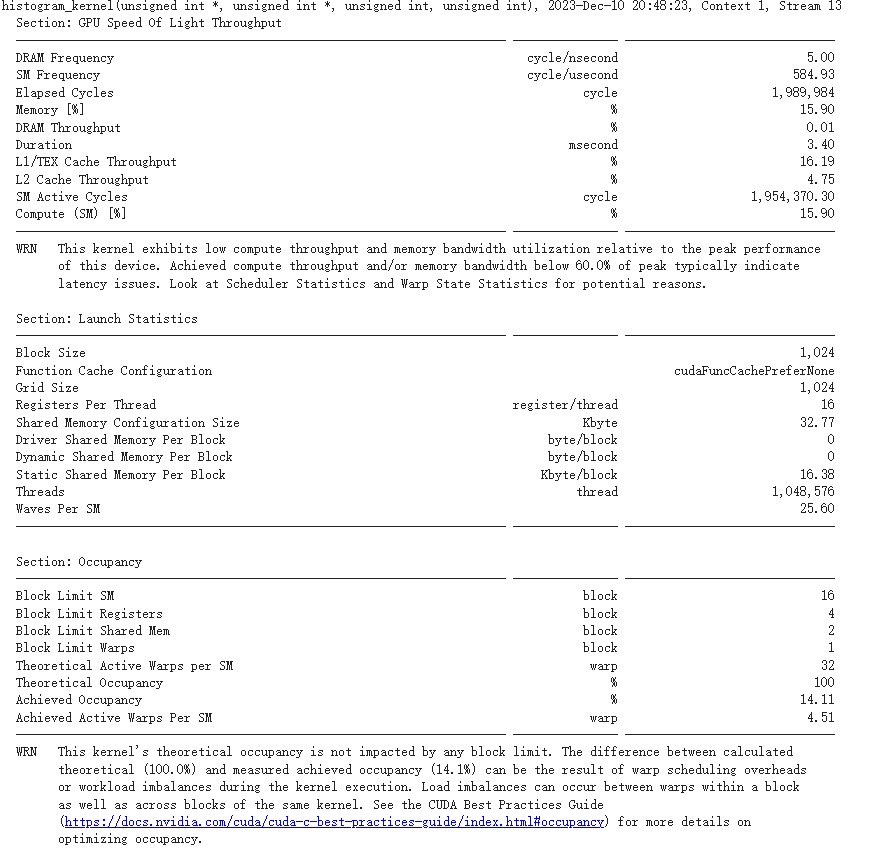
Here is a screen shot of the Top results. Please check the appendix A to check the full results.



1. **For a input array of 1024 elements, profile with Nvidia Nsight and report Shared Memory Configuration Size and Achieved Occupancy. Did Nvsight report any potential performance issues?**

Please check the appendix B to get the full results.

As the screen shot following. Shared Memory Configuration Size is 32.77 Kb. And static shared memory per block is 16.38 bytes. Here is no issues. Achieved Occupancy is 14.11%, here is no issues too.



#### Exercise 2

1. \_\_global\_\_ void MoverKernel(struct particles\* part, struct EMfield\* field, struct grid\* grd, struct parameters\* param){
2. int i = threadIdx.x + blockIdx.x \* blockDim.x;
3. if(i < part->nop){
4. *// auxiliary variables*
5. FPpart dt\_sub\_cycling = (FPpart) param->dt/((double) part->n\_sub\_cycles);
6. FPpart dto2 = .5\*dt\_sub\_cycling, qomdt2 = part->qom\*dto2/param->c;
7. FPpart omdtsq, denom, ut, vt, wt, udotb;
9. *// local (to the particle) electric and magnetic field*
10. FPfield Exl=0.0, Eyl=0.0, Ezl=0.0, Bxl=0.0, Byl=0.0, Bzl=0.0;
12. *// interpolation densities*
13. int ix,iy,iz;
14. FPfield weight[2][2][2];
15. FPfield xi[2], eta[2], zeta[2];
17. *// intermediate particle position and velocity*
18. FPpart xptilde, yptilde, zptilde, uptilde, vptilde, wptilde;
19. xptilde = part->x[i];
20. yptilde = part->y[i];
21. zptilde = part->z[i];
22. *// calculate the average velocity iteratively*
23. for(int innter=0; innter < part->NiterMover; innter++){
24. *// interpolation G-->P*
25. ix = 2 +  int((part->x[i] - grd->xStart)\*grd->invdx);
26. iy = 2 +  int((part->y[i] - grd->yStart)\*grd->invdy);
27. iz = 2 +  int((part->z[i] - grd->zStart)\*grd->invdz);
29. *// calculate weights*
30. xi[0]   = part->x[i] - grd->XN[ix - 1][iy][iz];
31. eta[0]  = part->y[i] - grd->YN[ix][iy - 1][iz];
32. zeta[0] = part->z[i] - grd->ZN[ix][iy][iz - 1];
33. xi[1]   = grd->XN[ix][iy][iz] - part->x[i];
34. eta[1]  = grd->YN[ix][iy][iz] - part->y[i];
35. zeta[1] = grd->ZN[ix][iy][iz] - part->z[i];
36. for (int ii = 0; ii < 2; ii++)
37. for (int jj = 0; jj < 2; jj++)
38. for (int kk = 0; kk < 2; kk++)
39. weight[ii][jj][kk] = xi[ii] \* eta[jj] \* zeta[kk] \* grd->invVOL;
41. *// set to zero local electric and magnetic field*
42. Exl=0.0, Eyl = 0.0, Ezl = 0.0, Bxl = 0.0, Byl = 0.0, Bzl = 0.0;
44. for (int ii=0; ii < 2; ii++)
45. for (int jj=0; jj < 2; jj++)
46. for(int kk=0; kk < 2; kk++){
47. Exl += weight[ii][jj][kk]\*field->Ex[ix- ii][iy -jj][iz- kk ];
48. Eyl += weight[ii][jj][kk]\*field->Ey[ix- ii][iy -jj][iz- kk ];
49. Ezl += weight[ii][jj][kk]\*field->Ez[ix- ii][iy -jj][iz -kk ];
50. Bxl += weight[ii][jj][kk]\*field->Bxn[ix- ii][iy -jj][iz -kk ];
51. Byl += weight[ii][jj][kk]\*field->Byn[ix- ii][iy -jj][iz -kk ];
52. Bzl += weight[ii][jj][kk]\*field->Bzn[ix- ii][iy -jj][iz -kk ];
53. }
55. *// end interpolation*
56. omdtsq = qomdt2\*qomdt2\*(Bxl\*Bxl+Byl\*Byl+Bzl\*Bzl);
57. denom = 1.0/(1.0 + omdtsq);
58. *// solve the position equation*
59. ut= part->u[i] + qomdt2\*Exl;
60. vt= part->v[i] + qomdt2\*Eyl;
61. wt= part->w[i] + qomdt2\*Ezl;
62. udotb = ut\*Bxl + vt\*Byl + wt\*Bzl;
63. *// solve the velocity equation*
64. uptilde = (ut+qomdt2\*(vt\*Bzl -wt\*Byl + qomdt2\*udotb\*Bxl))\*denom;
65. vptilde = (vt+qomdt2\*(wt\*Bxl -ut\*Bzl + qomdt2\*udotb\*Byl))\*denom;
66. wptilde = (wt+qomdt2\*(ut\*Byl -vt\*Bxl + qomdt2\*udotb\*Bzl))\*denom;
67. *// update position*
68. part->x[i] = xptilde + uptilde\*dto2;
69. part->y[i] = yptilde + vptilde\*dto2;
70. part->z[i] = zptilde + wptilde\*dto2;

73. } *// end of iteration*
74. *// update the final position and velocity*
75. part->u[i]= 2.0\*uptilde - part->u[i];
76. part->v[i]= 2.0\*vptilde - part->v[i];
77. part->w[i]= 2.0\*wptilde - part->w[i];
78. part->x[i] = xptilde + uptilde\*dt\_sub\_cycling;
79. part->y[i] = yptilde + vptilde\*dt\_sub\_cycling;
80. part->z[i] = zptilde + wptilde\*dt\_sub\_cycling;

83. *//////////*
84. *//////////*
85. *////////// BC*
87. *// X-DIRECTION: BC particles*
88. if (part->x[i] > grd->Lx){
89. if (param->PERIODICX==true){ *// PERIODIC*
90. part->x[i] = part->x[i] - grd->Lx;
91. } else { *// REFLECTING BC*
92. part->u[i] = -part->u[i];
93. part->x[i] = 2\*grd->Lx - part->x[i];
94. }
95. }
97. if (part->x[i] < 0){
98. if (param->PERIODICX==true){ *// PERIODIC*
99. part->x[i] = part->x[i] + grd->Lx;
100. } else { *// REFLECTING BC*
101. part->u[i] = -part->u[i];
102. part->x[i] = -part->x[i];
103. }
104. }

107. *// Y-DIRECTION: BC particles*
108. if (part->y[i] > grd->Ly){
109. if (param->PERIODICY==true){ *// PERIODIC*
110. part->y[i] = part->y[i] - grd->Ly;
111. } else { *// REFLECTING BC*
112. part->v[i] = -part->v[i];
113. part->y[i] = 2\*grd->Ly - part->y[i];
114. }
115. }
117. if (part->y[i] < 0){
118. if (param->PERIODICY==true){ *// PERIODIC*
119. part->y[i] = part->y[i] + grd->Ly;
120. } else { *// REFLECTING BC*
121. part->v[i] = -part->v[i];
122. part->y[i] = -part->y[i];
123. }
124. }
126. *// Z-DIRECTION: BC particles*
127. if (part->z[i] > grd->Lz){
128. if (param->PERIODICZ==true){ *// PERIODIC*
129. part->z[i] = part->z[i] - grd->Lz;
130. } else { *// REFLECTING BC*
131. part->w[i] = -part->w[i];
132. part->z[i] = 2\*grd->Lz - part->z[i];
133. }
134. }
136. if (part->z[i] < 0){
137. if (param->PERIODICZ==true){ *// PERIODIC*
138. part->z[i] = part->z[i] + grd->Lz;
139. } else { *// REFLECTING BC*
140. part->w[i] = -part->w[i];
141. part->z[i] = -part->z[i];
142. }
143. }
144. }
145. }
146. */\*\* particle mover \*/*
147. int mover\_PC(struct particles\* h\_part, struct EMfield\* h\_field, struct grid\* h\_grd, struct parameters\* h\_param)
148. {
149. *// print species and subcycling*
150. std::cout << "\*\*\*  MOVER with SUBCYCLYING "<< h\_param->n\_sub\_cycles << " - species " << h\_part->species\_ID << " \*\*\*" << std::endl;
152. *// start subcycling*
153. for (int i\_sub=0; i\_sub <  h\_part->n\_sub\_cycles; i\_sub++){
154. int ThreadsPerBlock = 256;
155. int BlocksPerGrid = (h\_part->nop + ThreadsPerBlock - 1)/ThreadsPerBlock;
156. particles  \*part;
157. EMfield   \*field;
158. grid    \*grd;
159. parameters \*param;
160. cudaMalloc( &part  , sizeof(particles));
161. cudaMalloc( &field , sizeof(EMfield));
162. cudaMalloc( &grd   , sizeof(grid));
163. cudaMalloc( &param , sizeof(parameters));
164. cudaMemcpy( part,  h\_part,  sizeof(particles),  cudaMemcpyHostToDevice);
165. cudaMemcpy( field, h\_field, sizeof(EMfield),    cudaMemcpyHostToDevice);
166. cudaMemcpy( grd,   h\_grd,   sizeof(grid),       cudaMemcpyHostToDevice);
167. cudaMemcpy( param, h\_param, sizeof(parameters), cudaMemcpyHostToDevice);

170. *// move each particle with new fields*
171. MoverKernel<<<BlocksPerGrid, ThreadsPerBlock>>>(part, field, grd, param);
172. cudaMemcpy( h\_part,  part,  sizeof(particles),  cudaMemcpyDeviceToHost);
173. cudaMemcpy( h\_field, field, sizeof(EMfield),    cudaMemcpyDeviceToHost);
174. cudaMemcpy( h\_grd,   grd,   sizeof(grid),       cudaMemcpyDeviceToHost);
175. cudaMemcpy( h\_param, param, sizeof(parameters), cudaMemcpyDeviceToHost);
176. cudaFree(part);
177. cudaFree(field);
178. cudaFree(grd);
179. cudaFree(param);
180. } *// end of one particle*
182. return(0); *// exit succcesfully*
183. } *// end of the mover*
184. **Describe the environment you used, what changes you made to the Makefile, and how you ran the simulation.**

The code was run on Google Colab T4 GPU. To make Makefile work correctly, I changed ARCH from “sm\_30” to “sm\_75”, which stands for the latest version of NVIDIA GPU. After executing Makefile, a new file ‘sputniPIC.out’ was created and it can be used to ran the simulation.

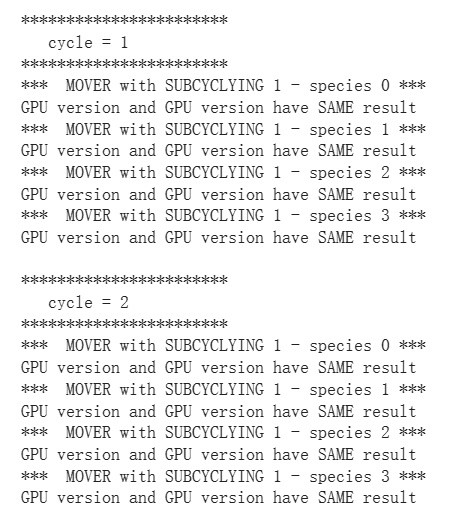
1. **Describe your design of the GPU implementation of mover\_PC() briefly.**

To enhance the performance of mover\_PC(), a new global kernel ‘MoverKernel’ was created to conduct the calculation the average velocity of particles. When we need to move particle, the kernel will called and the calculation will be carried out in parallel on GPU.

1. **Compare the output of both CPU and GPU implementation to guarantee that your GPU implementations produce correct answers.**

Calling the original implementation function and comparePart() at the end of mover\_pc() to compare the result of two versions. The result shows that two version conduct same operation on particle.

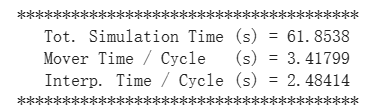
1. void comparePart(struct particles\* part1, struct particles\* part2){
2. bool result = true;
3. for (int i=0; i <  part1->nop; i++){
4. if(part1->x[i] != part2->x[i] || part1->y[i] != part2->y[i] || part1->z[i] != part2->z[i]||
5. part1->u[i] != part2->u[i] || part1->v[i] != part2->v[i] || part1->w[i] != part2->w[i]){
6. result = false;
7. }
8. }
9. if(result){
10. std::cout <<"GPU version and GPU version have SAME result "<< std::endl;
11. }
12. else{
13. std::cout <<"GPU version and GPU version have DIFFERENT result "<< std::endl;
14. }
15. }



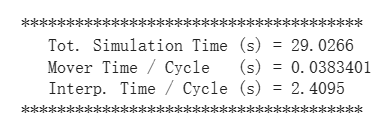
1. **Compare the execution time of your GPU implementation with its CPU version.**

Comparing to CPU version, the running time of the GPU version has significantly decreased.

CPU version:



GPU version:



### Appendix A:

Results of EX1, question 7:

The input length is 12949

GPU histogram\_kernel 4 Time elapsed 0.000112 sec

GPU convert\_kernel Time elapsed 0.000007 sec

GPU cudaMemcpy Time elapsed 0.013441 sec

Correct!

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### Appendix B:

==PROF== Connected to process 41400 (/content/drive/MyDrive/Assignment3/a.out)

The input length is 1024

==PROF== Profiling "histogram\_kernel" - 0: 0%....50%....100% - 8 passes

==PROF== Profiling "histogram\_kernel" - 1: 0%....50%....100% - 8 passes

==PROF== Profiling "histogram\_kernel" - 2: 0%....50%....100% - 8 passes

==PROF== Profiling "histogram\_kernel" - 3: 0%....50%....100% - 8 passes

GPU histogram\_kernel 4 Time elapsed 0.955816 sec

==PROF== Profiling "convert\_kernel" - 4: 0%....50%....100% - 8 passes

GPU convert\_kernel Time elapsed 0.151852 sec

GPU cudaMemcpy Time elapsed 0.000062 sec

Correct!

==PROF== Disconnected from process 41400

[41400] a.out@127.0.0.1

histogram\_kernel(unsigned int \*, unsigned int \*, unsigned int, unsigned int), 2023-Dec-10 20:48:23, Context 1, Stream 13

Section: GPU Speed Of Light Throughput

---------------------------------------------------------------------- --------------- ------------------------------

DRAM Frequency cycle/nsecond 5.00

SM Frequency cycle/usecond 584.93

Elapsed Cycles cycle 1,989,984

Memory [%] % 15.90

DRAM Throughput % 0.01

Duration msecond 3.40

L1/TEX Cache Throughput % 16.19

L2 Cache Throughput % 4.75

SM Active Cycles cycle 1,954,370.30

Compute (SM) [%] % 15.90

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance

of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate

latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Section: Launch Statistics

---------------------------------------------------------------------- --------------- ------------------------------

Block Size 1,024

Function Cache Configuration cudaFuncCachePreferNone

Grid Size 1,024

Registers Per Thread register/thread 16

Shared Memory Configuration Size Kbyte 32.77

Driver Shared Memory Per Block byte/block 0

Dynamic Shared Memory Per Block byte/block 0

Static Shared Memory Per Block Kbyte/block 16.38

Threads thread 1,048,576

Waves Per SM 25.60

---------------------------------------------------------------------- --------------- ------------------------------

Section: Occupancy

---------------------------------------------------------------------- --------------- ------------------------------

Block Limit SM block 16

Block Limit Registers block 4

Block Limit Shared Mem block 2

Block Limit Warps block 1

Theoretical Active Warps per SM warp 32

Theoretical Occupancy % 100

Achieved Occupancy % 14.11

Achieved Active Warps Per SM warp 4.51

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel's theoretical occupancy is not impacted by any block limit. The difference between calculated

theoretical (100.0%) and measured achieved occupancy (14.1%) can be the result of warp scheduling overheads

or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block

as well as across blocks of the same kernel. See the CUDA Best Practices Guide

(<https://docs.nvidia.com/cuda/cuda-c-best-practices-guide/index.html#occupancy>) for more details on

optimizing occupancy.

histogram\_kernel(unsigned int \*, unsigned int \*, unsigned int, unsigned int), 2023-Dec-10 20:48:23, Context 1, Stream 14

Section: GPU Speed Of Light Throughput

---------------------------------------------------------------------- --------------- ------------------------------

DRAM Frequency cycle/nsecond 5.00

SM Frequency cycle/usecond 584.93

Elapsed Cycles cycle 1,989,995

Memory [%] % 15.90

DRAM Throughput % 0.01

Duration msecond 3.40

L1/TEX Cache Throughput % 16.19

L2 Cache Throughput % 4.73

SM Active Cycles cycle 1,954,355.10

Compute (SM) [%] % 15.90

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance

of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate

latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Section: Launch Statistics

---------------------------------------------------------------------- --------------- ------------------------------

Block Size 1,024

Function Cache Configuration cudaFuncCachePreferNone

Grid Size 1,024

Registers Per Thread register/thread 16

Shared Memory Configuration Size Kbyte 32.77

Driver Shared Memory Per Block byte/block 0

Dynamic Shared Memory Per Block byte/block 0

Static Shared Memory Per Block Kbyte/block 16.38

Threads thread 1,048,576

Waves Per SM 25.60

---------------------------------------------------------------------- --------------- ------------------------------

Section: Occupancy

---------------------------------------------------------------------- --------------- ------------------------------

Block Limit SM block 16

Block Limit Registers block 4

Block Limit Shared Mem block 2

Block Limit Warps block 1

Theoretical Active Warps per SM warp 32

Theoretical Occupancy % 100

Achieved Occupancy % 14.11

Achieved Active Warps Per SM warp 4.51

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel's theoretical occupancy is not impacted by any block limit. The difference between calculated

theoretical (100.0%) and measured achieved occupancy (14.1%) can be the result of warp scheduling overheads

or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block

as well as across blocks of the same kernel. See the CUDA Best Practices Guide

(<https://docs.nvidia.com/cuda/cuda-c-best-practices-guide/index.html#occupancy>) for more details on

optimizing occupancy.

histogram\_kernel(unsigned int \*, unsigned int \*, unsigned int, unsigned int), 2023-Dec-10 20:48:23, Context 1, Stream 15

Section: GPU Speed Of Light Throughput

---------------------------------------------------------------------- --------------- ------------------------------

DRAM Frequency cycle/nsecond 5.00

SM Frequency cycle/usecond 584.92

Elapsed Cycles cycle 1,989,975

Memory [%] % 15.90

DRAM Throughput % 0.00

Duration msecond 3.40

L1/TEX Cache Throughput % 16.19

L2 Cache Throughput % 4.74

SM Active Cycles cycle 1,954,390.07

Compute (SM) [%] % 15.90

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance

of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate

latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Section: Launch Statistics

---------------------------------------------------------------------- --------------- ------------------------------

Block Size 1,024

Function Cache Configuration cudaFuncCachePreferNone

Grid Size 1,024

Registers Per Thread register/thread 16

Shared Memory Configuration Size Kbyte 32.77

Driver Shared Memory Per Block byte/block 0

Dynamic Shared Memory Per Block byte/block 0

Static Shared Memory Per Block Kbyte/block 16.38

Threads thread 1,048,576

Waves Per SM 25.60

---------------------------------------------------------------------- --------------- ------------------------------

Section: Occupancy

---------------------------------------------------------------------- --------------- ------------------------------

Block Limit SM block 16

Block Limit Registers block 4

Block Limit Shared Mem block 2

Block Limit Warps block 1

Theoretical Active Warps per SM warp 32

Theoretical Occupancy % 100

Achieved Occupancy % 14.11

Achieved Active Warps Per SM warp 4.51

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel's theoretical occupancy is not impacted by any block limit. The difference between calculated

theoretical (100.0%) and measured achieved occupancy (14.1%) can be the result of warp scheduling overheads

or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block

as well as across blocks of the same kernel. See the CUDA Best Practices Guide

(<https://docs.nvidia.com/cuda/cuda-c-best-practices-guide/index.html#occupancy>) for more details on

optimizing occupancy.

histogram\_kernel(unsigned int \*, unsigned int \*, unsigned int, unsigned int), 2023-Dec-10 20:48:23, Context 1, Stream 16

Section: GPU Speed Of Light Throughput

---------------------------------------------------------------------- --------------- ------------------------------

DRAM Frequency cycle/nsecond 5.00

SM Frequency cycle/usecond 584.93

Elapsed Cycles cycle 1,990,017

Memory [%] % 15.90

DRAM Throughput % 0.00

Duration msecond 3.40

L1/TEX Cache Throughput % 16.19

L2 Cache Throughput % 4.71

SM Active Cycles cycle 1,954,368.23

Compute (SM) [%] % 15.90

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance

of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate

latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Section: Launch Statistics

---------------------------------------------------------------------- --------------- ------------------------------

Block Size 1,024

Function Cache Configuration cudaFuncCachePreferNone

Grid Size 1,024

Registers Per Thread register/thread 16

Shared Memory Configuration Size Kbyte 32.77

Driver Shared Memory Per Block byte/block 0

Dynamic Shared Memory Per Block byte/block 0

Static Shared Memory Per Block Kbyte/block 16.38

Threads thread 1,048,576

Waves Per SM 25.60

---------------------------------------------------------------------- --------------- ------------------------------

Section: Occupancy

---------------------------------------------------------------------- --------------- ------------------------------

Block Limit SM block 16

Block Limit Registers block 4

Block Limit Shared Mem block 2

Block Limit Warps block 1

Theoretical Active Warps per SM warp 32

Theoretical Occupancy % 100

Achieved Occupancy % 14.11

Achieved Active Warps Per SM warp 4.51

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel's theoretical occupancy is not impacted by any block limit. The difference between calculated

theoretical (100.0%) and measured achieved occupancy (14.1%) can be the result of warp scheduling overheads

or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block

as well as across blocks of the same kernel. See the CUDA Best Practices Guide

(<https://docs.nvidia.com/cuda/cuda-c-best-practices-guide/index.html#occupancy>) for more details on

optimizing occupancy.

convert\_kernel(unsigned int \*, unsigned int), 2023-Dec-10 20:48:24, Context 1, Stream 7

Section: GPU Speed Of Light Throughput

---------------------------------------------------------------------- --------------- ------------------------------

DRAM Frequency cycle/nsecond 4.80

SM Frequency cycle/usecond 561.84

Elapsed Cycles cycle 3,598

Memory [%] % 4.27

DRAM Throughput % 1.13

Duration usecond 6.40

L1/TEX Cache Throughput % 10.09

L2 Cache Throughput % 1.94

SM Active Cycles cycle 1,522.45

Compute (SM) [%] % 4.27

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance

of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate

latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Section: Launch Statistics

---------------------------------------------------------------------- --------------- ------------------------------

Block Size 4

Function Cache Configuration cudaFuncCachePreferNone

Grid Size 1,024

Registers Per Thread register/thread 16

Shared Memory Configuration Size Kbyte 32.77

Driver Shared Memory Per Block byte/block 0

Dynamic Shared Memory Per Block byte/block 0

Static Shared Memory Per Block byte/block 0

Threads thread 4,096

Waves Per SM 1.60

---------------------------------------------------------------------- --------------- ------------------------------

WRN Threads are executed in groups of 32 threads called warps. This kernel launch is configured to execute 4

threads per block. Consequently, some threads in a warp are masked off and those hardware resources are

unused. Try changing the number of threads per block to be a multiple of 32 threads. Between 128 and 256

threads per block is a good initial range for experimentation. Use smaller thread blocks rather than one

large thread block per multiprocessor if latency affects performance. This is particularly beneficial to

kernels that frequently call \_\_syncthreads(). See the Hardware Model

(<https://docs.nvidia.com/nsight-compute/ProfilingGuide/index.html#metrics-hw-model>) description for more

details on launch configurations.

----- --------------------------------------------------------------------------------------------------------------

WRN A wave of thread blocks is defined as the maximum number of blocks that can be executed in parallel on the

target GPU. The number of blocks in a wave depends on the number of multiprocessors and the theoretical

occupancy of the kernel. This kernel launch results in 1 full waves and a partial wave of 384 thread blocks.

Under the assumption of a uniform execution duration of all thread blocks, the partial wave may account for

up to 50.0% of the total kernel runtime with a lower occupancy of 42.6%. Try launching a grid with no

partial wave. The overall impact of this tail effect also lessens with the number of full waves executed for

a grid. See the Hardware Model

(<https://docs.nvidia.com/nsight-compute/ProfilingGuide/index.html#metrics-hw-model>) description for more

details on launch configurations.

Section: Occupancy

---------------------------------------------------------------------- --------------- ------------------------------

Block Limit SM block 16

Block Limit Registers block 128

Block Limit Shared Mem block 16

Block Limit Warps block 32

Theoretical Active Warps per SM warp 16

Theoretical Occupancy % 50

Achieved Occupancy % 28.68

Achieved Active Warps Per SM warp 9.18

---------------------------------------------------------------------- --------------- ------------------------------

WRN This kernel's theoretical occupancy (50.0%) is limited by the required amount of shared memory This kernel's

theoretical occupancy (50.0%) is limited by the number of blocks that can fit on the SM The difference

between calculated theoretical (50.0%) and measured achieved occupancy (28.7%) can be the result of warp

scheduling overheads or workload imbalances during the kernel execution. Load imbalances can occur between

warps within a block as well as across blocks of the same kernel. See the CUDA Best Practices Guide

(<https://docs.nvidia.com/cuda/cuda-c-best-practices-guide/index.html#occupancy>) for more details on

optimizing occupancy.